SD Card Specification
SD3.0 UHS-I

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Revision History:

Rev.	***Date***	***Changes***	***Remark***
1.0	2013/12/01	Basic spec and architecture	Preliminary

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1. Overview

1.1 Product Description

The SD3.0 Cards are fully compatible with Physical Layer Specification, Version 3.0 (this specification is available from the SDA), support Ultra High Speed(UHS), provides high write/read speed and high IOPS, It was designed to meet the security, high capacity, high performance and environmental requirements inherent in next generation consumer electronic devices.

The SD card system is a new mass-storage system based on innovations in semiconductor technology. It has been developed to provide an inexpensive, mechanically robust storage medium in card form for multimedia consumer applications. SD card allows the design of inexpensive players and drivers without moving parts. A low power consumption and a wide supply voltage range favors consumer electronic devices.

1.2 Features Summary

-Capacity: 4GB/8GB

-Complies to SD specifications version 3.0

-Voltage operating: 2.7~3.6V.

-Targeted for portable and stationary applications

-Greater Performance Choices

-Bus Speed Mode:

DS-Default Speed mode: 3.3V signaling, frequency up to 25MHz, up to 12.5MB/sec

HS-High Speed mode: 3.3V signaling, frequency up to 50MHz, up to 25MB/sec

SDR12-1.8V signaling, frequency up to 25MHz, up to 12.5MB/sec

SDR25-1.8V signaling, frequency up to 50MHz, up to 25MB/sec

SDR50-1.8V signaling, frequency up to 100MHz, up to 50MB/sec

SDR104-1.8V signaling, frequency up to 208MHz, up to 104MB/sec

DDR50-1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50MB/s

-Switch function command supports Bus Speed Mode, Command System, Drive Strength, and future functions.

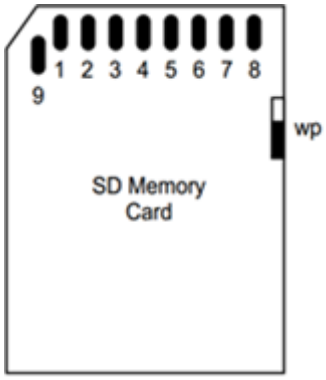
-password protection (CMD42-LOCK_UNLOCK)

-Sophisticated system for error recovery including a powerful ECC

-Global Wear Leveling

-Power management for low power operation

2. Pin Assignment



Pin No.	SD Mode			SPI Mode		
	Name	Type	Description	Name	Type	Description
1	CD/DAT 3	I/O/PP	Card Detect / Data Line [Bit 3]	CS	I[3]	Chip Select (neg true)
2	CMD	PP	Command/Response	DI	I	Data In
3	VSS	S	Supply voltage ground	VSS1	S	Supply voltage ground
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line [Bit 1]	RSV		-
9	DAT2	I/O/PP	Data Line [Bit 2]	RSV		-

S: power supply; I: input; O: output; PP: I/O using push-pull drivers

Table 1: Pin Assignment

3. Product List

Part Number	Capacity	Actual Size	Speed Class (Note1)	UHS-I (Note1)	Type
MKSD004G-CGT1	4GB	3.24GB	C10,U1,V10	SDR104	SDHC
MKSD008G-CGT1	8GB	7.24GB	C10,U1,V10	SDR104	SDHC

Table 2：Product List

Note1：*Measurement based on VTE3100 Test Metrix device, SW 3.2A software or up version.
Test scripts:
SD_Card(Spec3.0_High&Extended-Capacity_UHS-I and Non-UHS-I)_Compliance [rev31R].vte
SDR104@SDR104-208MHz.
SD_Card (Spec2.0-3.0 High&Extended-Capacity_UHS-I) Performance-Speed (Multiple Block Sequential) [rev31M] - SDR104-With Background Data.vte]

**Maximum speed differs from the bus I/F speed. It varies depending upon the card performance. The average speed that a device writes to an SD memory card may vary depending upon the device and the operation it is performing. Normal and high-speed cards can also be used with UHS-I host devices, but the high performance enabled by a UHS-I host device can only be achieved with a UHS- I memory card.*

4. Current Consumption

Standby current: 500uA（Maximum value）
Standby current: 250uA（average value）
Operating current: 250mA（Maximum value）
Operating current: 150mA（average value）
*Test condition: Realtek5308 card reader (Voltage 3.3V), Fluke289C multi-meter.

5. Reliability and Durability

Temperature	Operation: -25°C/85°C Storage: -25°C/85°C
Moisture and corrosion	Operation: 25°C/95% rel. humidity Storage: 40°C/93% rel. hum./500h Salt Water Spray: 3% NaCl/35C; 24h acc. MIL STD Method 1009
Durability	10,000 insertion/removal cycles;
Bending	10[N] Center 200[mm/minute] 60[sec]
Torque	0.10Nm,+/-2.5 deg.max.
Drop test	1.5m free fall
Electrostatic Discharge (ESD)	IEC 61000-4-2 contact discharge: +/- 2[kV] and +/- 4[kV] 150[pF],330[Ohm] air discharge: up to +/- 15[kV] 150[pF], 330[Ohm]

Table 3: Reliability and Durability

6. SD Card Registers

6.1 Card Identification Register (CID)

The Card Identification (CID) register is 128 bit wide. It contains the card identification information used during the card identification phase. Every individual flash card shall have a unique identification number.

The structure of the CID register is defined in the following table.

CID Bit	Width	Name	Field
[127:120]	8	Manufacture ID	MID
[119:104]	16	OEM/Application ID	OID
[103:64]	40	Product Name	PNM
[63:56]	8	Product Revision	PRV
[55:24]	32	Product Serial Number	PSN
[23:20]	4	Reserved	---
[19:8]	12	Manufacturing Date	MDT
[7:1]	7	CRC7 check sum	CRC
[0]	1	Not used,always”1	---

Table 4: SD Card CID Table

- All contents in the CID table are programmable; Manufacturers can update the CID data through utility.
- Manufacturers should license MID and OID field form the SD Card Association(SDA)

6.2 Card Specific Data Register (CSD)

The Card-Specific Data register provides information regarding access to the card contents. The CSD defines the data format, error correction type, maximum data access time, whether the DSR register can be used, etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The CSD Table Version 2.0(as shown below) is applied to SDHC and SDXC Cards. Note that bits [15:0] are programmable by the host side. Refer to the SD specification for detailed information

CSD Bit	Width	Name	Field	Value	Note
[127:126]	2	CSD structure	CSD_STRUCTURE	01b	V2.0(>2G B Card)
[125:120]	6	Reserved	---	---	---
[119:112]	8	Data read access-time 1	(TAAC)	0E h	
[111:104]	8	Data read access-time2 in CLK cycles(NSA*100)	(NSAC)	00 h	
[103:96]	8	Max data transfer rate	(TRAN_SPEED)	32 h 5A h 0B h 2B h	
[95:84]	12	Card command classes	CCC	5B5 h	
[83:80]	4	Max. read data block length	(READ_BL_LEN)	9 h	512 Byte
[79]	1	Partial block read allowed	(READ_BL_PARTIAL)	0	
[78]	1	Write block misalignment	(WRITE_BLK_MISALIGN)	0	
[77]	1	Read block misalignment	(READ_BLK_MISALIGN)	0	
[76]	1	DSR implemented	DSR_IMP	x	
[75:70]	6	Reserve	---	---	
[69:48]	22	Device size	C_SIZE	xxxxxxh	
[47]	1	Reserved	---	0	
[46]	1	Erase single block enable	(ERASE_BLK_EN)	1	
[45:39]	7	Erase sector size	(SECTOR_SIZE)	7F h	
[38:32]	7	Write protect group size	C_SIZE	0 b	
[31]	1	Write protect group enable	---	0	
[30:29]	2	Reserved	(ERASE_BLK_EN)	0 b	
[28:26]	3	Write speed factor	(SECTOR_SIZE)	010 b	
[25:22]	4	Max. write data block length	(WP_GRP_SIZE)	9 h	
[21]	1	Partial block write allowed	(WP_GRP_ENABLE)	0	
[20:16]	5	Reserved	---	---	
[15]	1	File format group	(FILE_FORMAT_GRP)	0	
[14]	1	Copy flag	COPY	x	
[13]	1	Permanent write protection	PERM_WRITE_PROTECT	x	
[12]	1	Temporary write protection	TMP_WRITE_PROTECT	x	
[11:10]	2	File format	(FILE_FORMAT)	00 b	
[9:8]	2	Reserved	---	00 b	
[7:1]	7	CRC	CRC	---	
[0]	1	Not used,always'1'	---	1	

Table 5: CSD (Version 2.0) Table

7. Bus Operation Conditions

7.1 For 3.3V Signaling

7.1.1 Threshold Level for High Voltage Range

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75* V_{DD}		V	I_{OH}=2mA $V_{DD\ min}$
Output Low Voltage	V_{OL}		0.125* V_{DD}	V	I_{OL}=2mA $V_{DD\ min}$
Input High Voltage	V_{IH}	0.625* V_{DD}	V_{ss}+0.3	V	
Input Low Voltage	V_{IL}	V_{ss}-0.3	0.25* V_{DD}	V	
Power Up Time			250	ms	From 0V to $V_{DD\ min}$

Table 6: Threshold Level for High Voltage

7.1.2 Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max	Unit	Remark
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

Table 7: Peak Voltage and Leakage Current

7.1.3 Bus Signal Line Load

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	K'Ω	To prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card C_{HOST}+C_{BUS} shall not exceed 30pF
Card capacitance for each signal pin	C_{CARD}		10	pF	
Maximum signal inductance			16	nH	
Pull-up resistance inside card(pin1)	R_{DAT3}	10	90	K'Ω	May be used for card detection
Capacity Connected to Power Line	C_C		5	uF	To prevent inrush current

Table 8: Bus Operating Conditions - Signal Line's Load

7.1.4 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

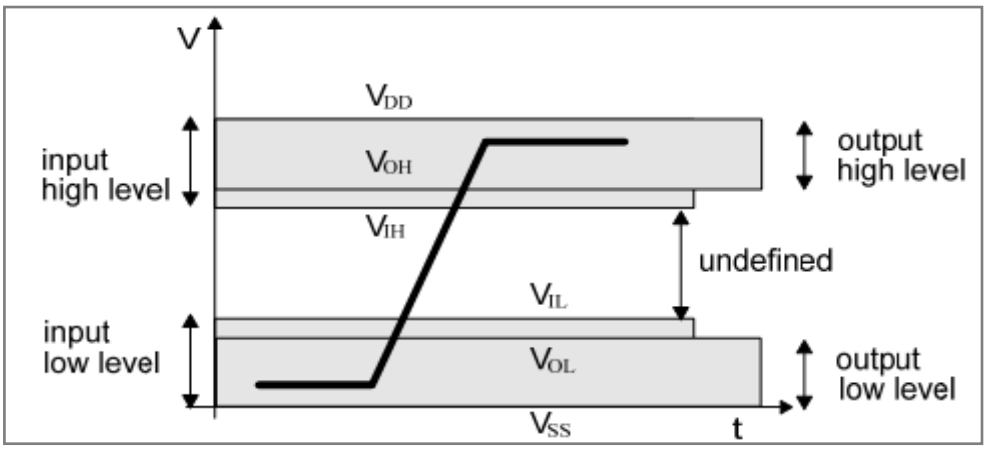


Figure 1: Bus Signal Levels

To meet the requirements of the JEDEC specification JESD8-1A and JESD8-7, the card input and output voltages shall be within the specified ranges shown in Table 6-2 for any VDD of the allowed voltage range:

7.1.5 Bus Timing(Default)

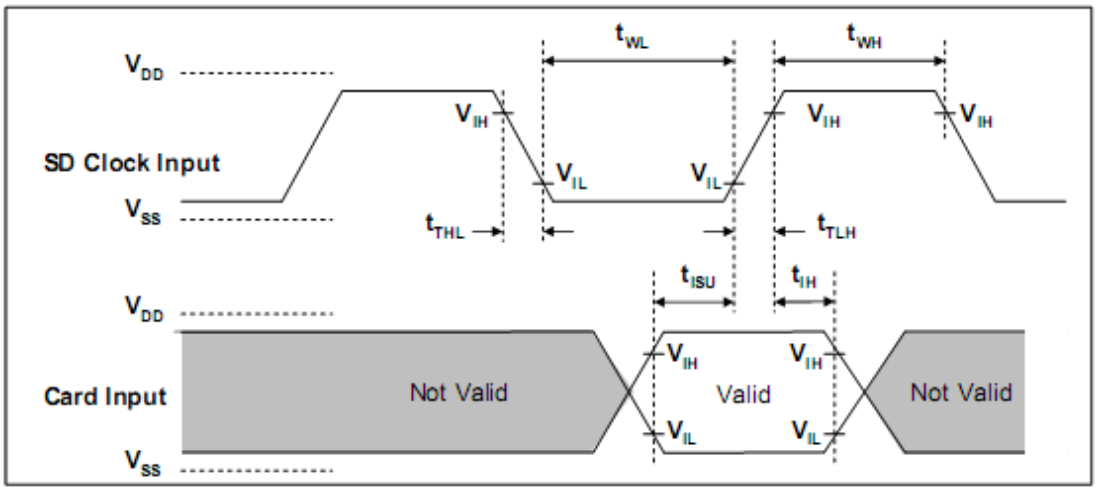


Figure 2: Card input Timing (Default Speed Card)

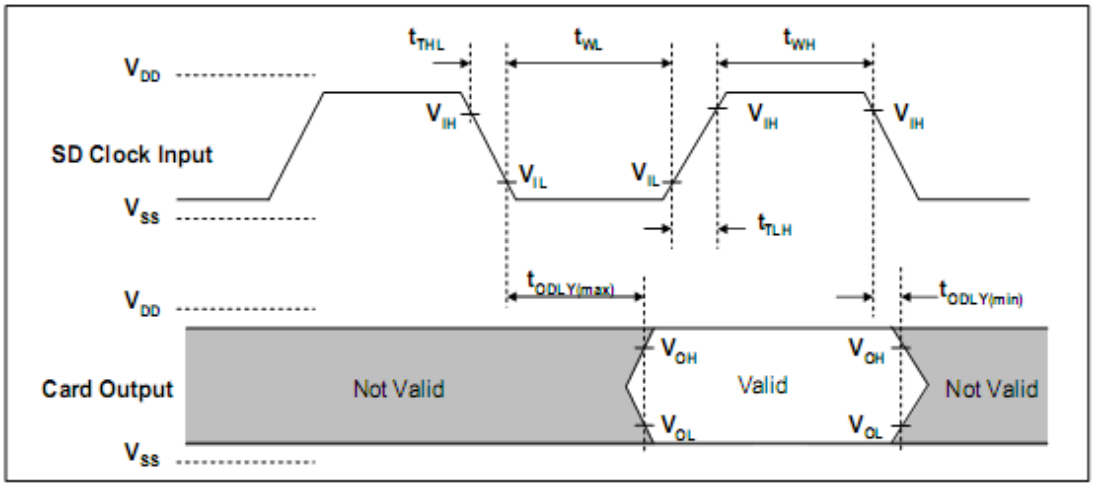


Figure 3: Card Output Timing (Default Speed Mode)

(1) 0 Hz means to stop the clock.The given minimum frequency range is for cases were continues clock is required (refer to Chapter 4.4-Clock Control)

Parameter	**Symbol**	**Min.**	**Max**	**Unit**	**Remark**
Clock CLK （All values are referred to min（V_{IH}）and max（V_{IL}））					
Clock frequency data transfer Mode	fpp	0	25	MHz	C_{CARD} ≤ 10pF (1 card)
Clock frequency Identification Mode	f_{OD}	0(1)/100	400	KHz	C_{CARD} ≤ 10pF (1 card)
Clock low time	t_{WL}	10		ns	C_{CARD} ≤ 10pF (1 card)
Clock high time	t_{WH}	10		ns	C_{CARD} ≤ 10pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{CARD} ≤ 10pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{CARD} ≤ 10pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{CARD} ≤ 10pF (1 card)
Input hold time	t_{IH}	5		ns	C_{CARD} ≤ 10pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L ≤ 40pF (1 card)
Output Hold time	t_{OH}	0	50	ns	C_L ≤ 40pF (1 card)

Table 9: Bus Timing-Parameters Values (Default Speed)

7.1.6 Bus Timing (High-Speed Mode)

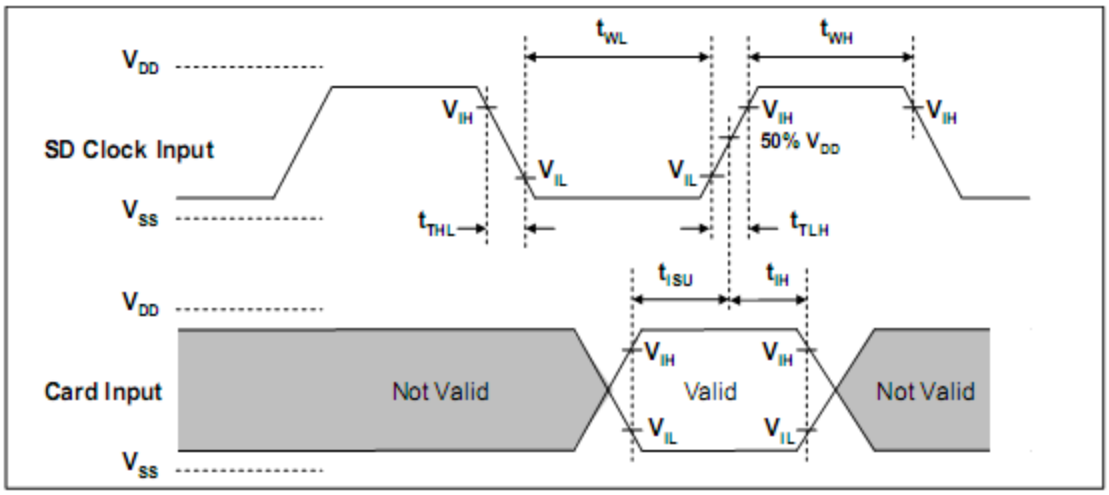


Figure 4:Card Input Timing(High Speed Card)

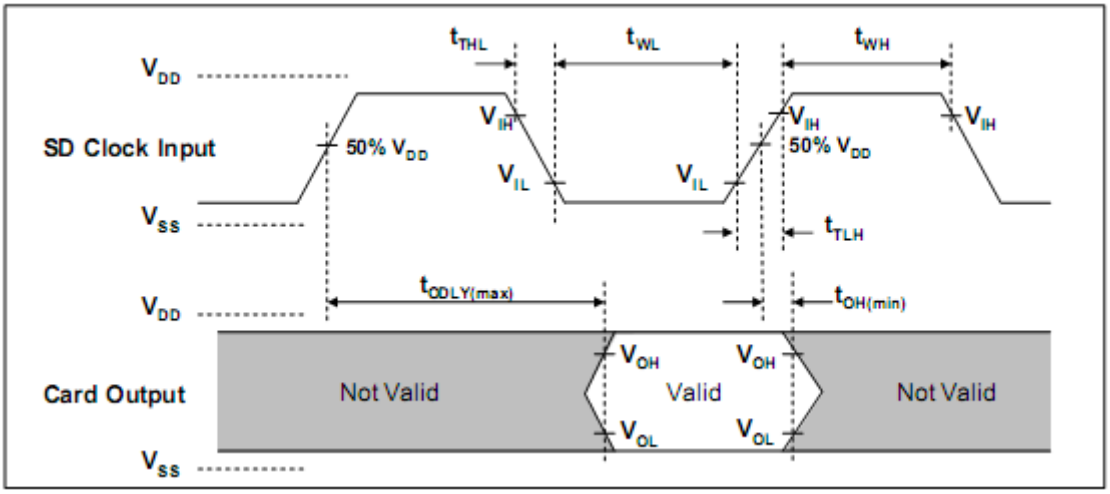


Figure 5: Card Output Timing(High Speed Mode)

Parameter	Symbol	Min.	Max	Unit	Remark
Clock CLK （All values are referred to min（V_{IH}）and max（V_{IL}））					
Clock frequency data transfer Mode	fpp	0	50	MHz	C_{CARD} ≤ 10pF (1 card)
Clock low time	t_{WL}	7		ns	C_{CARD} ≤ 10pF (1 card)
Clock high time	t_{WH}	7		ns	C_{CARD} ≤ 10pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{CARD} ≤ 10pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{CARD} ≤ 10pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{CARD} ≤ 10pF (1 card)
Input hold time	t_{TH}	2		ns	C_{CARD} ≤ 10pF (1 card)
Outputs CMD, DAT (referenced to CLK)					

Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	$C_L \leq 40pF$ (1 card)
Output Hold time	t_{OH}	2.5		ns	$C_L \geq 15pF$ (1 card)
Total System capacitance for each line[1p]	C_L		40	pF	1 card

(1) In order to satisty sever timing , host shall drive only one card.

Table 10: Bus Timing – Parameters Values (High Speed)

7.2 For 1.8V Signaling

7.2.1 Threshold Level for High Voltage Range

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4		V	I_{OH}=2mA $V_{DD\ min}$
Output Low Voltage	V_{OL}		0.45	V	I_{OL}=2mA $V_{DD\ min}$
Input High Voltage	V_{IH}	1.27	2.0	V	
Input Low Voltage	V_{IL}	V_{ss}-0.3	0.58	V	

Table 11: Threshold Level for High Voltage

7.2.2 Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max	Unit	Remark
Input Leakage Current		-2	2	uA	DAT3 pull-up is disconnected

Table 12: Peak Voltage and Leakage Current

7.2.3 Bus Timing Specification in SDR12, SDR25, SDR50 and SDR104 Modes

7.2.3.1 Clock Timing

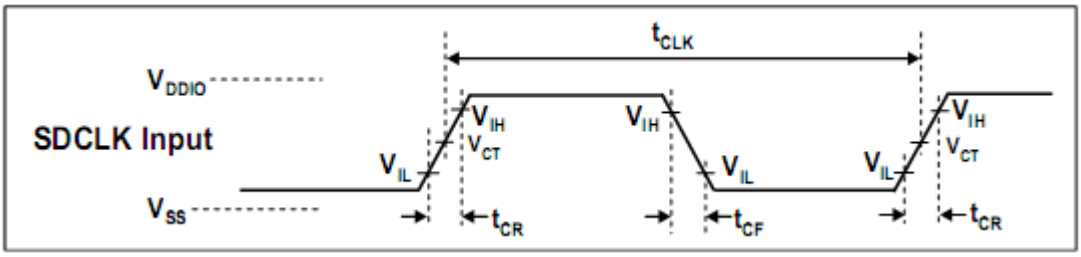


Figure 6: Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.8	-	ns	208MHz (Max.), Between rising edge, V_{CT}=0.975V
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	tCR, tCF < 2.00ns (max.) at 208MHz, CCARD=10pF tCR, tCF < 2.00ns (max.) at 100MHz, CCARD=10pF The absolute maximum value of tCR, tCF is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

Table 13: Clock Signal Timing

7.2.3.2 Card Input Timing

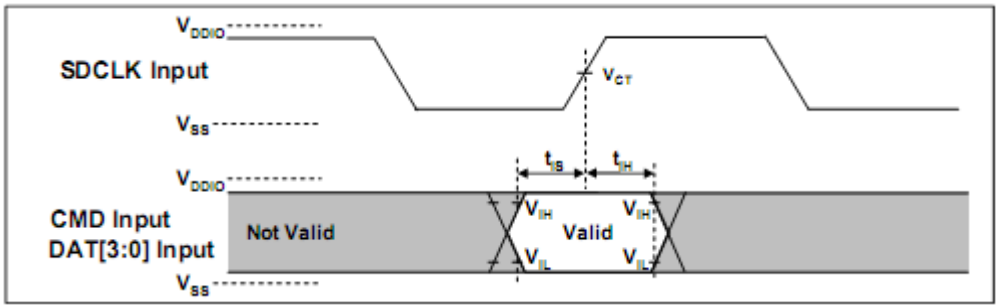


Figure 7: Card Input Timing

Symbol	Min	Max	Unit	SDR104 mode
t_{IS}	1.40	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80		ns	C_{CARD} = 5pF, V_{CT} = 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR12, SDR25 and SDR50 modes**
t_{IS}	3.00	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V

Table 14: SDR50 and SDR104 Input Timing

7.2.3.3 Card Output Timing

7.2.3.3.1 Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50)

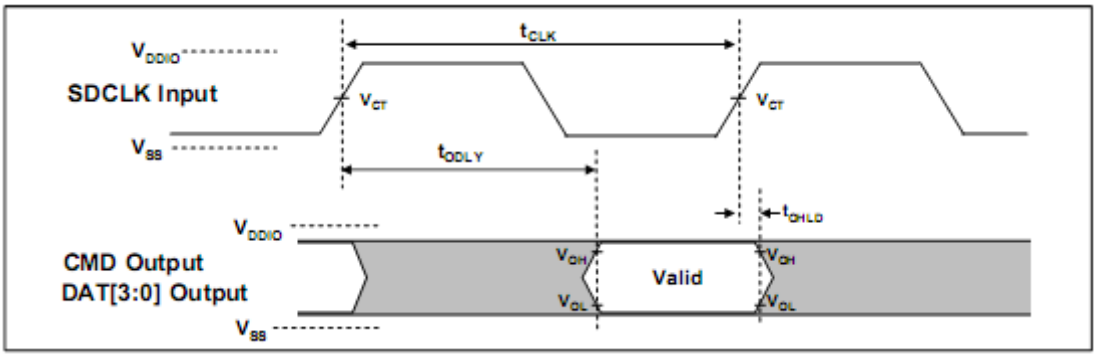


Figure 8: Output Timing of Fixed Data Window

Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK} ≥10.0ns, CL=30pF, using driver Type B, for SDR50.
t_{ODLY}		14	ns	t_{CLK} ≥20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12.
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.). CL=15pF

Table 15: Output Timing of Fixed Data Window

7.2.3.3.2 Output Timing of Variable Window (SDR104)

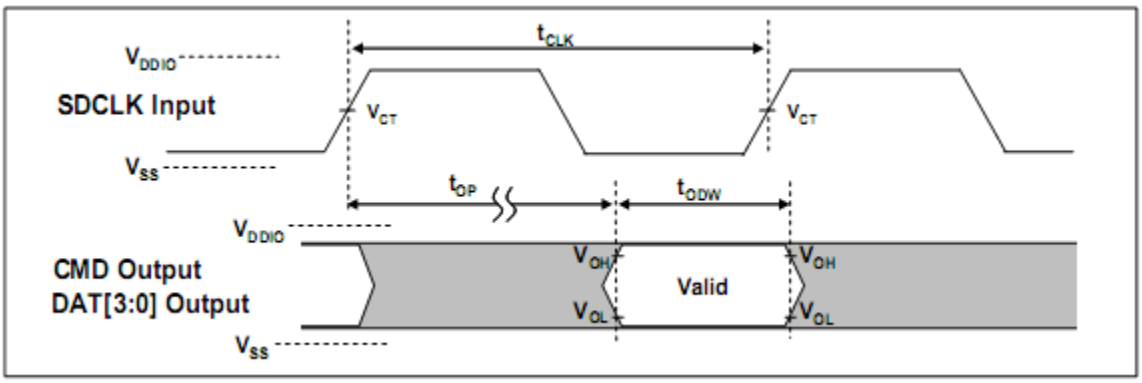


Figure 9: Output Timing of Variable Data Window

Symbol	Min	Max	Unit	Remark
t_{OP}	-	2	UI	Card Output Phase
$\triangle t_{OP}$	-350	+1550	ps	Delay variation due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

Table 16: Output Timing of Variable Data Window

8. Physical Dimension

Type	Measurement
Length	32.00mm ±0.10mm
Width	24.00mm ±0.10mm
Thickness	2.10mm ±0.15mm
Weight	Approx.2.0 gram

Physical Dimension Specifications (Unit in mm)

Mechanical form factor as follows: (Unit in mm)

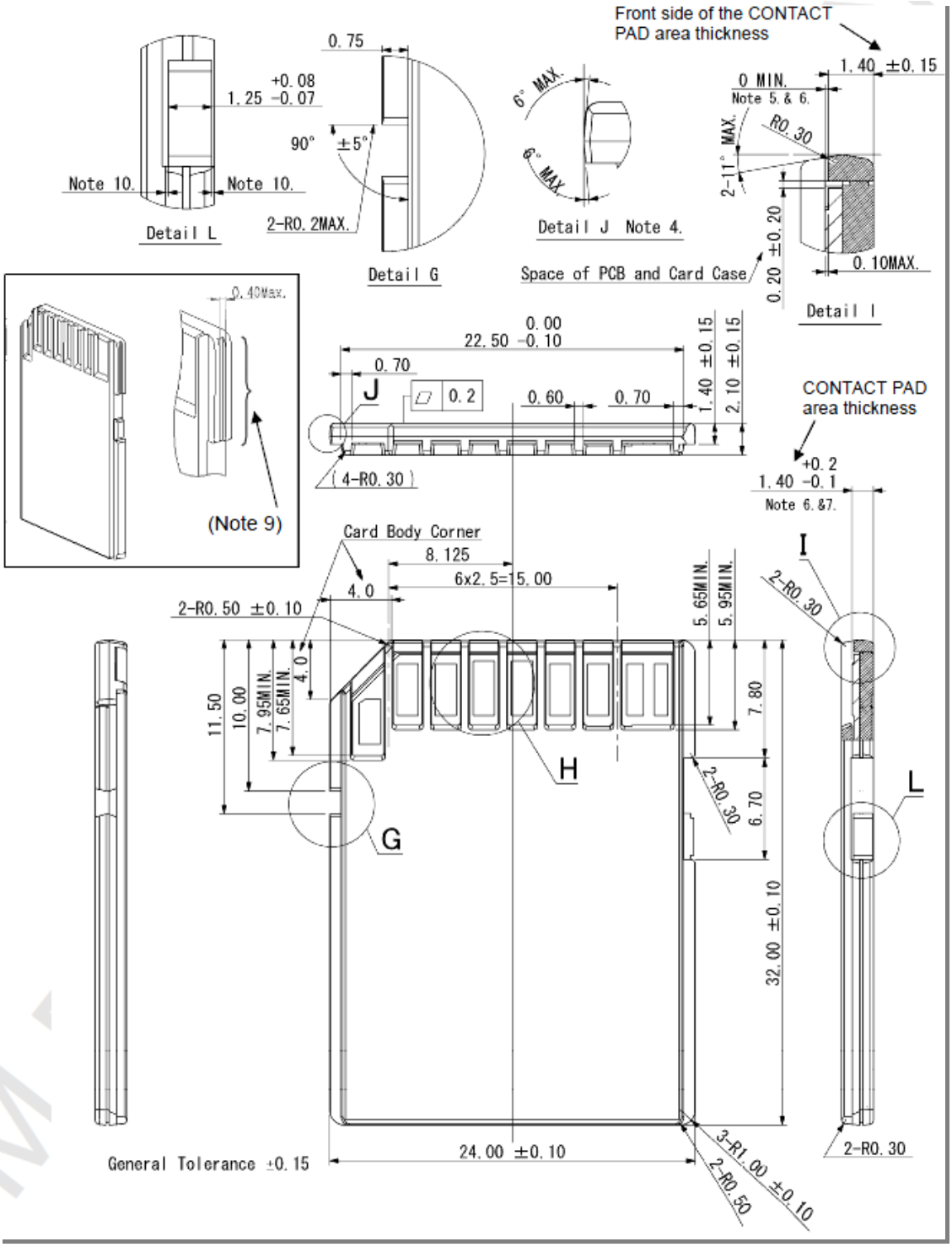


Figure 10: Dimension Drawing

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