HFC0310

Programmable Fixed-Frequency Flyback Controller

DESCRIPTION

The HFC0310 is a flyback controller with programmable fixed-frequency operation.

The controller uses peak current mode to provide excellent transient response and ease loop compensation. When the output power falls below a given level, the controller enters burst mode to lower the stand-by power consumption.

An external capacitor connected between the FSET pin and GND programs the HFC0310 switching frequency. Otherwise, the HFC0310 uses a frequency shaping function that greatly reduces the noise level, and reduces the cost of the EMI filter.

The HFC0310 provides various protections, such as thermal shutdown, V_{CC} under-voltage lockout, over-load protection, over-voltage protection, and short-circuit protection.

The HFC0310 is available in a SOIC8 package.

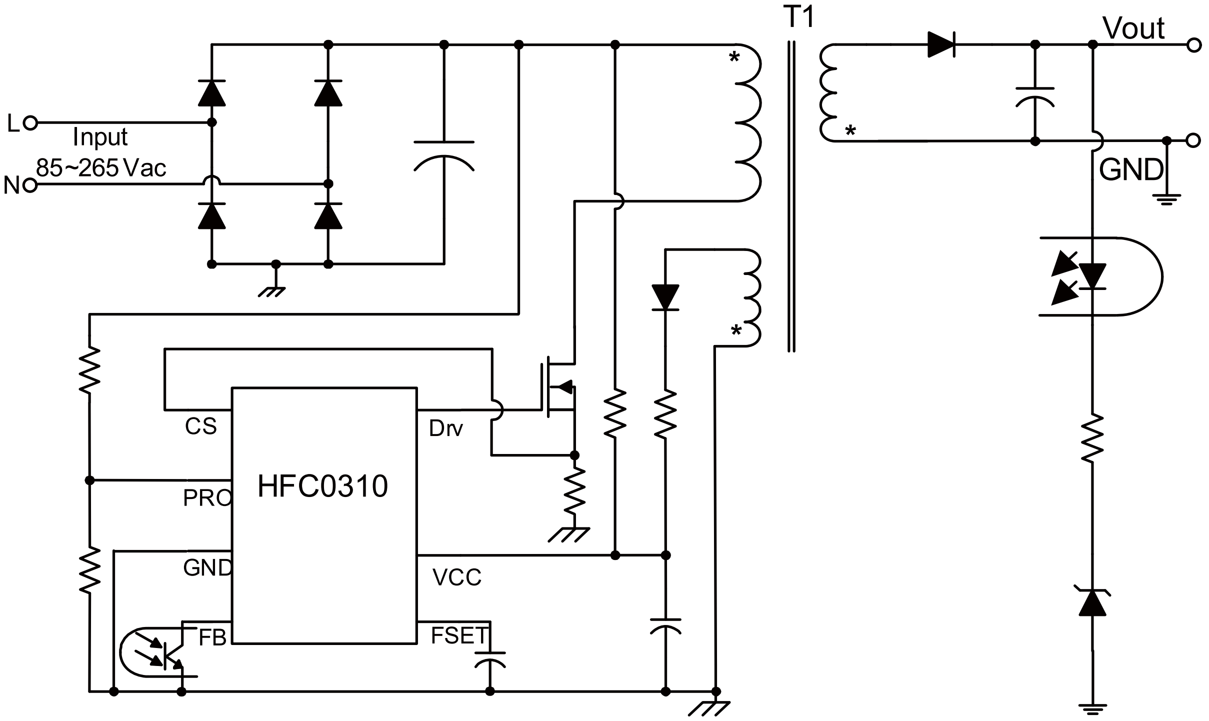
FEATURES

- Programmable switching frequency up to 600kHz
- Frequency shaping
- Current-mode operation
- Very low start-up current
- Very low standby power consumption via active-burst mode
- Internal leading-edge blanking
- Built-in soft-start function
- Internal slope compensation
- External protection with recovery hysteresis on PRO pin
- Over-temperature protection
- V_{CC} under-voltage lockout with hysteresis
- Over-voltage protection on VCC
- Time-based over-load protection
- Short-circuit protection

APPLICATIONS

- Power Meters
- Switching Mode Power Supplies
- AC/DC Adapters, Switching Chargers

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
HFC0310GS	SOIC8	*See below*

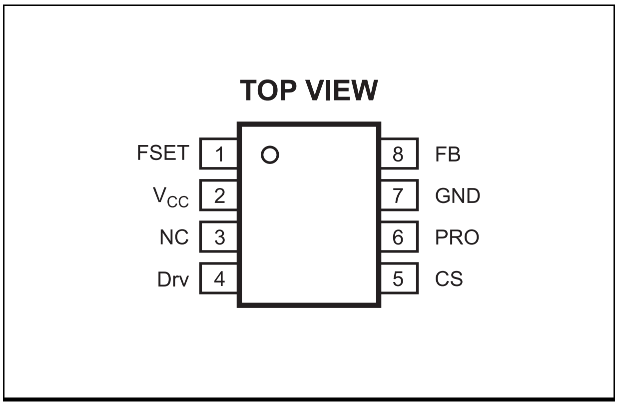
* For Tape & Reel, add suffix –Z (e.g. HFC0310GS–Z);

TOP MARKING

HFC0310
LLLLLLLL
MPSYWW

MPS: MPS prefix
Y: year code
WW: week code
HFC0310: part number
LLLLLLLL: lot number

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Vcc, Drv to GND .... –0.3V to 30 V
All Other Pins to GND.................... –0.3V to 7 V
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC8.. 1.3W
Junction Temperature .... 150°C
Lead Temperature .... 260°C
Storage Temperature................-60°C to +150°C
ESD Capability Human Body Model.......... 2.0kV
ESD Capability Machine Model 200V

Recommended Operation Conditions (3)

V_{CC} to GND .... 11V to 20V

Thermal Resistance (4)

Thermal Resistance (4)	θ_{JA}	θ_{JC}	
SOIC8	96	45	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VCC = 12V, T_J = -40°C to 105°C, min and max values are guaranteed by characterization, typical values are tested under 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Driving Signal (Pin Drv)						
Sourcing Resistor	R_H		17	25	34	Ω
Sinking Resistor	R_L		9	13	17	Ω
Supply Voltage Management (Pin Vcc)						
V_{CC} Upper Turn-On/Off Level	V_{CCH}		10.8	12	13.2	V
V_{CC}, Lower Turn-On/Off Level	V_{CCL}		8.5	9.5	10.5	V
Start-Up Current	I_{ST}	V_{CC}=V_{CCH}-0.5V, Before start up		12	20	μA
V_{CC} OVP Level	V_{OVP}		21	23	25	V
V_{CC} Protection-Enabled Recharge Level	V_{CCR}		5.8	6.4	7.0	V
Internal IC Consumption, Protection Phase	I_{Pro}	V_{CC} =6.0V		8	12	μA
Feedback Management (Pin FB)						
Internal Pull-Up Resistor	R_{FB}		12.5	14.5	17.0	kΩ
Internal Pull-Up Voltage	V_{UP}		4.25	4.55	4.85	V
FB to Current-Set–Point Division Ratio	I_{DIV}		3	3.5	4	
Internal Soft-Start Time	t_{SS}			3		ms
Falling FB Level Where the Regulator Enters Burst Mode	V_{BURL}		0.43	0.5	0.57	V
Rising FB Level where the Regulator Exits Burst Mode	V_{BURH}		0.66	0.73	0.80	V
Over-Load Set Point	V_{OLP}		3.5	3.75	4	V
Over-Load Delay Time	t_{Delay}	Fs=100kHz		82		ms
Timing Capacitor(FSET)						
Maximum Voltage on the FSET Capacitor	$V_{FSETmax}$		0.82	0.87	0.92	V
Source Current	I_{FSET}		40	50	60	μA
FSET Capacitor Discharge Time (Active at drive turn on)	t_{DISCH}			500		ns
Frequency Spectrum Shaping range, in percentage of Fs	$R_{Shaping}$			±3.5		%
Current Sampling Management (CS)						
Leading-Edge Blanking for Current Sensor	t_{LEB1}		180	280	400	ns
Leading-Edge Blanking for SCP	t_{LEB2}		150	250	370	ns
Maximum Current Set-Point	V_{CS}		0.90	0.97	1.03	V
Short-Circuit–Protection Set Point	V_{SCP}		1.60	1.72	1.84	V
Internal-Slope–Compensation Ramp	S_{Ramp}	f_S=100kHz	27	42	57	mV/μs
Protection Management (PRO)						
Protection Voltage	V_{PRO}		3.1	3.3	3.5	V
Protection Hysteresis	V_{HY}			0.2		V
Thermal Shutdown						
Thermal shutdown threshold (5)				150		°C
Thermal shutdown recovery hysteresis (5)				40		°C

Notes:

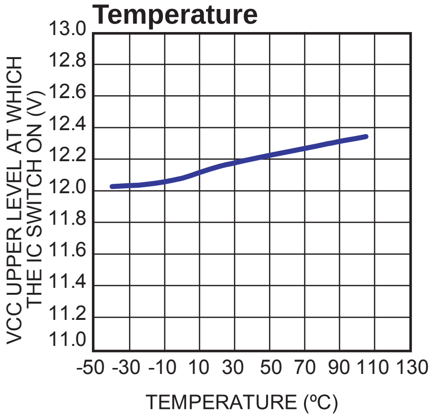
5) This parameter is guaranteed by design.

PIN FUNCTIONS

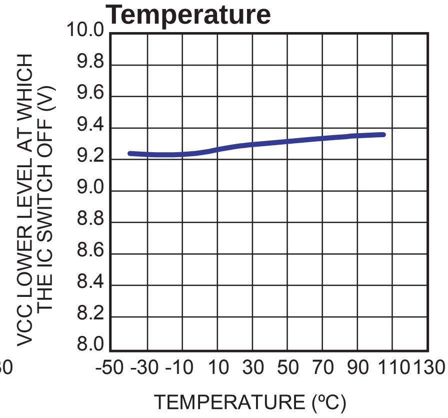
Package Pin #	Name	Description
1	FSET	Switching Frequency Set. Connect a capacitor to GND to set the switching frequency up to 600kHz.
2	V_{CC}	IC Power Supply.. Connect to a 47μF bulky capacitor and a 0.1μF ceramic capacitor for most applications.
3	NC	Not Connected.
4	Drv	Drive Signal Output.
5	CS	Primary Current Sense.
6	PRO	Pull up PRO to shut down the IC with hysteresis.
7	GND	Ground.
8	FB	Feedback. The output voltage from the external compensation circuit is fed into this pin. This pin and the current sense signal from Source determines the PWM duty cycle. Burst mode operation and Over Load Protection are also detected on it.

TYPICAL CHARACTERISTICS

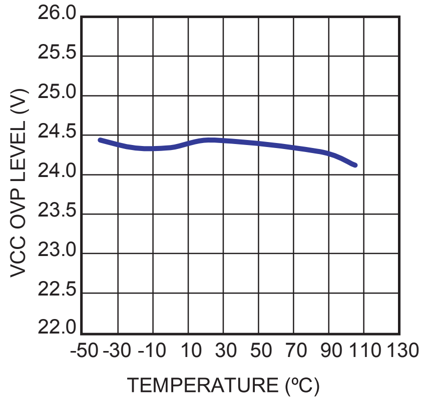
VCC Upper Level at which the IC switch on vs. Temperature



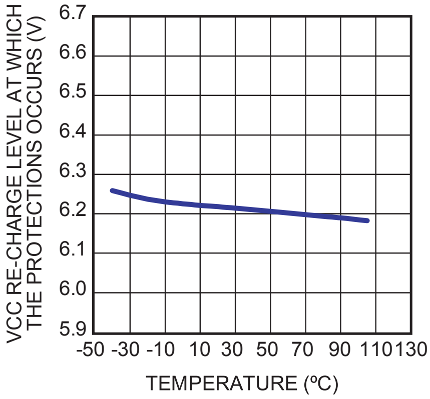
VCC Lower Level at which the IC switch off vs. Temperature



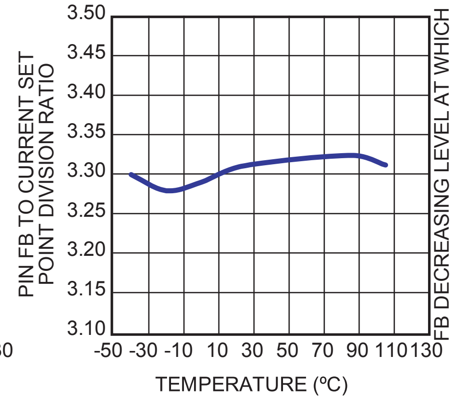
VCC OVP Level vs. Temperature



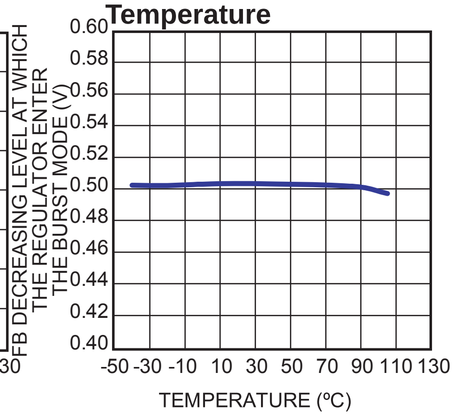
VCC Re-Charge Level at which the protections occurs vs.Temperature



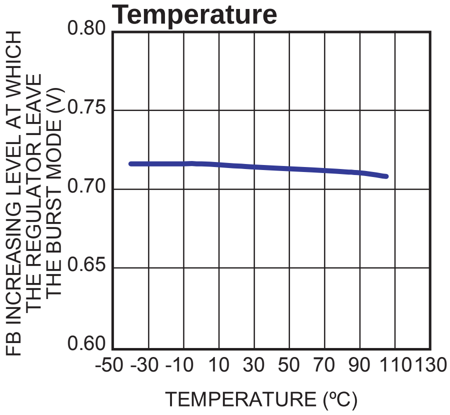
Pin FB to Current Set point Division Ratio vs. Temperature



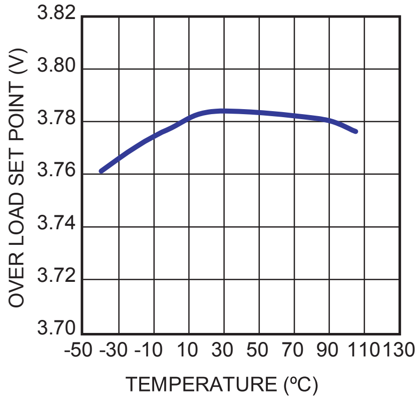
FB Decreasing Level at which the Regulator enter the Burst Mode vs. Temperature



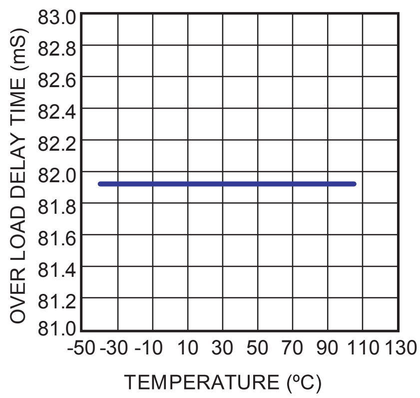
FB Increasing Level at which the Regulator leave the Burst Mode vs. Temperature



Over Load Set Point vs. Temperature

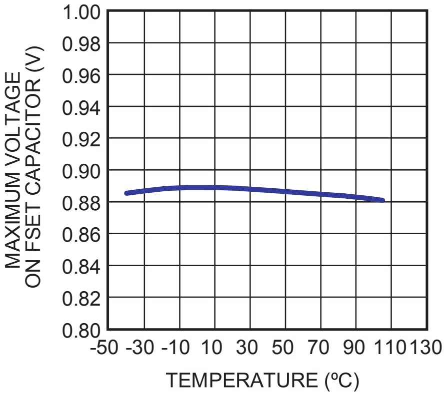


Over Load Delay Time vs. Temperature

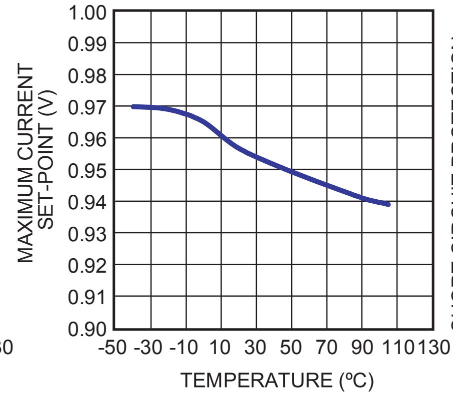


TYPICAL CHARACTERISTICS *(continued)*

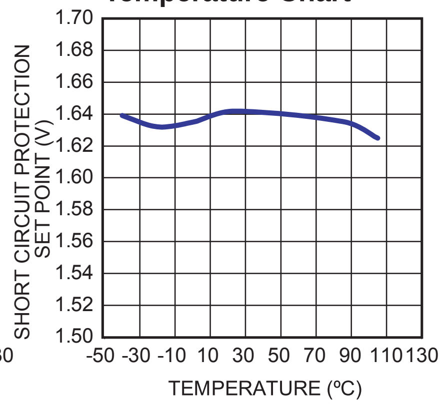
Maximum Voltage On FSET Capacitor vs. Temperature



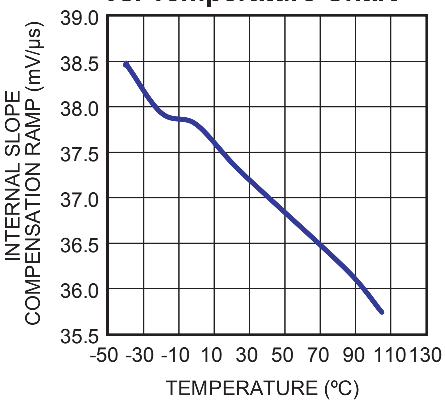
Maximum Current Set-point vs. Temperature



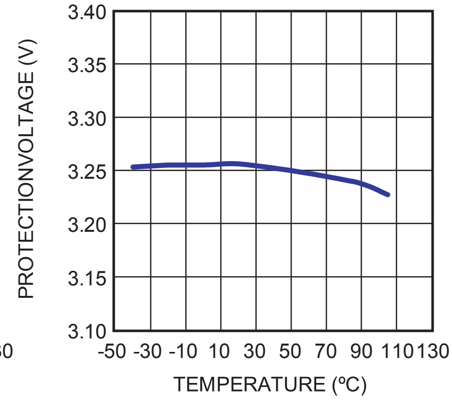
Short Circuit Protection Set Point vs. Temperature Chart



Internal Slope Compensation Ramp vs. Temperature Chart



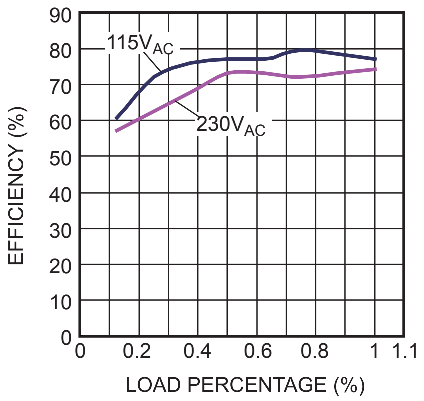
Protection Voltage vs. Temperature



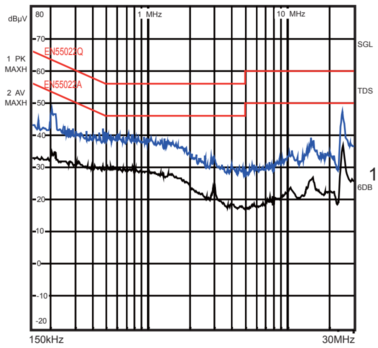
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=230VAC, V_{OUT1}=12V/0.8A, V_{OUT2}=8V/0.2A, V_{OUT3}=8V/0.05A, T_A=+25°C, unless otherwise noted.

Efficiency

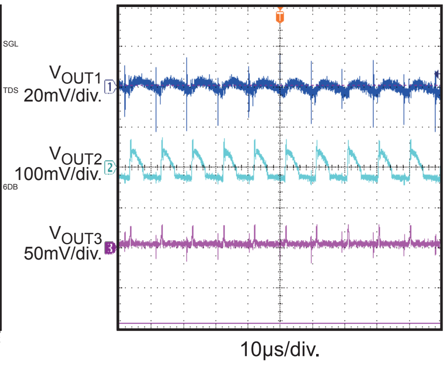


EMI



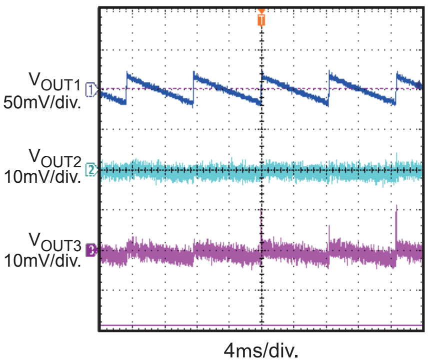
Output Voltage Ripple

Full Load



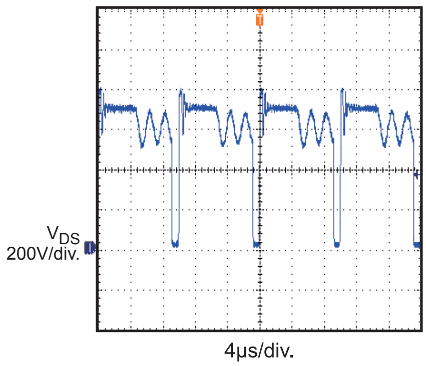
Output Voltage Ripple

No Load



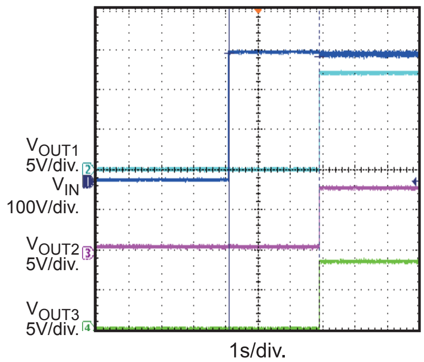
Stress

V_{IN} = 420V_{AC}, Full Load



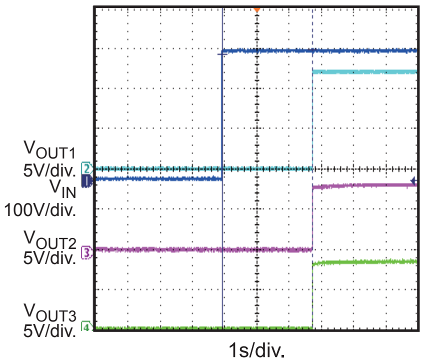
Input Power Startup

Full Load



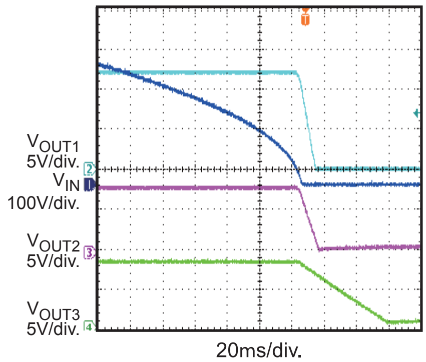
Input Power Startup

No Load



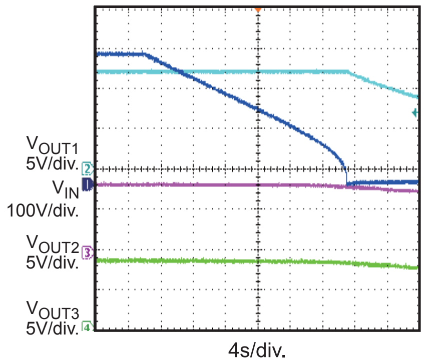
Input Power Shutdown

Full Load



Input Power Shutdown

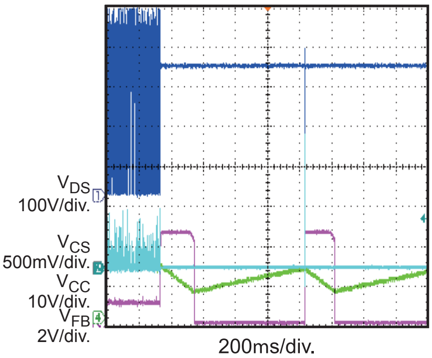
No Load



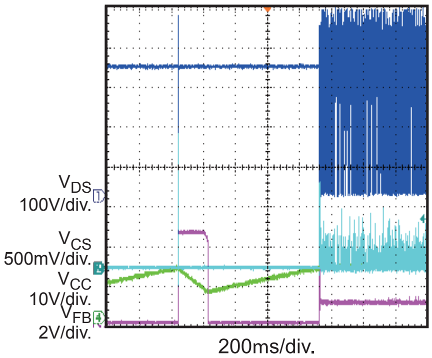
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=230VAC, V_{OUT1}=12V/0.8A, V_{OUT2}=8V/0.2A, V_{OUT3}=8V/0.05A, T_A=+25°C, unless otherwise noted.

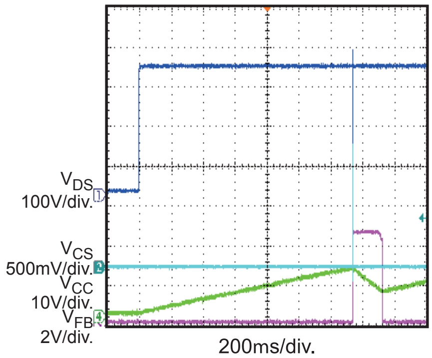
SCP Entry
Full Load



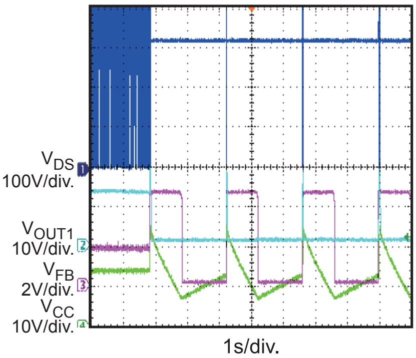
SCP Recovery
Full Load



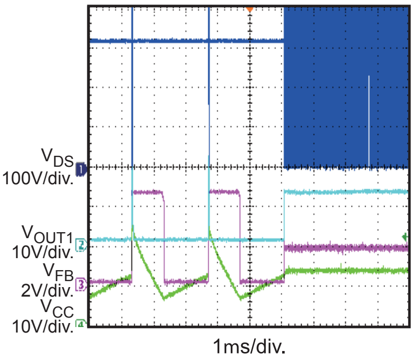
SCP Startup
Full Load



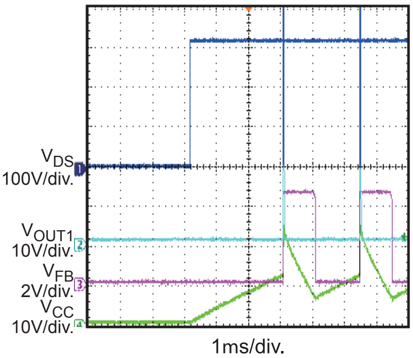
OVP Entry
Full Load



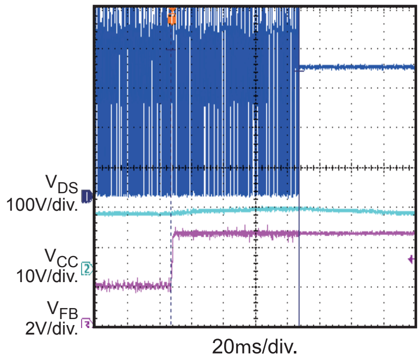
OVP Recovery
Full Load



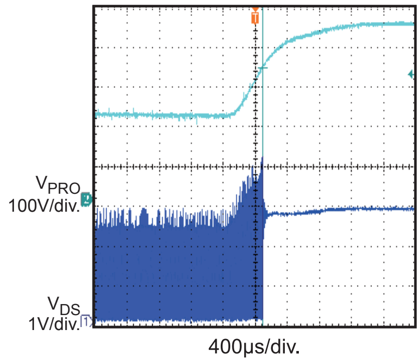
OVP Startup
Full Load



OCP Protection
Full Load



Pro Protection
V_{IN}=85V, 160V Protection,Full Load



BLOCK DIAGRAM

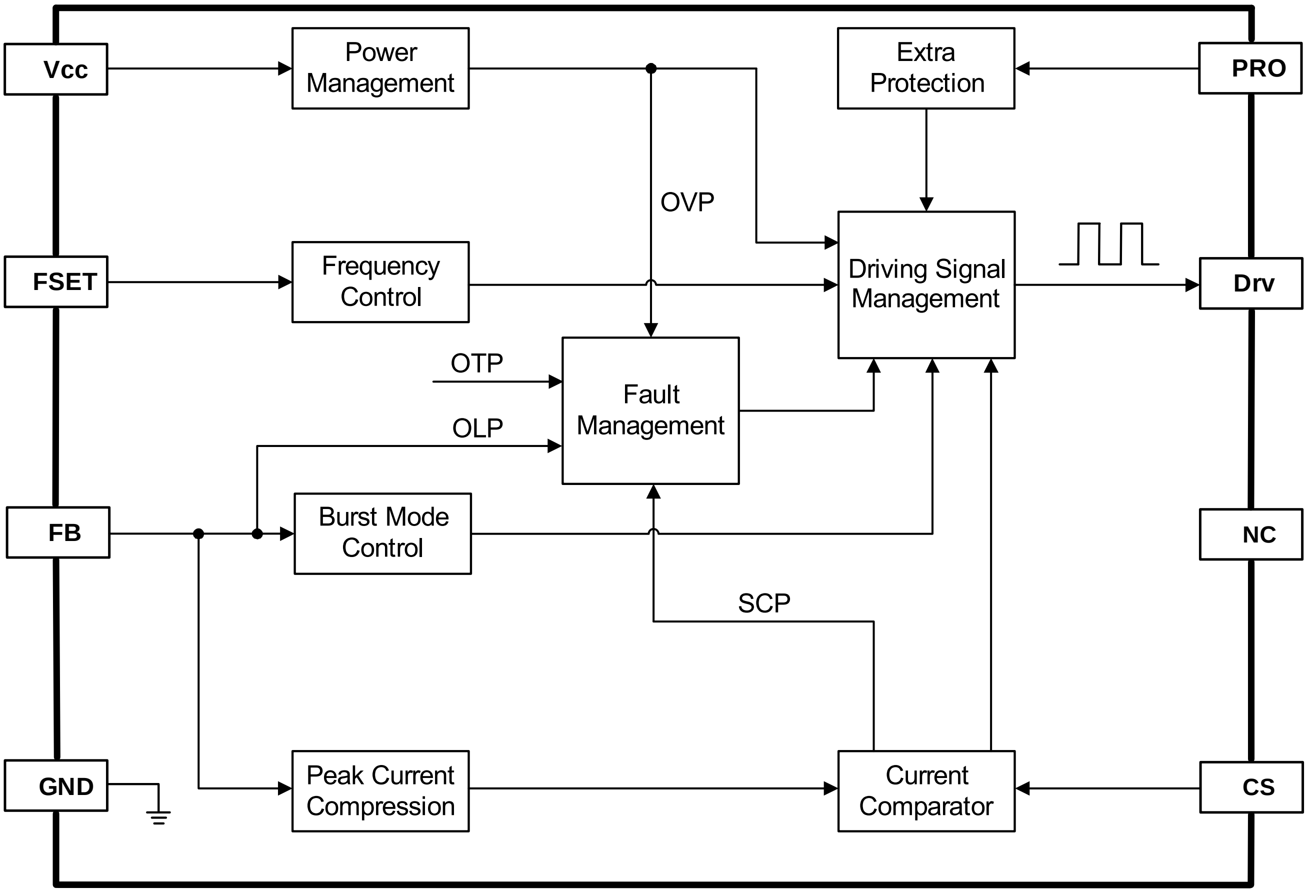


Figure 1: Functional Block Diagram

OPERATION

The HFC0310 incorporates all the necessary features to build a reliable switch-mode power supply. Its high level of integration requires very few external components. It has burst-mode operation to minimize the stand-by power consumption at light load. Protection features—such as auto-recovery for over-load protection (OLP), short-circuit protection (SCP), over-voltage protection (OVP), or thermal shutdown (TSD) for over-temperature protection (OTP)—contribute to a safer converter design without increasing circuit complexity.

PWM Operation

The HFC0310 is a fully integrated converter with adjustable-frequency peak-current-mode control PWM switching regulators. The output voltage is measured at FB through a resistive voltage divider, amplifier, and optocoupler. The voltage at the FB pin is compared to the internally measured switch current to control the output voltage. The integrated MOSFET turns on at the beginning of each clock cycle. The current in the inductor increases until it reaches the value set by the FB voltage, and then the integrated MOSFET turns off.

Start-Up and V_{CC} UVLO

During start-up, the IC consumption is I_{ST}, and the current supplied through the start-up resistor charges the V_{CC} capacitor.

The IC starts switching and the operation current increases when V_{CC} reaches V_{CCH}. At this point, the transformer's auxiliary winding powers the IC. When V_{CC} falls below V_{CCL}, the regulator stops switching and the current through the start up resistor charges the V_{CC} capacitor again.

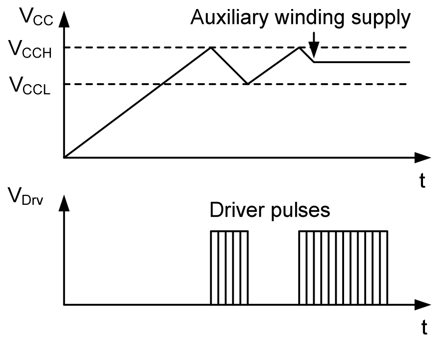


Figure 2: V_{CC} UVLO

The lower threshold of VCC under-voltage lock-out (UVLO) decreases from V_{CCL} to V_{CCR} when fault conditions occur, such as OLP, OVP, and OTP.

Soft-Start

To reduce stress on the primary MOSFET and the secondary diode during start-up and to smoothly establish the output voltage, the HFC0310 has an internal soft-start circuit that gradually increases the primary current sense threshold, which determines the MOSFET peak current during start-up. The pulse-width of the power switching device progressively increases to establish optimal operating conditions until the feedback control loop takes charge.

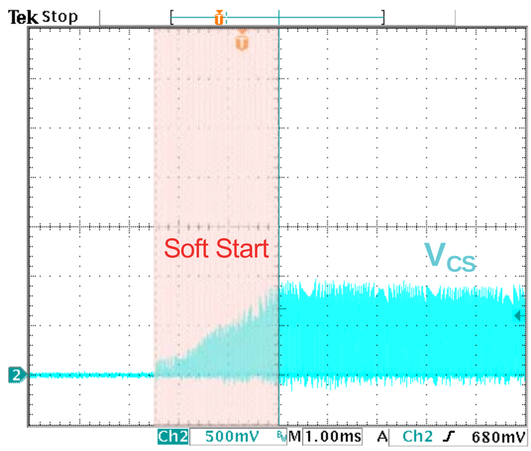


Figure 3: Soft Start

Switching Frequency

The capacitor between the FSET pin and GND sets the switching frequency of the HFC0310. Estimate the oscillator frequency as per the equation below:

$$f_S = \frac{1}{t_{DISCH} + C \times \frac{V_{FSETmax}}{I_{FSET}}} Hz$$

Over Voltage Protection

Monitoring the V_{CC} pin with about 20μs delay time allows the HFC0310 to enter OVP during an over-voltage condition; when V_{CC} goes above V_{OVP}. HFC0310 will resume operation after the fault disappears.

Over-Current Protection

The HFC0310 continuously monitors the FB pin. When FB pulls up to V_{OLP}, if after a 8192 switching cycle delay the fault signal is still present, the HFC0310 shuts down as soon as the power supply undergoes an overload. When the fault disappears, the power supply resumes operation.

Short-Circuit Protection

By monitoring the CS pin, the HFC0310 shuts down when the voltage rises higher than V_{SCP}, to indicate a short circuit. The HFC0310 enters a safe low-power mode that prevents any lethal thermal or stress damage. As soon as the fault disappears, the power supply resumes operation.

Thermal Shutdown

When the temperature of the IC exceeds thermal shutdown threshold, the OTP is activated and it will resume operation when junction temperature drops to thermal shutdown recovery point.

Burst Operation

To minimize stand-by power consumption, the HFC0310 implements burst mode at no load or light load. As the load decreases, the FB voltage decreases. The IC stops switching when the FB voltage drops below the lower threshold, V_{BRUL}. Then the output voltage drops at a rate dependent on the load. This causes the FB voltage to rise again due to the negative feedback control loop. Once the FB voltage exceeds the upper threshold, V_{BRUH}, the switching pulse resumes. The FB voltage then decreases and the whole process repeats. Burst-mode operation alternately enables and disables the switching pulse of the MOSFET. Hence switching loss at no load or light load conditions is greatly reduced.

Figure 4 shows the signals generated by burst-mode operation.

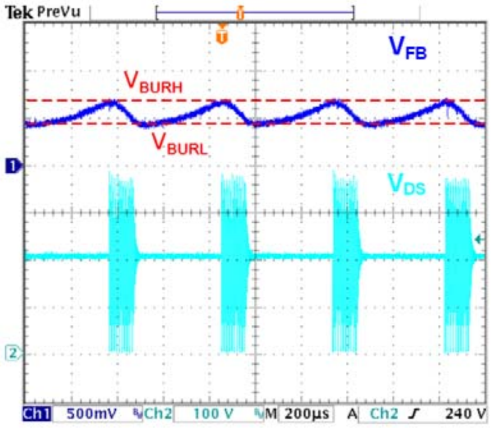


Figure 4: Burst-Mode Operation

PRO Pin

The PRO pin provides extra protection against abnormal conditions. Use the PRO pin for input OVP and/or other protections. If the PRO pin voltage exceeds V_{PRO}, the IC shuts down. As soon as the fault disappears, the power supply resumes operation.

Leading-Edge Blanking (LEB)

In normal operation, a resistor is placed between the MOSFET Source and Ground to senses the primary peak current. The FB voltage sets the turn-off threshold of the MOSFET, $V_{SENSE}=V_{FB}/ I_{DIV}$. HFC0310 turns off the MOSFET when the sensing resistor voltage rises to V_{SENSE}.

During start-up and over-load condition, the maximum primary peak current threshold is internally limited to Vcs to avoid excessive output power and lower the switch voltage stress.

In order to avoid turning off the MOSFET by mis-triggered spikes shortly after the switch turns on, the IC implements a leading-edge blanking period. During blanking time, any trigger signal on the source pin is blocked. Figure 5 shows the primary-current–sense waveform and the leading-edge blanking.

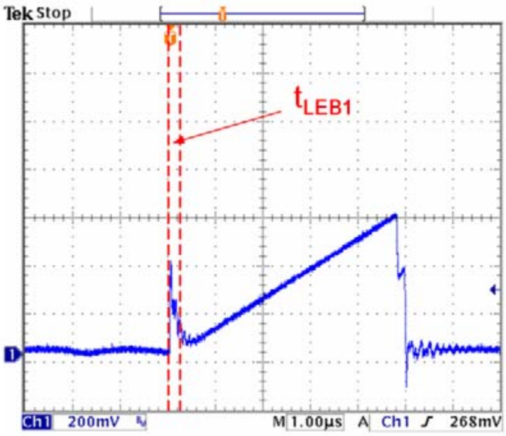


Figure 5: Leading-Edge Blanking

Design Example

The following is a design example using the application guidelines for the given specifications:

V_{IN}	85V to 420V
V_{OUT1}	12V
V_{OUT2}	8V
V_{OUT3}	8V
f_{SW}	100kHz

The detailed application schematic is shown in Figure 6. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more possible applications of this device, please refer to the related Evaluation Board datasheets.

TYPICAL APPLICATION CIRCUITS

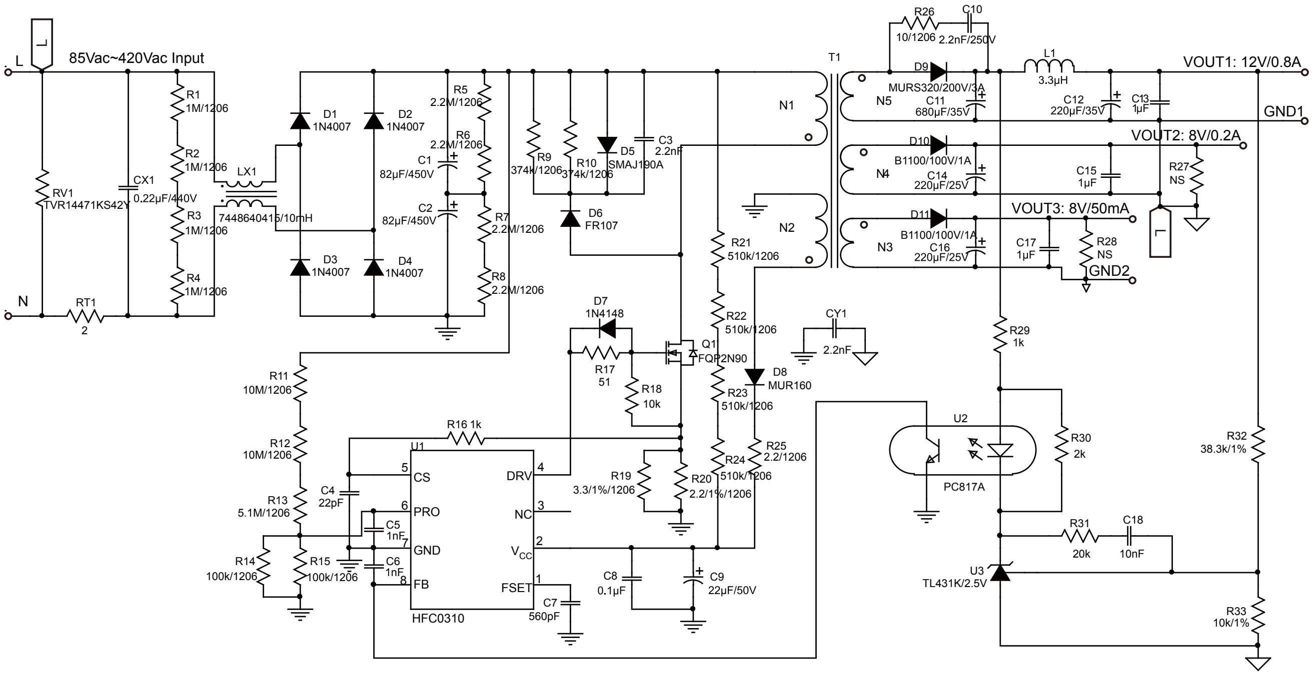
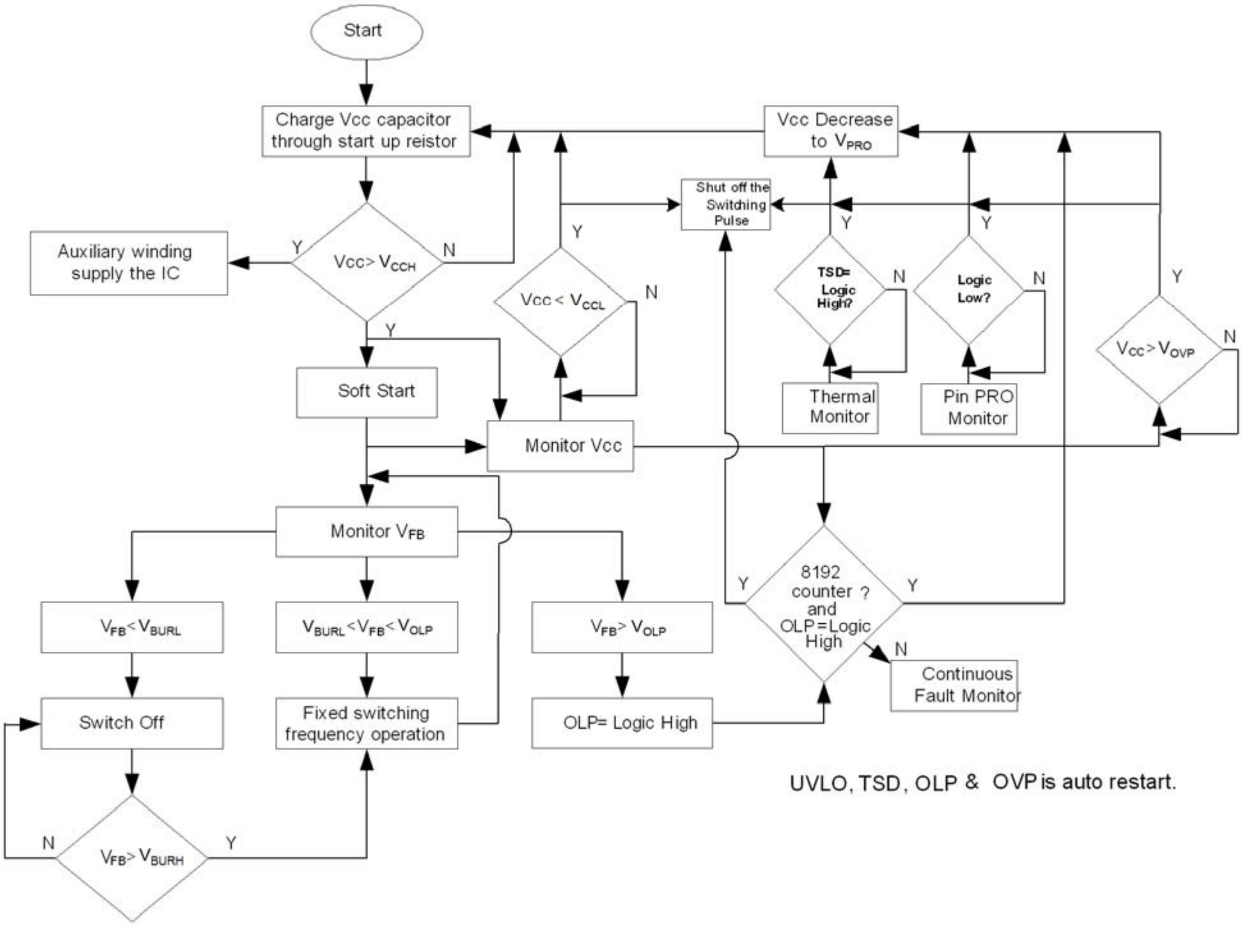


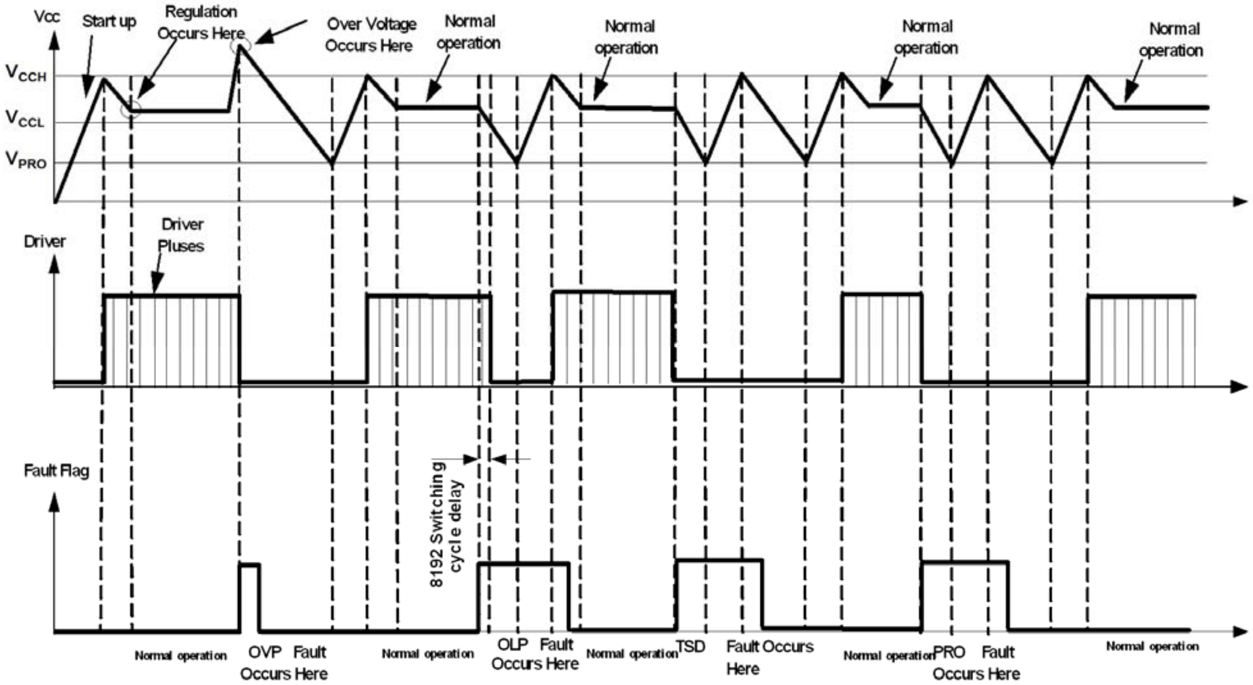
Figure 6: Typical Application Schematic

FLOW CHART



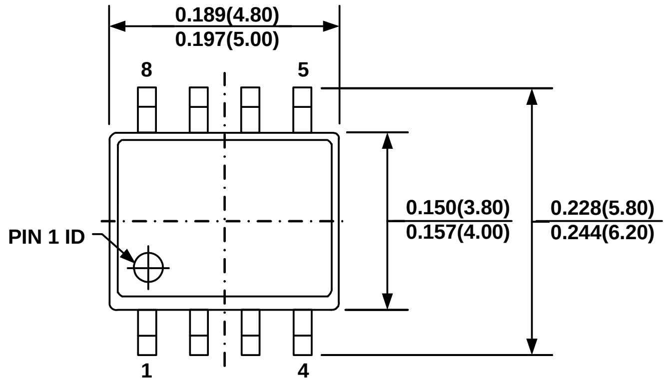
UVLO, TSD, OLP & OVP is auto restart.

SIGNAL EVOLUTION IN THE PRESENCE OF FAULTS

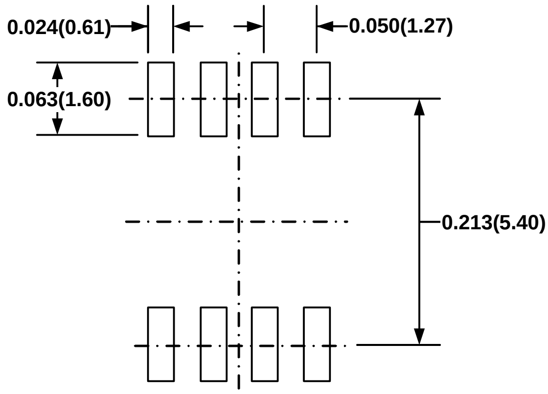


PACKAGE INFORMATION

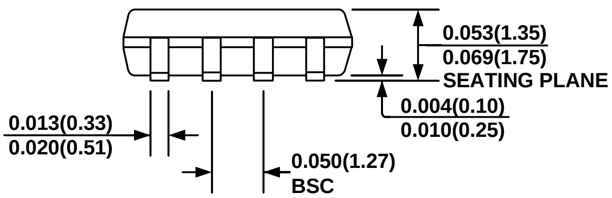
SOIC8



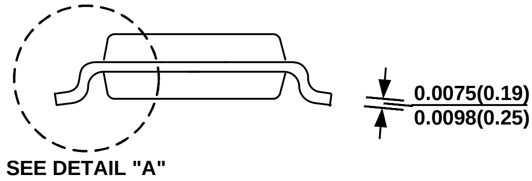
TOP VIEW



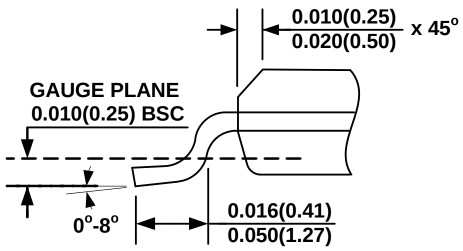
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMIN SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.