MP2151

5.5V, 1A, Synchronous Step-Down Converter with 25μA I_Q and Output Discharge in an Ultra-Small Package

DESCRIPTION

The MP2151 is a monolithic, step-down, switch-mode converter with built-in, internal power MOSFETs. The MP2151 achieves 1A of continuous output current from a 2.5V to 5.5V input voltage with excellent load and line regulation. The output voltage can be regulated as low as 0.6V.

The constant-on-time (COT) control scheme provides fast transient response and eases loop stabilization. Full protection features include cycle-by-cycle current limiting and thermal shutdown.

The MP2151 is ideal for a wide range of applications including high-performance DSPs, wireless power, portable and mobile devices, and other low-power systems.

The MP2151 requires a minimal number of readily available, standard, external components and is available in ultra-small SOT563 or UTQFN (1.2mmx1.6mm) packages.

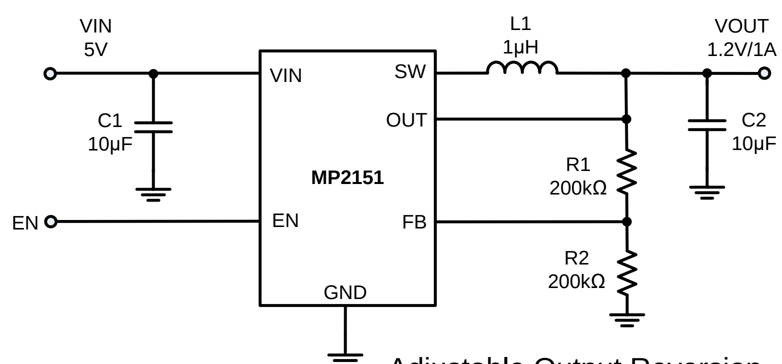
FEATURES

- Low I_Q: 25μA
- 1.1MHz Switching Frequency
- EN for Power Sequencing
- 1% FB Accuracy
- Wide 2.5V to 5.5V Operating Input Range
- Output Adjustable from 0.6V
- Up to 1A Output Current
- 80mΩ and 50mΩ Internal Power MOSFET Switches
- 100% Duty On
- Output Discharge
- Output Over-Voltage Protection (OVP)
- Short-Circuit Protection (SCP) with Hiccup Mode
- Power Good (PG) only for Fixed Output Version
- Available in a SOT563 or UTQFN (1.2mmx1.6mm) Package

APPLICATIONS

- Wireless/Networking Cards
- Portable Instruments
- Battery-Powered Devices
- Low-Voltage I/O System Power
- Multi-Function Printers

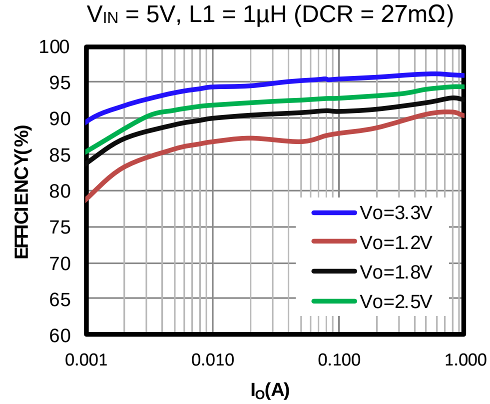
TYPICAL APPLICATION



Adjustable Output Reversion

Efficiency vs. Output Current

V_{IN} = 5V, L1 = 1μH (DCR = 27mΩ)



ORDERING INFORMATION

Part Number*	Package	Top Marking	V_{OUT} Range
MP2151GTF	SOT563	*See below*	*Adjustable*
MP2151GTF-12		*See below*	*Fixed 1.2V*
MP2151GTF-15		*See below*	*Fixed 1.5V*
MP2151GTF-18		*See below*	*Fixed 1.8V*
MP2151GTF-25		*See below*	*Fixed 2.5V*
MP2151GTF-33		*See below*	*Fixed 3.3V*

* For Tape & Reel, add suffix –Z (e.g. MP2151GTF–Z).

TOP MARKING (MP2151GTF)

AZDY

LLL

AZD: Product code of MP2151GTF
Y: Year code
LLL: Lot number

TOP MARKING (MP2151GTF-12)

BBDY

LLL

BBD: Product code of MP2151GTF-12
Y: Year code
LLL: Lot number

TOP MARKING (MP2151GTF-15)

BBEY

LLL

BBE: Product code of MP2151GTF-15
Y: Year code
LLL: Lot number

TOP MARKING (MP2151GTF-18)

BBFY

LLL

BBF: product code of MP2151GTF-18
Y: Year code
LLL: Lot number

TOP MARKING (MP2151GTF-25)

BBGY

LLL

BBG: Product code of MP2151GTF-25
Y: Year code
LLL: Lot number

TOP MARKING (MP2151GTF-33)

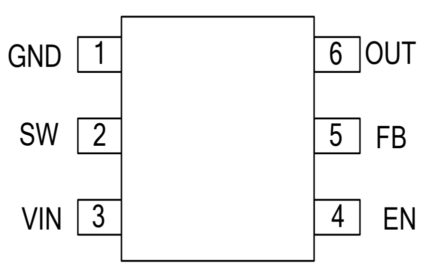
BBHY

LLL

BBH: Product code of MP2151GTF-33
Y: Year code
LLL: Lot number

PACKAGE REFERENCE

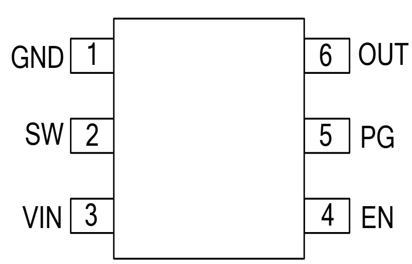
TOP VIEW



SOT563

Adjustable Version
MP2151GTF

TOP VIEW



SOT563
Fixed Vo Version
MP2151GTF-12, MP2151GTF-15, MP2151GTF-18, MP2151GTF-25, MP2151GTF-33

ORDERING INFORMATION

Part Number*	Package	Top Marking	V_{OUT} Range
MP2151GQFU	UTQFN (1.2mmx1.6mm)	*See below*	Adjustable
MP2151GQFU-12		*See below*	*Fixed 1.2V*
MP2151GQFU-15		*See below*	*Fixed 1.5V*
MP2151GQFU-18		*See below*	*Fixed 1.8V*
MP2151GQFU-25		*See below*	*Fixed 2.5V*
MP2151GQFU-33		*See below*	*Fixed 3.3V*

* For Tape & Reel, add suffix –Z (e.g. MP2151GQFU–Z).

TOP MARKING (MP2151GQFU)

FX
LL

FX: Product code of MP2151GQFU
LL: Lot number

TOP MARKING (MP2151GQFU-12)

GD
LL

GD: Product code of MP2151GQFU-12
LL: Lot number

TOP MARKING (MP2151GQFU-15)

GE
LL

GE: Product code of MP2151GQFU-15
LL: Lot number

TOP MARKING (MP2151GQFU-18)

GF
LL

GF: Product code of MP2151GQFU-18
LL: Lot number

TOP MARKING (MP2151GQFU-25)

GG
LL

GG: Product code of MP2151GQFU-25
LL: Lot number

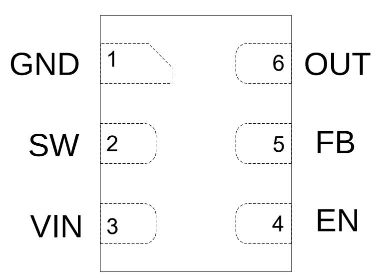
TOP MARKING (MP2151GQFU-33)

GH
LL

GH: Product code of MP2151GQFU-33
LL: Lot number

PACKAGE REFERENCE

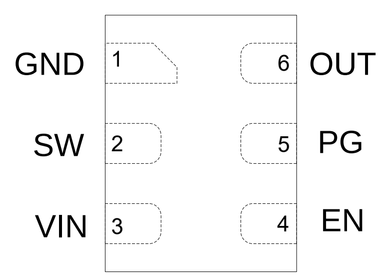
TOP VIEW



UTQFN (1.2mmx1.6mm)

MP2151GQFU-Z

TOP VIEW



UTQFN (1.2mmx1.6mm)
MP2151GQFU-12, MP2151GQFU-15
MP2151GQFU-18, MP2151GQFU-25
MP2151GQFU-33

PIN FUNCTIONS

Pin #	Name SOT563 and UTQFN Adj version	Name SOT563 and UTQFN Fixed version	Description
1	GND	GND	**Power ground.**
2	SW	SW	**Output switching node.** SW is the drain of the internal, high-side, P-channel MOSFET. Connect an inductor to SW to complete the converter.
3	VIN	VIN	**Supply voltage.** The MP2151 operates from a +2.5V to +5.5V unregulated input range. Decouple the capacitor to prevent large voltage spikes from appearing at the input.
4	EN	EN	**On/off control.**
5	FB	-	**Feedback.** An external resistor divider from the output to GND tapped to FB sets the output voltage.
5	-	PG	**Power good indicator.** The output of PG is an open drain with an external pull-up resistor to VIN.
6	OUT	OUT	**Output sense.** OUT is the voltage power rail and input sense pin for the output voltage. Connect the load to OUT. Use an output capacitor to decrease the output voltage ripple.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 6.5V
V_{SW} .... -0.3V (-5V for <10ns) to 6.5V (10V for <10ns)
All other pins ....-0.3V to 6.5V
Junction temperature ....150°C
Lead temperature ....260°C
Continuous power dissipation (T_A = +25°C)
SOT563 .... 1.5W (2)(4)
UTQFN .... 2W (2)(5)
Storage temperature .... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ....2.5V to 5.5V
Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}	
SOT563			
EV2151-TF-00A (4)	80	50	°C/W
JESD51-7 (6)	130	60	°C/W
UTQFN (1.2mmx1.6mm)			
EV2151-QFU-00A (5)	65	30	°C/W
JESD51-7 (6)	173	127	°C/W

NOTES:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV2151-TF-00A, 2-layer PCB, 63mmx63mm.
5) Measured on EV2151-QFU-00A, 2-layer PCB, 63mmx63mm.
6) Measured on JESD51-7, 4-layer PCB.
The value of θ_{JA} given in this table is valid for comparison with other packages only and cannot be used for design purposes. These values are calculated in accordance with JESD51-7 and are simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +125°C(6), typical value is tested at T_J = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} range			2.5		5.5	V
Under-voltage lockout threshold rising				2.3	2.45	V
Under-voltage lockout threshold hysteresis				200		mV
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C	591	600	609	
OUT voltage (MP2151XX-12)	V_O	T_J = 25°C	1188	1200	1212	mV
		T_J = -40°C to +125°C	1182	1200	1218	mV
OUT voltage (MP2151XX-15)	V_O	T_J = 25°C	1485	1500	1515	mV
		T_J = -40°C to +125°C	1478	1500	1522	mV
OUT voltage (MP2151XX-18)	V_O	T_J = 25°C	1782	1800	1818	mV
		T_J = -40°C to +125°C	1873	1800	1827	mV
OUT voltage (MP2151XX-25)	V_O	T_J = 25°C	2475	2500	2525	mV
		T_J = -40°C to +125°C	2463	2500	2537	mV
OUT voltage (MP2151XX-33)	V_O	T_J = 25°C	3267	3300	3333	mV
		T_J = -40°C to +125°C	3251	3300	3349	mV
Feedback current	I_{FB}	V_{FB} = 0.63V		50	100	nA
P-FET switch on resistance	R_{DSON_P}	V_{IN} = 5V		80		mΩ
N-FET switch on resistance	R_{DSON_N}	V_{IN} = 5V		50		mΩ
Switch leakage		V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V and 6V, T_J = +25°C		0	1	μA
P-FET peak current limit			1.8			A
ZCD				50		mA
On time	T_{ON}	V_{IN} = 5V, V_{OUT} = 1.2V	180	220	260	ns
		V_{IN} = 3.6V, V_{OUT} = 1.2V	240	300	360	
Switching frequency	f_s	V_{OUT} = 1.2V		1100		kHz
Minimum off time	$T_{MIN-OFF}$			100		ns
Minimum on time (6)	T_{MIN-ON}			60		ns
Soft-start time	T_{SS-ON}	V_{OUT} rise from 10% to 90%		0.5		ms
Maximum duty cycle			100			%
Power good rising threshold UV		Fixed Vo version, V_{OUT} rising edge		90		%
Power good falling threshold UV		Fixed Vo version, V_{OUT} falling edge		85		%
Power good rising threshold OV		Fixed Vo version, V_{OUT} rising edge		115		%
Power good falling threshold OV		Fixed Vo version, V_{OUT} falling edge		105		%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +125°C(6), typical value is tested at T_J = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

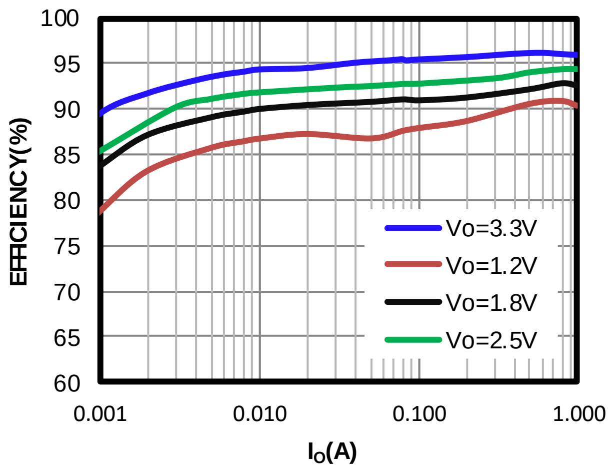
Parameter	Symbol	Condition	Min	Typ	Max	Units
Power good delay	PG_D	Fixed Vo version, PG rising/falling edge		150		μs
Power good sink current capability	V_{PG-L}	Fixed Vo version, sink 1mA			0.4	V
Power good logic high voltage	V_{PG-H}	Fixed Vo version, V_{IN} =5V, V_{FB} = 0.6V	4.9			V
EN turn on delay		EN on to SW active		150		us
EN input logic low voltage					0.4	V
EN input logic high voltage			1.2			V
Output discharge resistor	R_{DIS}	V_{EN} = 0V, V_{OUT} = 1.2V		200		Ω
EN input current		V_{EN} = 2V		1.2		μA
		V_{EN} = 0V		0		μA
Supply current (shutdown)		V_{EN} = 0V, T_J = +25°C		0	1	μA
Supply current (quiescent) (MP2151XX, adjustable)		V_{EN} = 2V, V_{FB} = 0.63V, V_{IN} = 5V, T_J = +25°C		25	30	μA
Supply current (quiescent) (MP2151XX-XX, fixed Vo)		V_{EN} = 2V, no switching, V_{IN} = 5V, T_J = +25°C		30	35	μA
Output over-voltage threshold	V_{OVP}		110%	115%	120%	V_{FB}
Vo OVP hysteresis	V_{OVP_HYS}			10%		V_{FB}
OVP delay				12		us
Low-side current		Current flow from SW to GND		1.5		A
Absolute VIN OVP		After Vo OVP enable		6.1		V
Absolute VIN OVP hysteresis				400		mV
Thermal shutdown (7)				160		°C
Thermal hysteresis (7)				30		°C

NOTES:
7) Guaranteed by over-temperature correlation, not tested in production.
8) Guaranteed by engineering sample characterization.

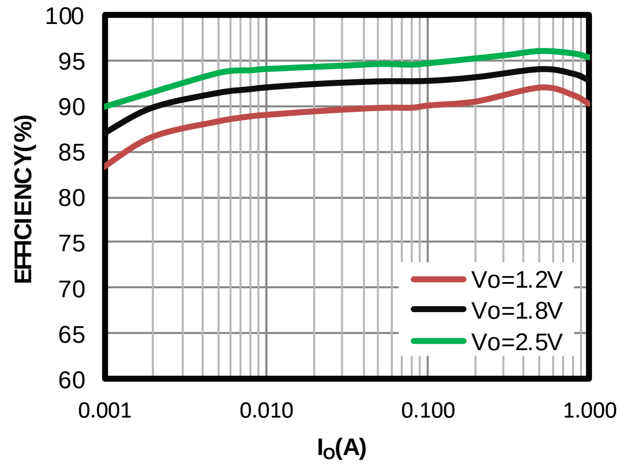
TYPICAL CHARACTERISTICS

V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = +25°C, unless otherwise noted.

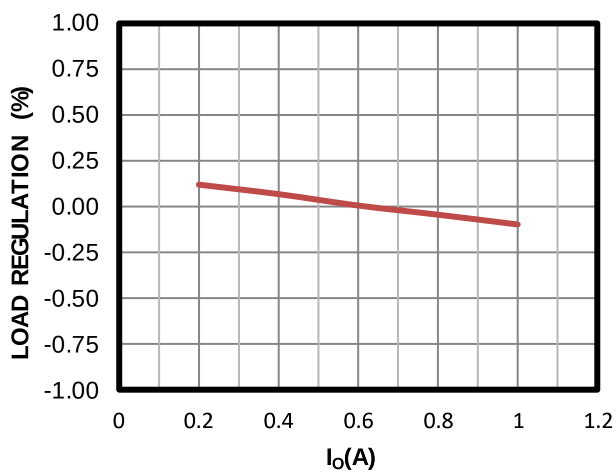
Efficiency vs. Io
V_{IN} = 5V



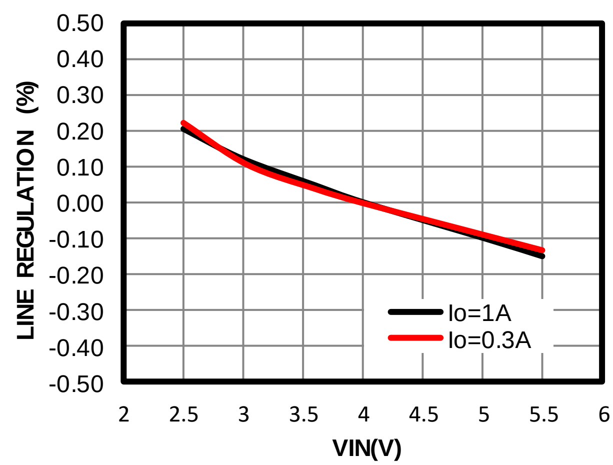
Efficiency vs. Io
V_{IN} = 3.6V



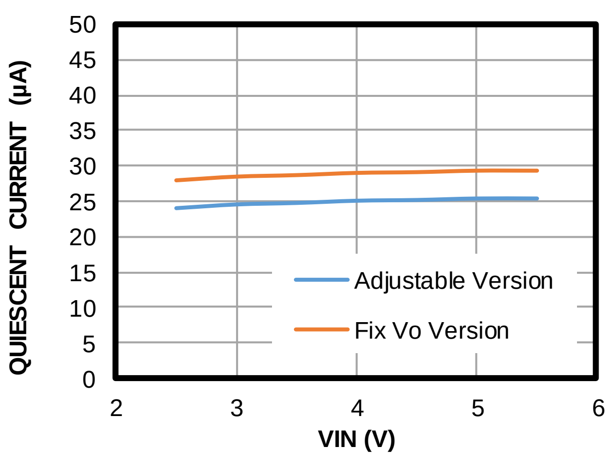
Load Regulation



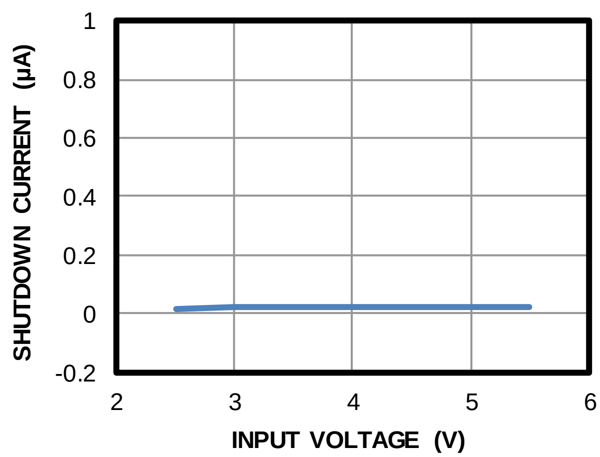
Line Regulation



Quiescent Current vs. V_{IN}



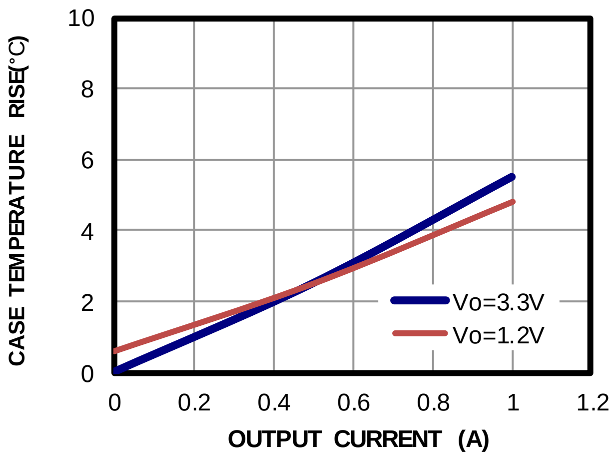
Shutdown Current vs. Input Voltage
V_{EN} = 0V



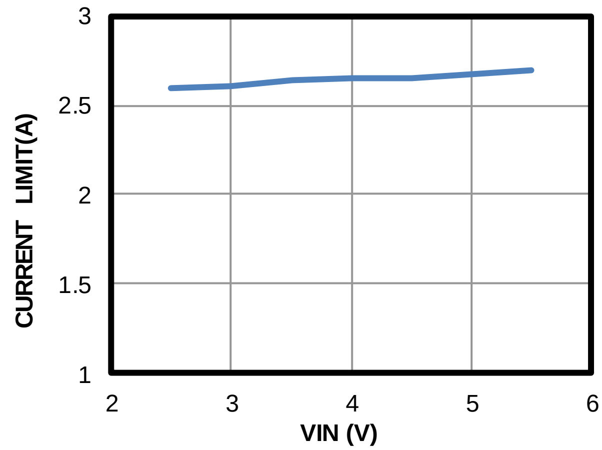
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = +25°C, unless otherwise noted.

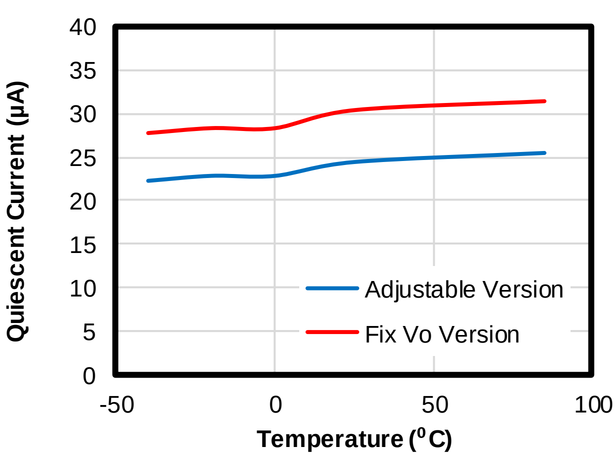
Case Temperature Rising vs. Output Current



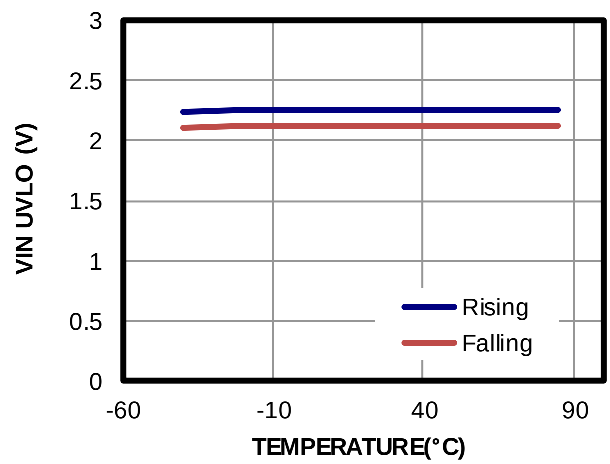
Peak Current Limit vs. V_{IN}



Quiescent Current vs. Temperature

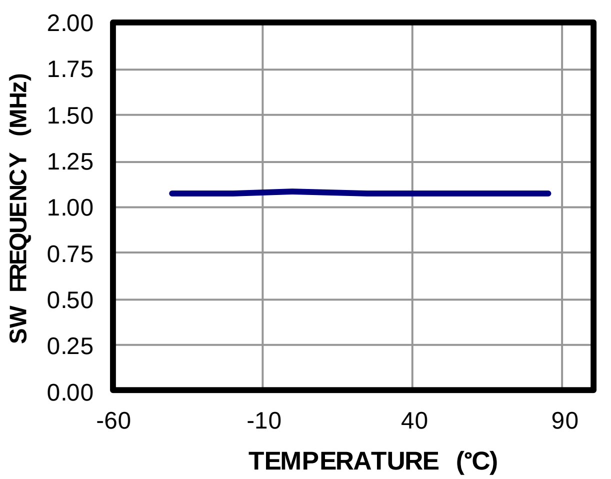


V_{IN} UVLO Rising Threshold vs. Temperature



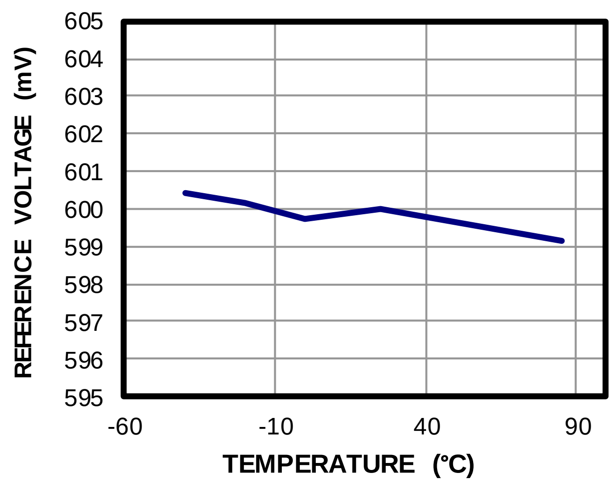
Switch Frequency vs Temperature

V_{IN} = 3.6V, V_{OUT} = 1.2V, I_{OUT} = 500mA



Reference Voltage vs. Temperature

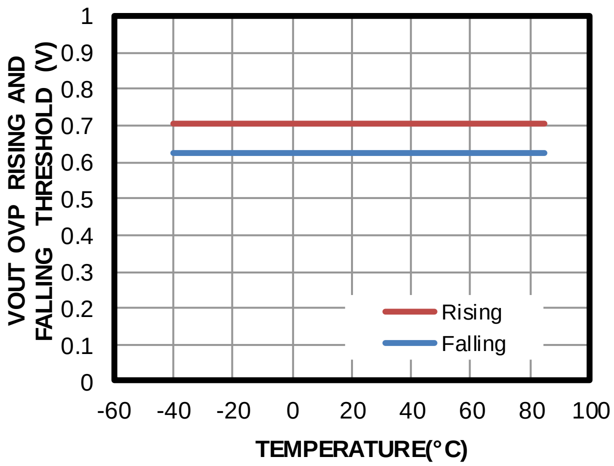
V_{IN} = 3.6V



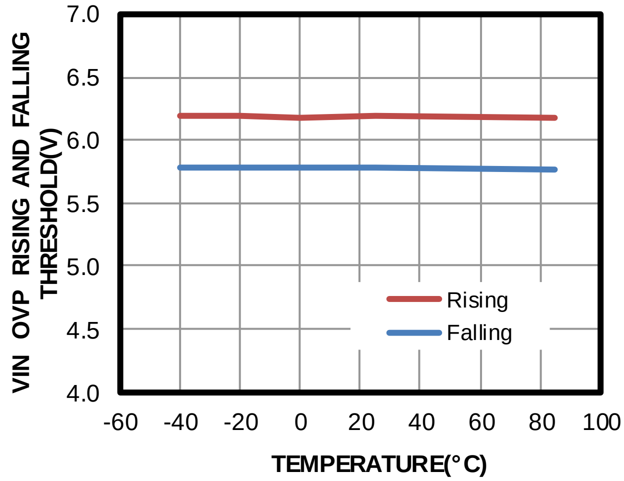
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = +25°C, unless otherwise noted.

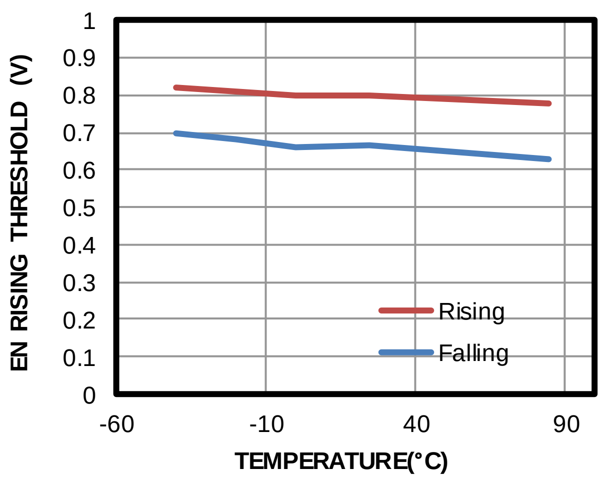
V_{OUT} OVP Rising and Falling Threshold vs. Temperature



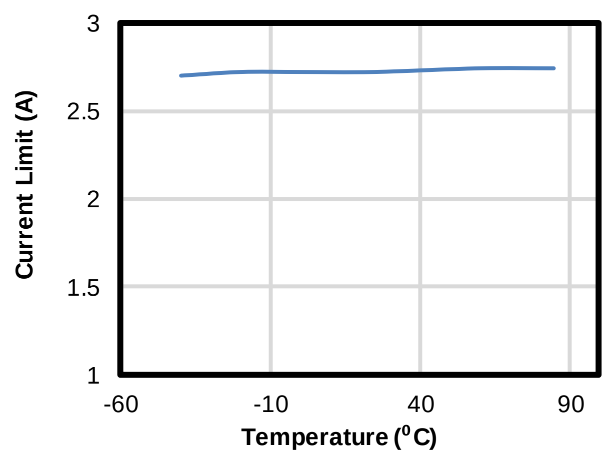
V_{IN} OVP Rising and Falling Threshold vs. Temperature



EN Rising and Falling Threshold vs. Temperature



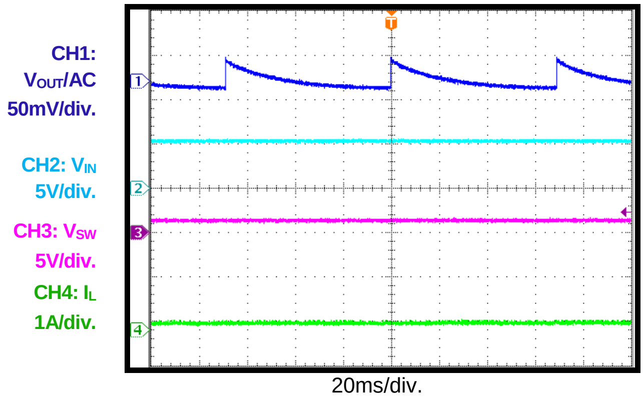
Peak Current Limit vs. Temperature



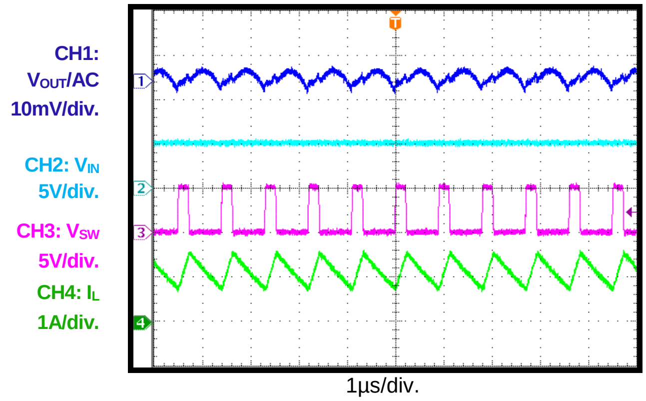
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = +25°C, unless otherwise noted.

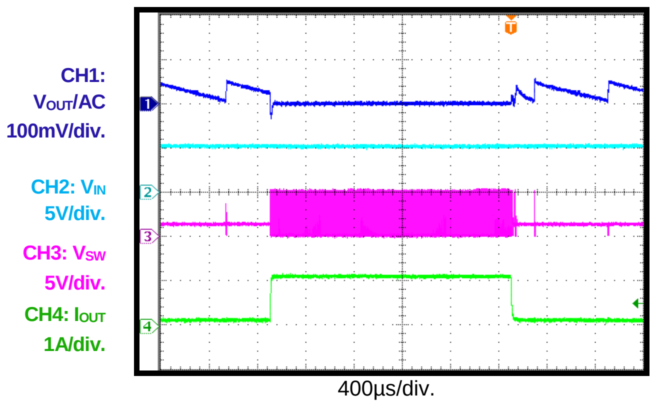
Steady State
I_{OUT} = 0A



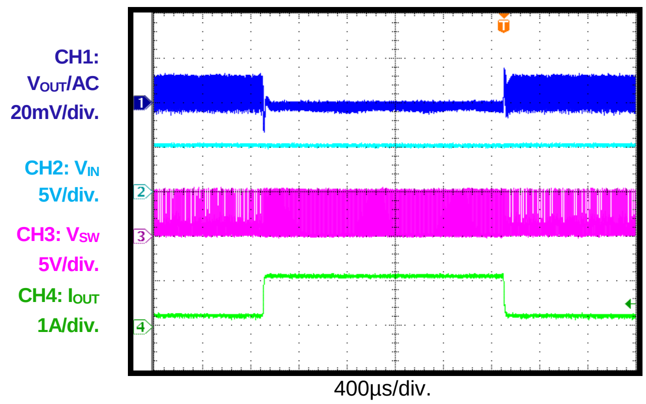
Steady State
I_{OUT} = 1A



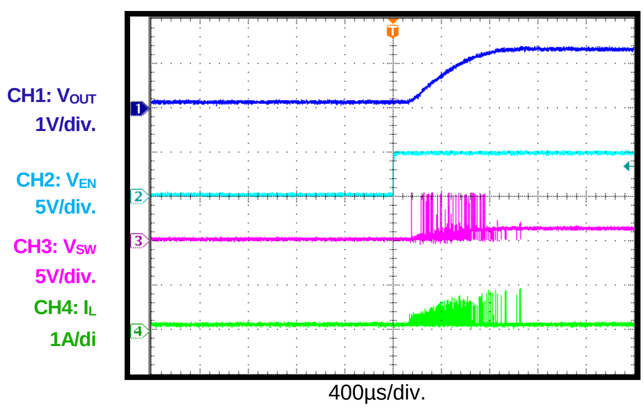
Load Transient Response
I_{OUT} = 0 - 1A



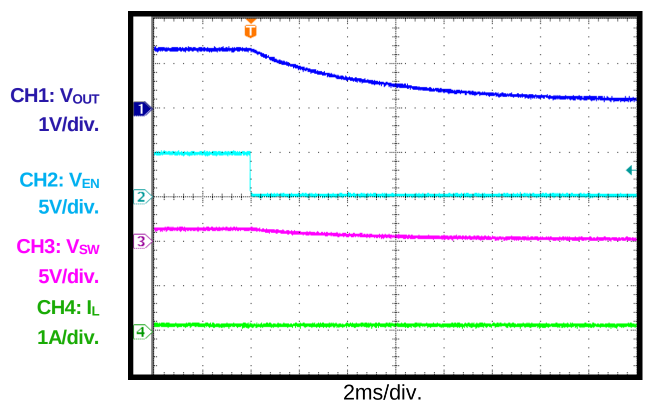
Load Transient Response
I_{OUT} = 0.1 - 1A



EN Power-Up
I_{OUT} = 0A



EN Shutdown
I_{OUT} = 0A

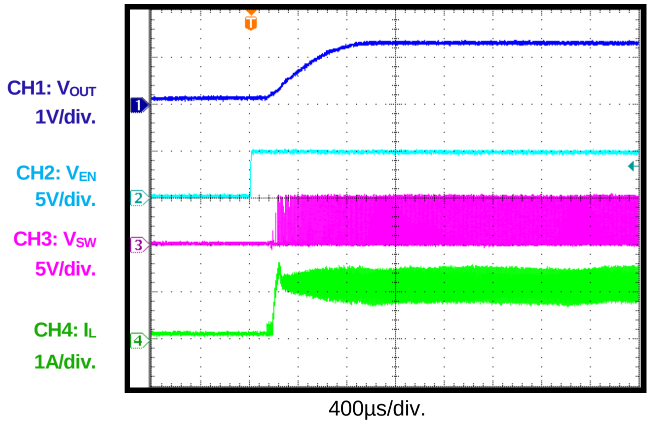


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1μH, C_{OUT} = 22μF, T_A = +25°C, unless otherwise noted.

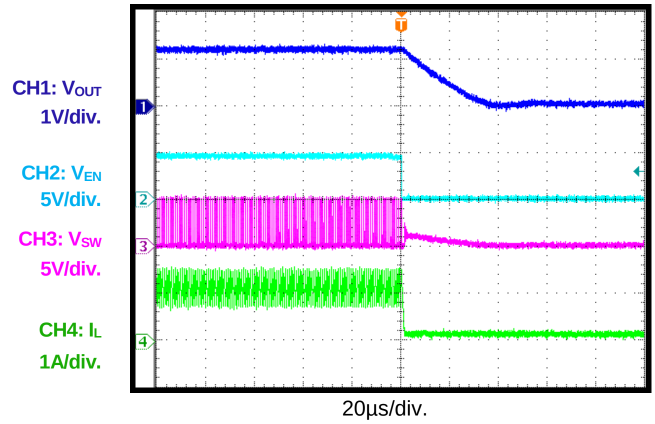
EN Power-Up

I_{OUT} = 1A



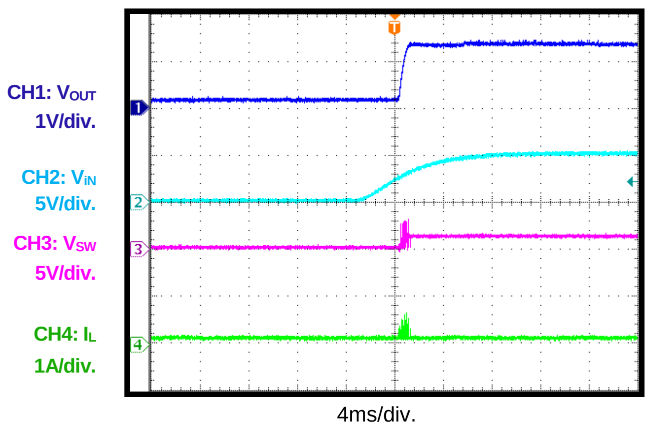
EN Shutdown

I_{OUT} = 1A



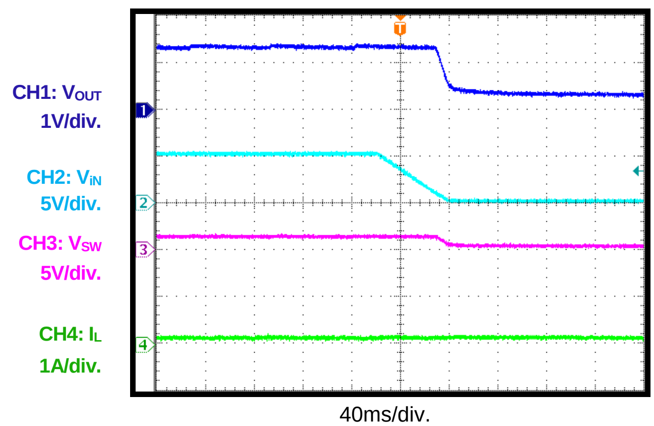
V_{IN} Power-Up

I_{OUT} = 0A



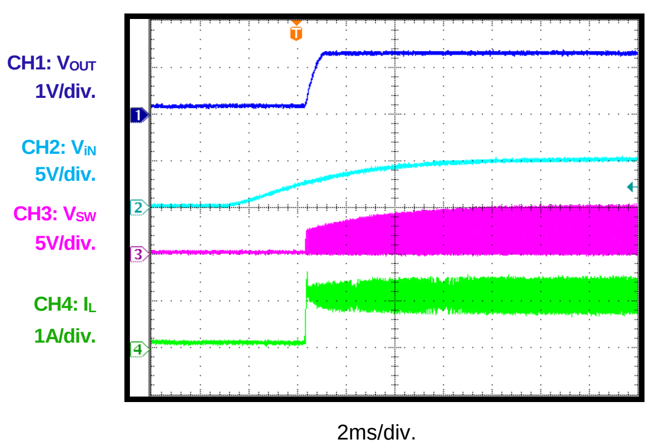
V_{IN} Shutdown

I_{OUT} = 0A



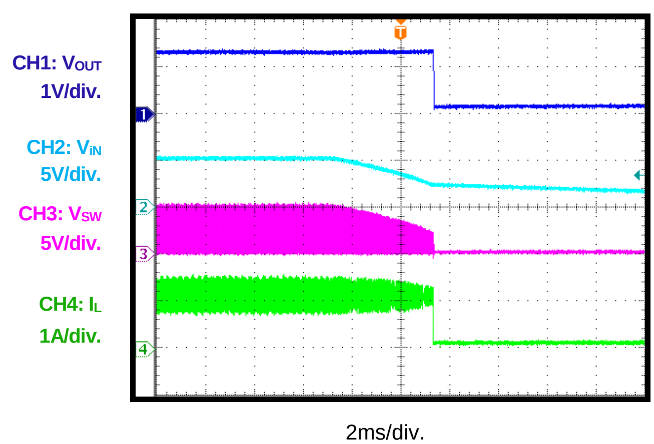
V_{IN} Power-Up

I_{OUT} = 1A



V_{IN} Shutdown

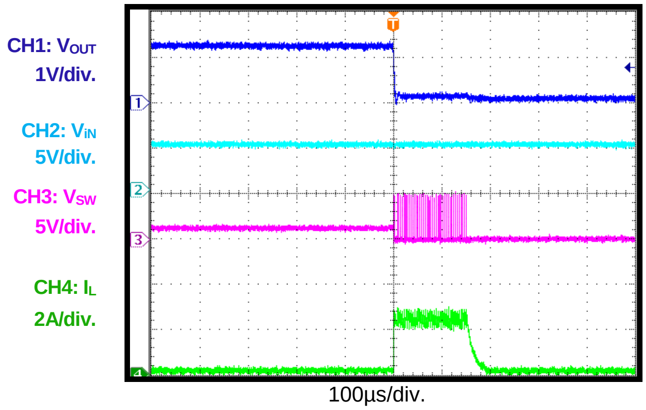
I_{OUT} = 1A



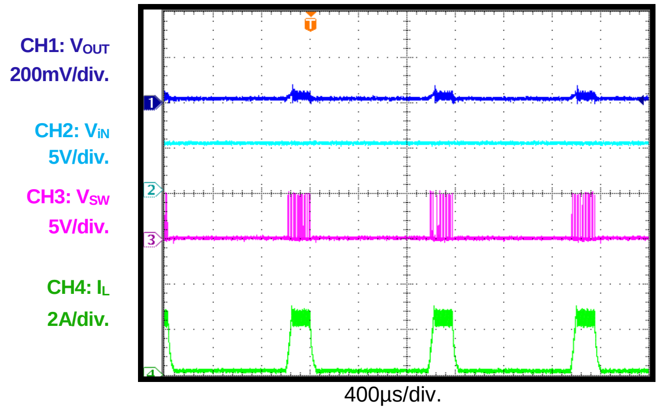
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = +25°C, unless otherwise noted.

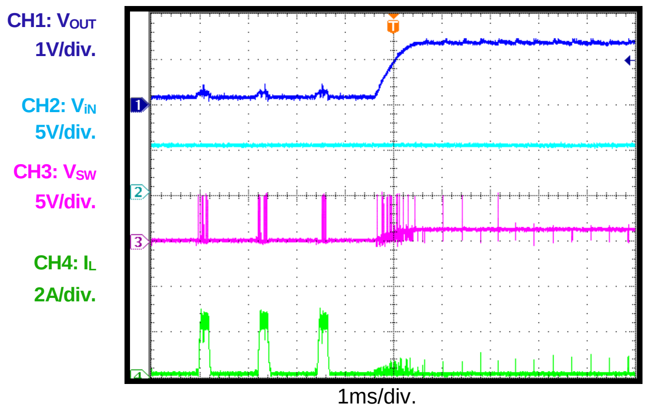
Short-Circuit Entry



Short-Circuit State



Short-Circuit Recovery



BLOCK DIAGRAM

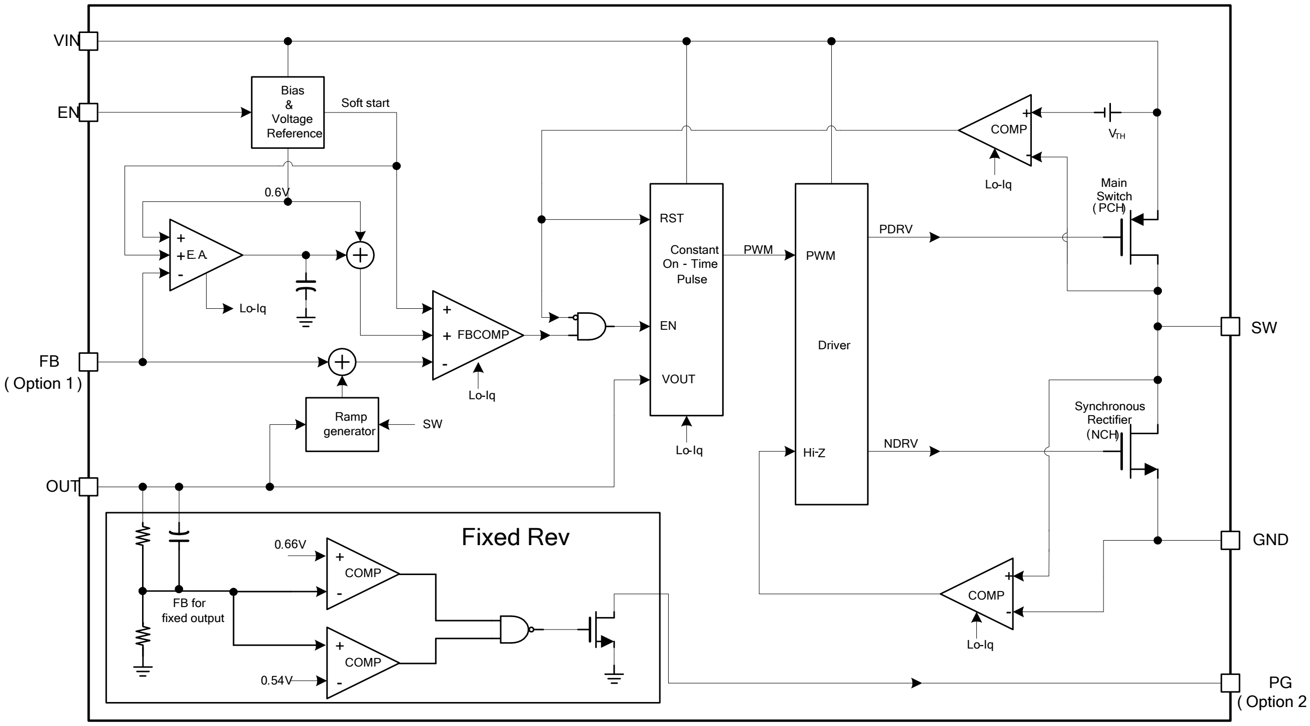


Figure 1: Functional Block Diagram

Option 1: FB is only for MP2151XXX.

Option 2: PG is only for MP2151XXX-XX.

OPERATION

The MP2151 uses constant-on-time (COT) control with input voltage feed-forward to stabilize the switching frequency over the entire input range. The MP2151 achieves 1A of continuous output current from a 2.5V to 5.5V input voltage with excellent load and line regulation. The output voltage can be regulated as low as 0.6V.

Constant-On-Time (COT) Control

Compare to fixed-frequency pulse-width modulation (PWM) control, COT control offers a simpler control loop and faster transient response. By using input voltage feed-forward, the MP2151 maintains a fairly constant switching frequency across the input and output voltage ranges. The switching pulse on time can be estimated with Equation (1):

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.91us \qquad (1)$$

To prevent inductor current runaway during the load transient, the MP2151 has a fixed minimum off time of 100ns.

Sleep Mode Operation

The MP2151 features sleep mode to achieve high efficiency at extremely light-load conditions. In sleep mode, most of the circuit blocks are turned off, except for the error amplifier and PWM comparator, so the operation current is reduced to a minimal value (see Figure 2).

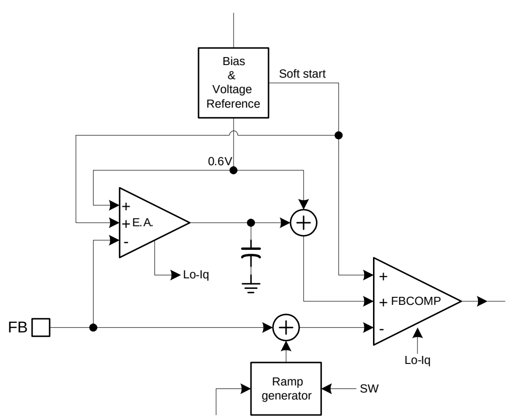


Figure 2: Operation Blocks in Sleep Mode

When the load lightens, the ripple of the output voltage increases and drives the error amplifier output (EAO) lower. When the EAO reaches an internal low threshold, it is clamped at that level, and the MP2151 enters sleep mode. During sleep mode, the valley of the FB voltage is regulated to the internal reference voltage. Therefore, the average output voltage is slightly higher than the output voltage at discontinuous conduction mode (DCM) or continuous conduction mode (CCM). The on time pulse in sleep mode is slightly larger than that in DCM or CCM. Figure 3 shows the average FB voltage in relation to the internal reference in sleep mode.

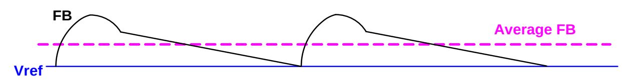


Figure 3: FB Average Voltage in Sleep Mode

When the MP2151 is in sleep mode, the average output voltage is higher than the internal reference voltage. The EAO is kept low and clamped in sleep mode. When the load increases, the PWM switching period decreases to keep the output voltage regulated. The output voltage ripple is decreased relatively. Once the EAO is higher than the internal low threshold, the MP2151 exits sleep mode and enters either DCM or CCM depending on the load. In DCM or CCM, the error amplifier regulates the average output voltage to the internal reference (see Figure 4).

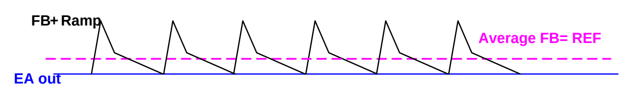


Figure 4: DCM Control

There is always a load hysteresis when entering and exiting sleep mode due to the error amplifier clamping response time.

AAM Operation at Light-Load Operation

The MP2151 uses advanced asynchronous modulation (AAM) power-save mode together with a zero-current cross detection (ZCD) circuit in light-load operation.

The simplified AAM control theory is shown in Figure 5. The AAM current (I_{AAM}) is set internally. The SW on pulse time is determined by the on-time generator and AAM comparator. In light-load condition, the SW on pulse time is the longer pulse. If the AAM comparator pulse is longer than the on-time generator, the operation mode is as shown in Figure 6.

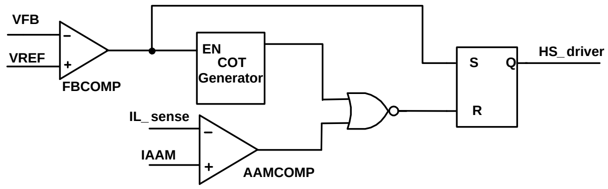
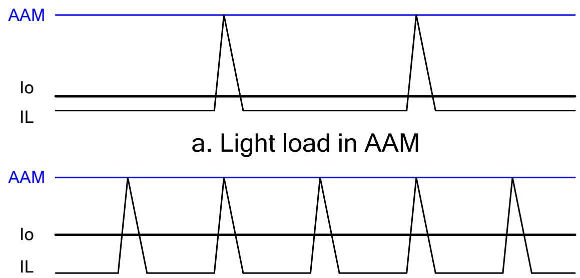


Figure 5: Simplified AAM Control Logic

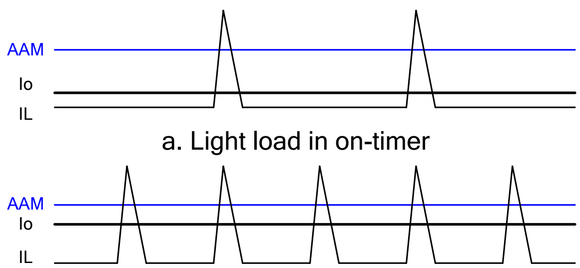


a. Light load in AAM

b. Increased load in AAM

Figure 6: AAM Comparator Control T_{ON}

If the AAM comparator pulse is shorter than the on-time generator, the operation mode is as shown in Figure 7.



a. Light load in on-timer

b. Increased load in on-timer

Figure 7: On-Time Control T_{ON}

Figure 8 shows the AAM threshold decreasing as T_{ON} increases gradually. In CCM, Io must be more than half of the AAM threshold at least. Generally, the AAM threshold is lower than the inductor current in a normal duty cycle.

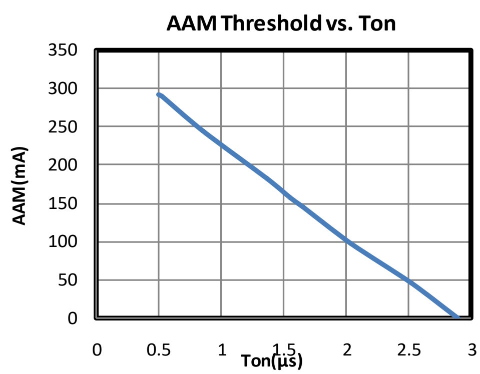


Figure 8: AAM Threshold Decreasing as T_{ON} Increases

The MP2151 ZCD determines when the inductor current starts reversing. When the inductor current reaches the ZCD threshold, the low-side switch is turned off.

AAM mode together with the ZCD circuit makes the MP2151 always operate in DCM in light-load conditions, even if Vo is close to V_{IN}.

Enable (EN)

When the input voltage is greater than the under-voltage lockout (UVLO) threshold (typically 2.3V), the MP2151 can be enabled by pulling EN above 1.2V. Leave EN floating or pull EN down to ground to disable the MP2151. There is an internal 1MΩ resistor from EN to ground.

When the MP2151 is disabled, it goes into output discharge mode automatically. The internal discharge MOSFET provides a resistive discharge path for the output capacitor.

Soft Start

The MP2151 has a built-in soft start that ramps up the output voltage at a controlled slew rate to avoid overshooting during start-up. The soft-start time is about 0.5ms, typically.

Current Limit

The MP2151 has a minimum 1.8A high-side switch current limit, typically. When the high-side switch reaches its current limit, the MP2151 is in hiccup mode until the current drops. This prevents the inductor current from continuing to rise and damaging components.

Short Circuit and Recovery

The MP2151 also enters short-circuit protection (SCP) mode when it reaches the current limit and attempts to recover with hiccup mode. In hiccup mode, the MP2151 disables the output power stage, discharges the soft-start capacitor, and attempts to soft start again automatically. If the short-circuit condition remains after the soft start ends, the MP2151 repeats this cycle until the short circuit is removed and the output rises back to the regulation level.

Over-Voltage Protection (Vo OVP)

The MP2151 monitors the feedback voltage to detect an over-voltage condition. When the feedback voltage rises higher than 115% of the target voltage, the controller enters a dynamic regulation period. During this period, the low side is on until the low-side current drops to -1.5A. This discharges the output to keep it within the normal range. If the over-current condition still remains, the low side turns on again after a 1μs delay. The MP2151 exits this regulation period when the feedback voltage drops below 105% of the reference voltage. If the dynamic regulation cannot limit the increasing of Vo, once the input detects that a 6.1V input over-voltage protection (OVP) has occurred, the MP2151 stops switching until the input voltage drops below 5.7V. The MP2151 then resumes operation.

Power Good (PG) Indicator (only for MP2151XXX-XX)

The MP2151XXX-XX has an open-drain output and requires an external pull-up resistor (100 ~ 500kΩ) for the power good (PG) indicator. When the feedback voltage is within -10%/+15% of the regulation voltage, V_{PG} is pulled up to V_{OUT}/V_{IN} by the external resistor. If the feedback voltage exceeds this window, the internal MOSFET pulls PG to ground. The MOSFET has a maximum $R_{DS(ON)}$ of less than 400Ω.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage. Select a feedback resistor (R1) that will reduce the Vo leakage current (typically 100 - 200kΩ). There is no strict requirement for the feedback resistor. An R1 value greater than 10kΩ is reasonable for most applications. R2 can then be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{out}}{0.6} - 1} \qquad (2)$$

Figure 9 shows the feedback circuit.

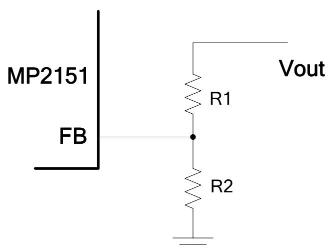


Figure 9: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Values for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200 (1%)	300 (1%)
1.2	200 (1%)	200 (1%)
1.8	200 (1%)	100 (1%)
2.5	200 (1%)	63.2 (1%)
3.3	200 (1%)	44.2 (1%)

Selecting the Inductor

Most applications work best with a 1 - 2.2µH inductor. Select an inductor with a DC resistance less than 50mΩ to optimize efficiency.

A high-frequency, switch-mode power supply with a magnetic device produces a strong electronic magnetic inference in the system. Avoid applying any unshielded power inductor due to poor magnetic shielding. Any shield inductor, such as metal alloy or multiplayer chip power, are ideal for applications as they can decrease the influence effectively. Table 2 lists some recommended inductors.

Table 2: Recommended Inductors

Manufacturer P/N	Inductance (µH)	Manufacturer
PIFE25201B-1R0MS	1.0	CYNTEC CO. LTD.
74437324010	1.0	Wurth

For most designs, estimate the inductance value with Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \qquad (3)$$

Where ΔI_L is the inductor ripple current.

Choose an inductor current that is approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \qquad (4)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient. Higher output voltages may require a 44µF capacitor to increase system stability.

The input capacitor requires an adequate ripple current rating since it absorbs the input switching current. Estimate the RMS current in the input capacitor with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \qquad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \qquad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, ceramic, 0.1µF capacitor as close to the IC as possible.

When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent an excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Output Capacitor

The output capacitor (C2) stabilizes the DC output voltage. Low ESR ceramic capacitors are recommended to limit the output voltage ripple. Estimate the output voltage ripple with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (8)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^{\ 2} \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high-frequency switching converter, a poor layout design can result in poor line or load regulation and stability issues. For best results, refer to Figure 10 and follow the guidelines below.

1. Place the high-current paths (GND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitor as close to VIN and GND as possible.
3. Place the external feedback resistors next to FB.
4. Keep the switching node SW short and away from the feedback network.
5. Keep the VOUT sense line as short as possible or away from the power inductor, especially the surrounding inductor.

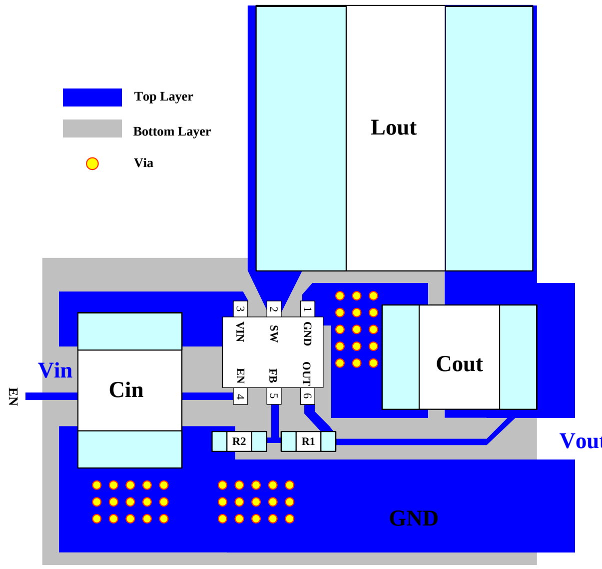


Figure 10: Recommended Layout for MP2151GTF

TYPICAL APPLICATION CIRCUITS

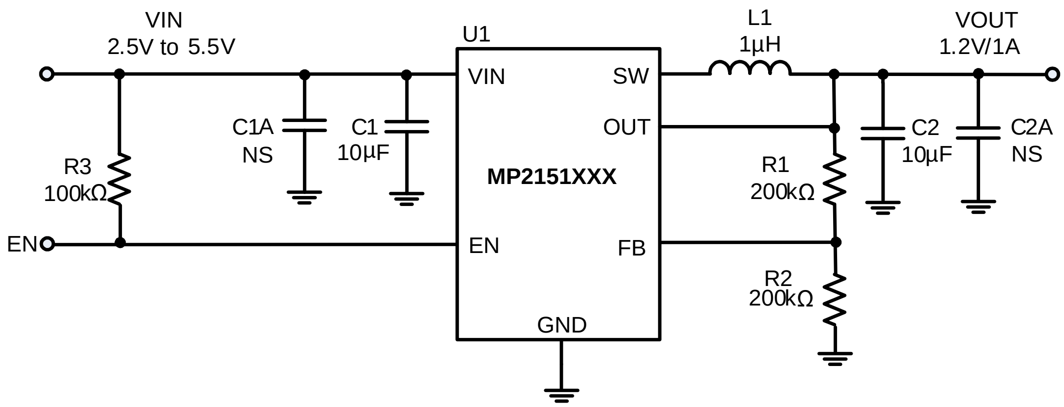


Figure 11: Typical Application Circuit for MP2151XXX
NOTE: VIN < 3.3V applications may require more input capacitors.

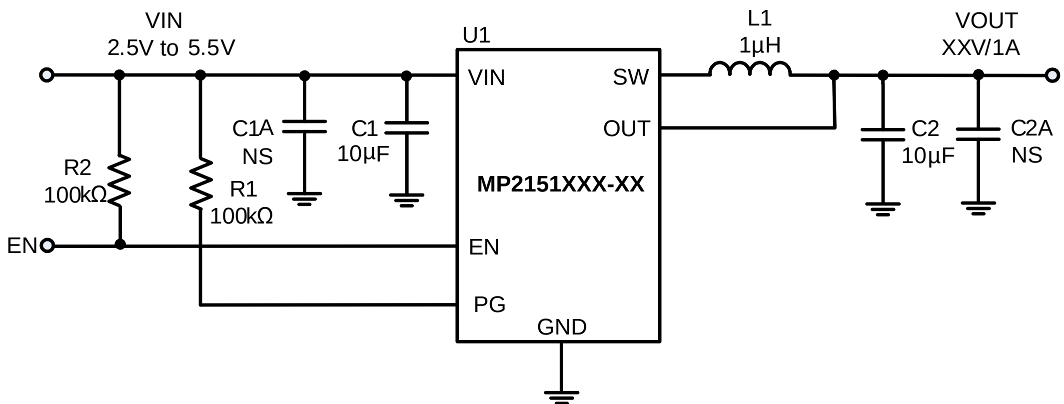
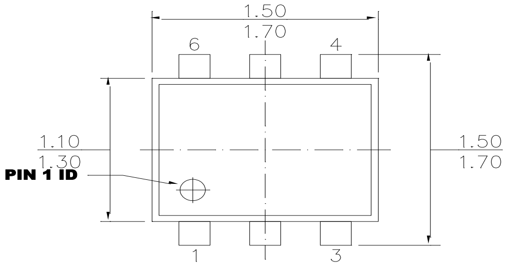


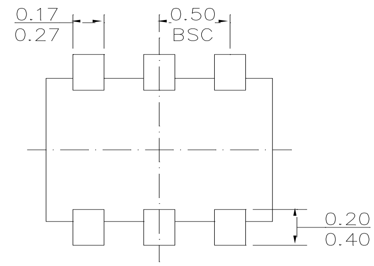
Figure 12: Typical Application Circuit for MP2151XXX-XX
NOTE: VIN < 3.3V applications may require more input capacitors.

PACKAGE INFORMATION

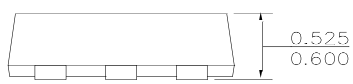
SOT563



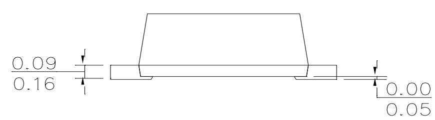
TOP VIEW



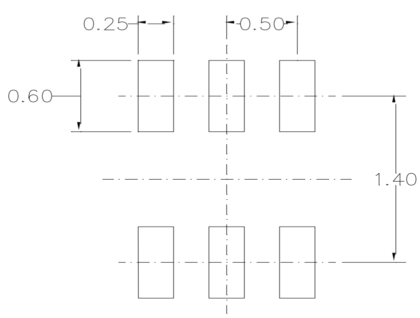
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



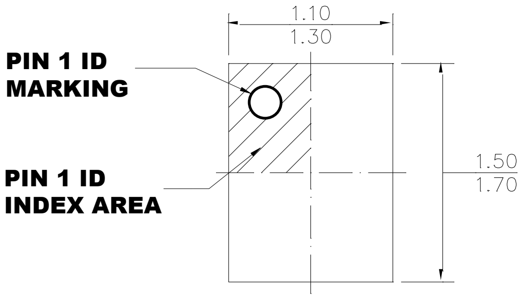
RECOMMENDED LAND PATTERN

NOTE:

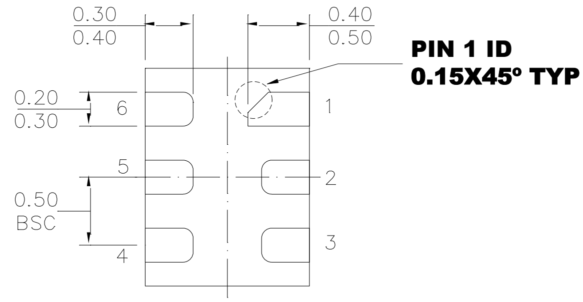
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

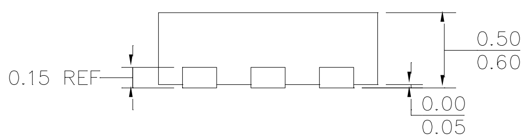
UTQFN (1.2mmx1.6mm)



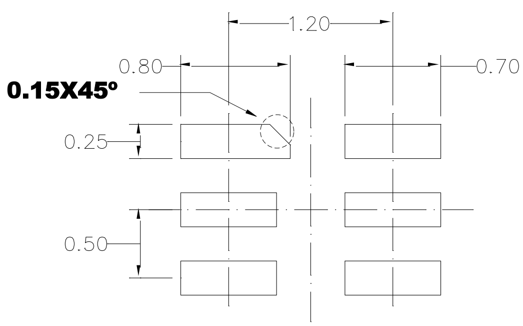
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.