# MP2664

## 500mA, 5V USB, I²C-Controlled Battery Charger with Power Path Management for Single-Cell Li-Ion Battery in QFN Package

## DESCRIPTION

The MP2664 is a highly integrated, single-cell, Li-ion/Li-polymer battery charger with system power path management for space-limited, portable applications. The MP2664 uses input power from either an AC adapter or a USB port to supply the system load and charge the battery independently. The charger features constant current pre-charge, constant current fast charge (CC) and constant voltage (CV) regulation, charge termination, and auto-recharge.

The power path management function ensures continuous power to the system by automatically selecting the input, the battery, or both to power the system. This power stage features a low dropout regulator from the input to the system and a 100mΩ switch from the battery to the system. Power path management separates the charging current from the system load, which allows for proper charge termination and keeps the battery in full-charge mode.

The MP2664 provides system short-circuit protection (SCP) by limiting the current from the input to the system and the battery to the system. This feature is especially critical for preventing the Li-ion battery from being damaged by excessively high currents. An on-chip battery under-voltage lockout (UVLO) cuts off the path between the battery and the system if the battery voltage drops below the programmable battery UVLO threshold, which prevents the Li-ion battery from being over-discharged. An integrated I²C control interface allows the MP2664 to program the charging parameters, such as input current limit, input minimum voltage regulation, charging current, battery regulation voltage, safety timer, and battery UVLO.

The MP2664 is available in a QFN-10 (2mmx2mm) package.

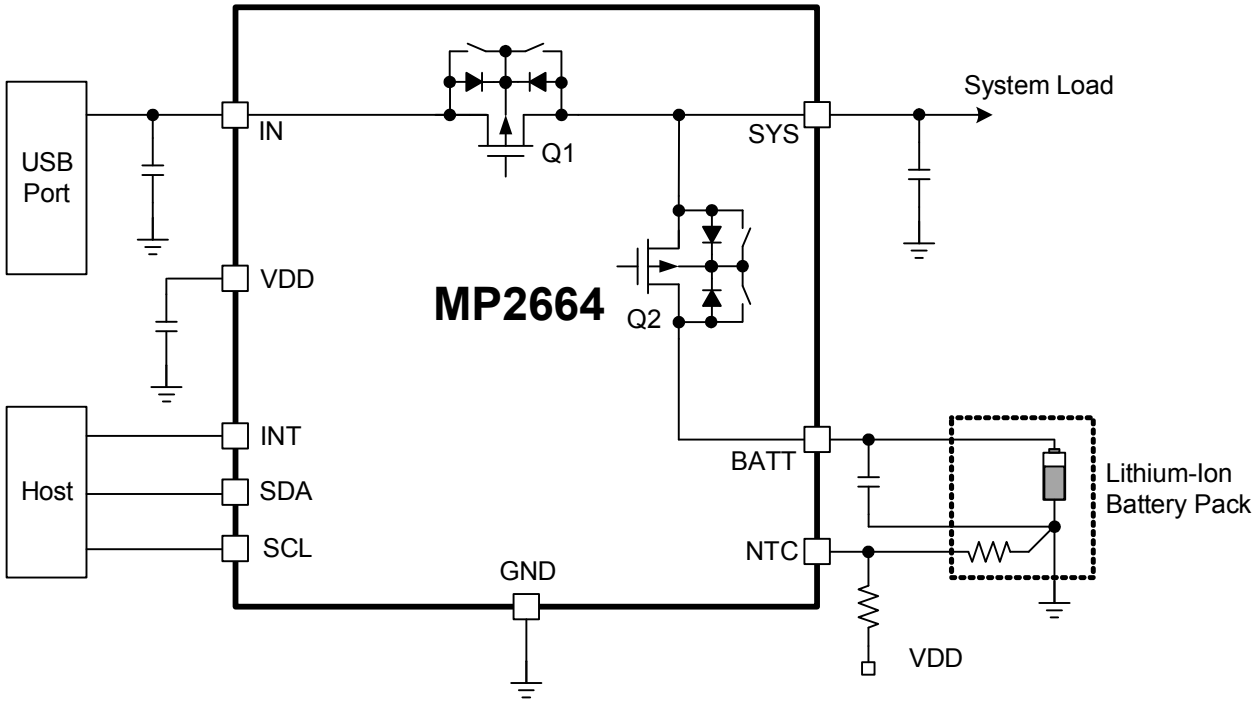
## FEATURES

- Fully Autonomous Charger for Single-Cell Li-Ion/Li-Polymer Batteries
- Complete Power Path Management for Simultaneously Powering the System and Charging the Battery
- ±0.5% Charging Voltage Accuracy
- 13V Maximum Voltage for the Input Source
- I²C Interface for Setting Charging Parameters and Status Reporting
- Fully Integrated Power Switches and No External Blocking Diode Required
- Built-In Robust Charging Protection Including Battery Temperature Monitoring and Programmable Timer
- PCB Over-Temperature Protection (OTP)
- System Reset Function
- Built-In Battery Disconnection Function
- Thermal Limiting Regulation On-Chip
- Available in a QFN-10 (2mmx2mm) Package

## APPLICATIONS

- Wearable Devices
- Smart Handheld Devices
- Fitness Accessories
- Smartwatches

## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|---|---|---|
| MP2664GG-xxxx** | QFN-10 (2mmx2mm) | *See Below* |
| EVKT-MP2664 | Evaluation Kit | |

* For Tape & Reel, add suffix -Z (e.g. MP2664GG-xxxx-Z).

**"xxxx" is the register setting option. The factory default is "0000". This content can be viewed in the I²C register map. Please contact an MPS FAE to obtain an "xxxx" value.

## TOP MARKING

HVY

LLL

HV: Product code of MP2664GG
Y: Year code
LLL: Lot number

## EVALUATION KIT EVKT-MP2664

EVKT-MP2664 Kit contents: (Items below can be ordered separately)

| # | Part Number | Item | Quantity |
|---|---|---|---|
| 1 | EV2664-G-00A | MP2664 evaluation board | 1 |
| 2 | EVKT-USBI2C-02-Bag | Includes one USB to I²C communication interface device, one USB cable, one ribbon cable | 1 |
| 3 | Online resources | Include Datasheet, User guide, Product brief, and GUI | 1 |

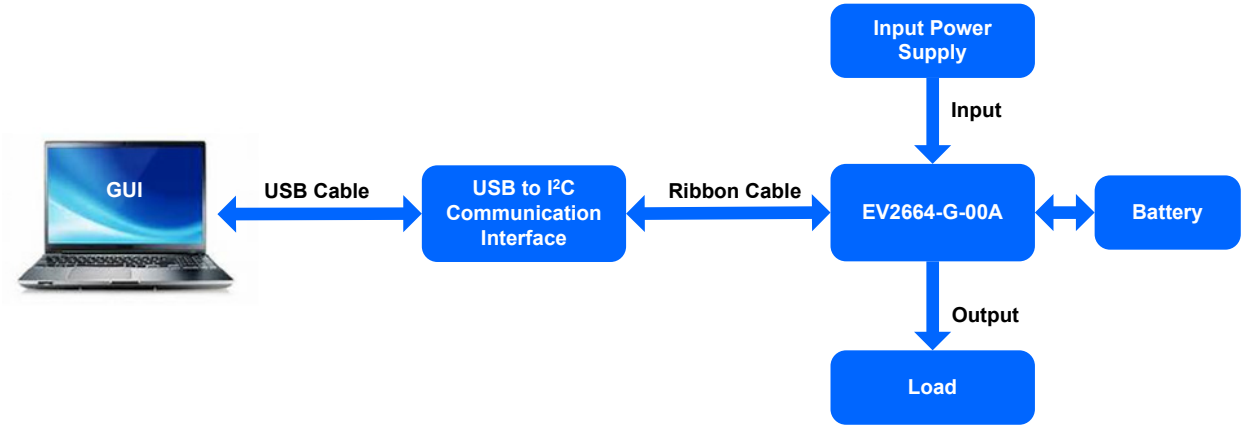
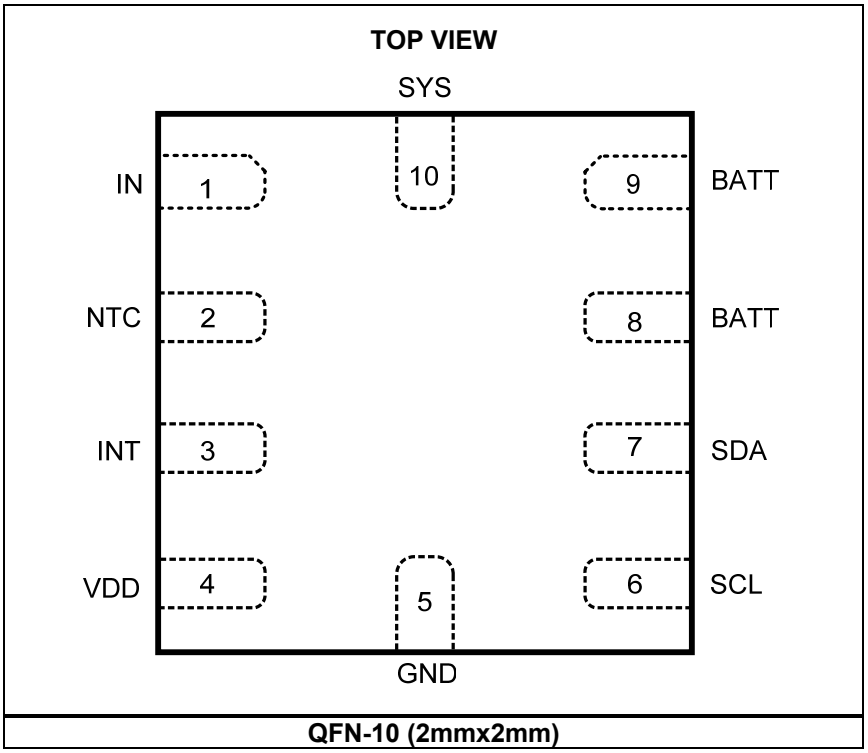



**Figure 1: EVKT-MP2664 Evaluation Kit Set-Up**

## PACKAGE REFERENCE




QFN-10 (2mmx2mm)

## PIN FUNCTIONS

| Pin # | Name | I/O | Description |
|---|---|---|---|
| 1 | IN | Power | **Input power.** Place a ceramic capacitor from IN to GND, as close to the IC as possible. |
| 2 | NTC | I | **Temperature-sense input.** Connect a negative temperature coefficient thermistor to NTC. Program the hot and cold temperature window with a resistor divider from VDD to NTC to GND. The charge is suspended when NTC is out of range. |
| 3 | INT | I/O | **Interrupt signal.** INT can send the charging status and fault interruption to the host. INT can also disconnect the system from the battery. Pull INT from high to low for >16s.The battery FET is off and turns on automatically after >4s regardless of the INT state. The external pull-up resistor at INT must not be smaller than 300kΩ. |
| 4 | VDD | Power | **Internal control power supply.** Connect a ceramic capacitor from VDD to GND. No external load is allowed. |
| 5 | GND | Power | **Ground.** |
| 6 | SCL | I | **I²C interface clock.** Connect SCL to the logic rail through a 10kΩ resistor. |
| 7 | SDA | I/O | **I²C interface data.** Connect SDA to the logic rail through a 10kΩ resistor. |
| 8, 9 | BATT | Power | **Battery.** Place a ceramic capacitor from BATT to GND, as close to the IC as possible. |
| 10 | SYS | Power | **System power supply.** Place a ceramic capacitor from SYS to GND, as close to the IC as possible. |

## ABSOLUTE MAXIMUM RATINGS (1)

$V_{IN}$ ..... -0.3V to +13V
All other pins to GND ..... -0.3V to +6.0V
Continuous power dissipation ($T_A$ = 25°C) (2)
..... 1.25W
Junction temperature ..... 150°C
Lead temperature (solder) ..... 260°C
Storage temperature ..... -65°C to +150°C

### *Recommended Operating Conditions* (3)

Supply voltage ($V_{IN}$) ..... 4.35V to 5.5V (USB input)
$I_{IN}$ ..... Up to 455mA
$I_{SYS}$ ..... Up to 3.2A (5)
$I_{CHG}$ ..... Up to 455mA
$V_{BATT}$ ..... Up to 4.545V
Operating junction temp ($T_J$) ..... -40°C to +125°C

### *Thermal Resistance* (4) $\theta_{JA}$ $\theta_{JC}$

| | | | |
|---|---|---|---|
| QFN-10 (2mmx2mm) | 80 | 16 | °C/W |

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$) / $\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.
5) Guaranteed by design.

## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 5.0V, $V_{BATT}$ = 3.5V, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Input Source and Battery Protection** | | | | | | |
| Input operation voltage | $V_{IN}$ | | 4.35 | 5 | 5.5 | V |
| Battery input voltage (6) | $V_{BATT}$ | | | | 4.5 | V |
| Input over-voltage protection trigger threshold | $V_{IN\_OVP}$ | Input rising threshold | 5.85 | 6 | 6.15 | V |
| Input over-voltage protection recover threshold | | | | 350 | | mV |
| Input under-voltage lockout threshold | $V_{IN\_UVLO}$ | Input rising threshold | 3.8 | 3.9 | 4 | V |
| Input under-voltage lockout threshold hysteresis | | | | 170 | | mV |
| Input vs. battery voltage headroom threshold | $V_{HDRM}$ | Input rising vs. battery | 100 | 130 | 160 | mV |
| Input vs. battery voltage headroom threshold hysteresis | | | | 85 | | mV |
| Battery under-voltage lockout threshold | $V_{BATT\_UVLO}$ | I²C programmable range | 2.4 | | 3.1 | V |
| | | Falling, programmable, REG01h, bits[2:0] = 100 | 2.6 | 2.8 | 3 | V |
| Battery under-voltage threshold hysteresis | | | | 210 | | mV |
| Battery over-voltage protection threshold | $V_{BATT\_OVP}$ | Rising, higher than $V_{BATT\_REG}$ | | 130 | | mV |
| Battery over-voltage protection hysteresis | | | | 70 | | |
| **Power Path Management** | | | | | | |
| System regulation voltage | $V_{SYS\_REG}$ | $V_{IN}$ = 5.5V, $I_{SYS}$ = 10mA, $I_{CHG}$ = 0A | 4.55 | 4.65 | 4.75 | V |
| Input current limit | $I_{IN\_LIM}$ | REG00h, bits[2:0] = 000 - 85mA | 65 | 75 | 85 | mA |
| | | REG00h, bits[2:0] = 001 - 130mA | 102 | 116 | 130 | |
| | | REG00h, bits[2:0] = 100 - 265mA | 230 | 247 | 265 | |
| | | REG00h, bits[2:0] = 111 - 455mA | 400 | 428 | 455 | |
| Input minimum voltage regulation | $V_{IN\_MIN}$ | I²C programmable range | 3.88 | | 5.08 | V |
| | | I²C setting $V_{IN\_MIN}$ = 4.20V | 4.1 | 4.2 | 4.3 | |
| IN to SYS switch on resistance | $R_{ON\_Q1}$ | $V_{IN}$ = 5V, $I_{SYS}$ = 100mA | | 300 | 400 | mΩ |
| Input quiescent current | $I_{IN\_Q}$ | $V_{IN}$ = 5.5V, CEB = 0, charge enabled, $I_{CHG}$ = 0A, $I_{SYS}$ = 0A | | 630 | | µA |
| | | $V_{IN}$ = 5.5V, CEB = 1, charge disabled | | 500 | | |
| Battery quiescent current | $I_{BATT\_Q}$ | $V_{IN}$ = 5V, CEB = 0, $I_{SYS}$ = 0A, $V_{BATT}$ = 4.3V | | 32 | | µA |
| | | $V_{IN}$ = 0V, CEB = 1, $I_{SYS}$ = 0A, $V_{BATT}$ = 4.35V, disable PCB OTP function, do not include the current from external NTC resistor | | 11 | 13 | µA |
| | | $V_{IN}$ = 0V, CEB = 1, $I_{SYS}$ = 0A, $V_{BATT}$ = 4.35V, enable PCB OTP function, do not include the current from external NTC resistor | | 20 | 24 | µA |
| | | $V_{BATT}$ = 4.5V, $V_{IN}$ = $V_{SYS}$ = GND, FET_DIS = 1, shipping mode | | 4 | 5.5 | µA |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5.0V, $V_{BATT}$ = 3.5V, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Battery FET on resistance | $R_{ON\_Q2}$ | $V_{IN}$ < 2V, $V_{BATT}$ = 3.5V, $I_{SYS}$ = 100mA | | 100 | 150 | mΩ |
| Battery current regulation in discharge mode | $I_{DSCHG}$ | I²C programmable range | 400 | | 3200 (6) | mA |
| Battery FET switch leakage | | $V_{BATT}$ = 4.5V, $V_{IN}$ = $V_{SYS}$ = GND, disconnect mode | | | 1 | μA |
| SYS reverse to BATT switch leakage | | $V_{SYS}$ = 6V, $V_{IN}$ = 4.5V, $V_{BATT}$ = GND, CEB = 1 | | | 1 | μA |
| Battery FET disconnect by INT (6) | $t_{INT}$ | INT pull-low lasting time to turn off the battery FET | | 16 | | s |
| | | Battery FET off lasting time before turn-on | | 4 | | |
| **Battery Charger** | | | | | | |
| Battery charge voltage regulation | $V_{BATT\_REG}$ | I²C programmable range | 3.6 | | 4.545 | V |
| | | REG04h, bits[7:2] = 101000 | 4.179 | 4.2 | 4.221 | |
| | | REG04h, bits[7:2] = 110010 | 4.328 | 4.35 | 4.372 | |
| Fast charge current | $I_{CC}$ | $V_{IN}$ = 5V, $V_{BATT}$ = 3.8V, I²C programmable range | 8 | | 535 (6) | mA |
| | | $V_{IN}$ = 5V, $V_{BATT}$ = 3.8V, $I_{CC\_SETTING}$ = 93mA | 88 | 93 | 98 | |
| | | $V_{IN}$ = 5V, $V_{BATT}$ = 3.8V, $I_{CC\_SETTING}$ = 246mA | 232 | 248 | 263 | |
| | | $V_{IN}$ = 5V, $V_{BATT}$ = 3.8V, $I_{CC\_SETTING}$ = 399mA | 376 | 401 | 440 | |
| Junction temperature regulation (6) | $T_{J\_REG}$ | REG06h, bits[1:0] = 11 - 120°C | | 120 | | °C |
| Pre-charge current | $I_{PRE}$ | I²C programmable range | 6 | | 27 | mA |
| | | $I_{PRE\_SETTING}$ = 6mA, REG03h, bits[1:0] = 00 | 2.5 | 4.7 | | mA |
| | | $I_{PRE\_SETTING}$ = 20mA, REG03h, bits[1:0] = 10 | 14 | 18 | 22 | mA |
| Charge termination current threshold | $I_{TERM}$ | $I_{CC\_SETTING}$ ≤ 263mA, (REG02h, bit[4] = 0), REG03h, bits[1:0] = 00 | 5 | 7 | 9 | mA |
| | | $I_{CC\_SETTING}$ ≤ 263mA, (REG02h, bit[4] = 0), REG03h, bits[1:0] = 01 | 10 | 13.5 | 17 | mA |
| | | $I_{CC\_SETTING}$ ≤ 263mA, (REG02h, bit[4] = 0), REG03h, bits[1:0] = 10 | 16 | 20 | 24 | mA |
| | | $I_{CC\_SETTING}$ ≤ 263mA, (REG02h, bit[4] = 0), REG03h, bits[1:0] = 11 | 22 | 27 | 32 | mA |
| | | $I_{CC\_SETTING}$ ≤ 280mA, (REG02h, bit[4] = 1), REG03h, bits[1:0] = 00 | 10 | 13.5 | 17 | mA |
| | | $I_{CC\_SETTING}$ ≤ 280mA, (REG02h, bit[4] = 1), REG03h, bits[1:0] = 01 | 22 | 27 | 32 | mA |
| | | $I_{CC\_SETTING}$ ≤ 280mA, (REG02h, bit[4] = 1), REG03h, bits[1:0] = 10 | 34 | 42 | 49 | mA |
| | | $I_{CC\_SETTING}$ ≤ 280mA, (REG02h, bit[4] = 1), REG03h, bits[1:0] = 11 | 46 | 55 | 64 | mA |
| Charge termination current threshold hysteresis | $I_{TERM\_HYS}$ | $I_{CC\_SETTING}$ ≤ 263mA, (REG02h, bit[4] = 0), REG03h, bits[1:0] = 10 | | | | |
| | | $I_{CC\_SETTING}$ ≤ 280mA, (REG02h, bit[4] = 0), REG03h, bits[1:0] = 10 | | | | |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5.0V, $V_{BATT}$=3.5V, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Pre-charge to fast charge threshold | $V_{BATT\_PRE}$ | $V_{BATT}$ rising, set $V_{BATT\_PRE}$ = 3V | 2.8 | 3 | 3.1 | V |
| Pre-charge to fast charge threshold hysteresis | | | | 90 | | mV |
| Auto-recharge battery voltage threshold | $V_{RECH}$ | REG04h, bit[0] = 0 | 120 | 160 | 200 | mV |
| | | REG04h, bit[0] = 1 | 260 | 300 | 365 | |
| **Thermal Protection** | | | | | | |
| Thermal shutdown threshold (6) | $T_{J\_SHDN}$ | Rising | | 150 | | °C |
| Thermal shutdown hysteresis (6) | | | | 20 | | °C |
| NTC output current | $I_{NTC}$ | CEB = 0, NTC = 3V | -100 | 0 | +100 | nA |
| NTC cold temperature rising threshold | $V_{COLD}$ | As a percentage of $V_{DD}$ | 63 | 65 | 67 | % |
| NTC cold temperature rising threshold hysteresis | | | | 30 | | mV |
| NTC hot temperature falling threshold | $V_{HOT}$ | As a percentage of $V_{DD}$ | 31 | 33 | 35 | % |
| NTC hot temperature falling threshold hysteresis | | | | 70 | | mV |
| NTC hot temperature falling threshold for PCB OTP | $V_{HOT\_PCB}$ | As a percentage of $V_{DD}$ | 30 | 32 | 34 | % |
| NTC hot temperature falling threshold hysteresis for PCB OTP | | | | 85 | | mV |
| **Logic I/O Pin Characteristics** (6) | | | | | | |
| Low logic voltage threshold | $V_L$ | | | | 0.4 | V |
| High logic voltage threshold | $V_H$ | | 1.3 | | | V |
| **I²C Interface (SDA, SCL)** (6) | | | | | | |
| Input high voltage level | $V_{IH}$ | $V_{PULL\_UP}$ = 1.8V, SDA and SCL | 1.3 | | | V |
| Input low voltage level | $V_{IL}$ | $V_{PULL\_UP}$ = 1.8V, SDA and SCL | | | 0.4 | V |
| Output low voltage level | $V_{OL}$ | $I_{SINK}$ = 5mA | | | 0.4 | V |
| I²C clock frequency | $F_{SCL}$ | | | | 400 | kHz |
| **Clock Frequency and Watchdog Timer** | | | | | | |
| Clock frequency | $F_{CLK}$ | | | 32 | | kHz |
| Watchdog timer | $t_{WDT}$ | Programmable, REG05h, bits[5:4] = 11 | | 160 | | s |

**Note:**

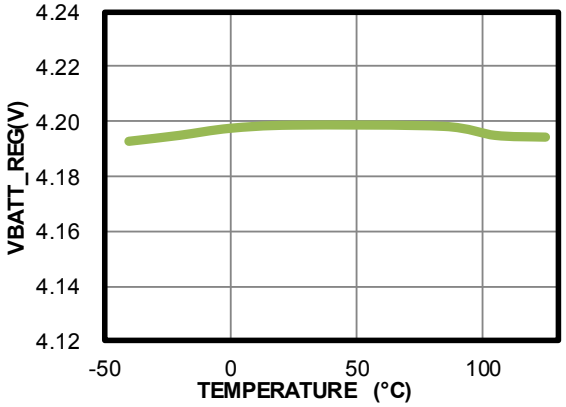
6) Guaranteed by design.

## TYPICAL PERFORMANCE CHARACTERISTICS

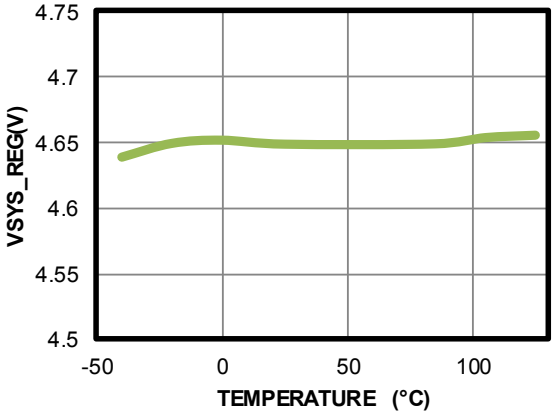
**$V_{IN}$ = 5V, $T_A$ = 25°C, $I_{IN\_LIM}$ = 455mA, $I_{CC}$ = 246mA, $V_{IN\_MIN}$ = 4.6V, unless otherwise noted.**

**Battery Regulation Voltage vs. Temperature**

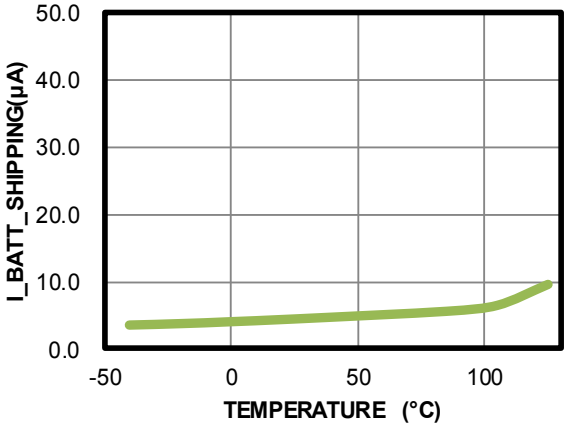
$V_{BATT\_REG}$ = 4.2V




**System Regulation Voltage vs. Temperature**

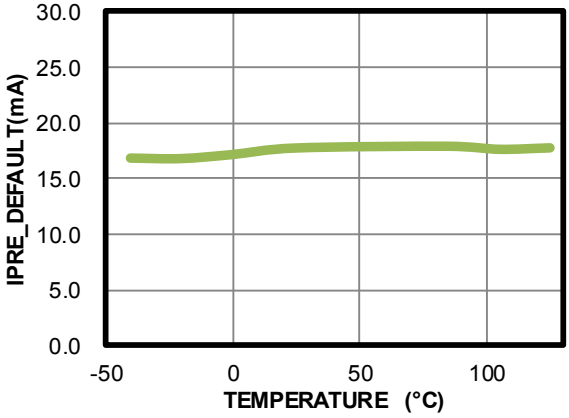



**Battery Current under Shipping Mode vs. Temperature**



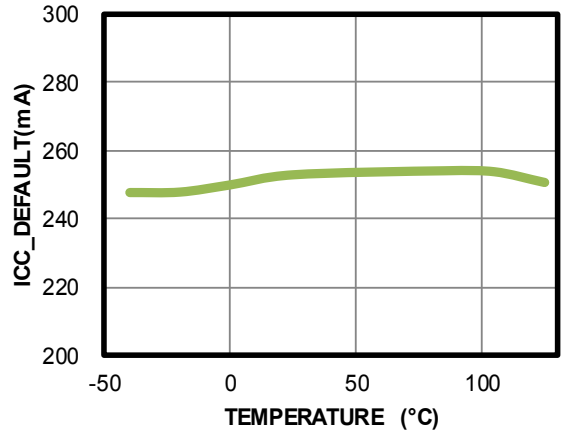

**Pre-Charge Current vs. Temperature**

$I_{PRE}$ = 20mA



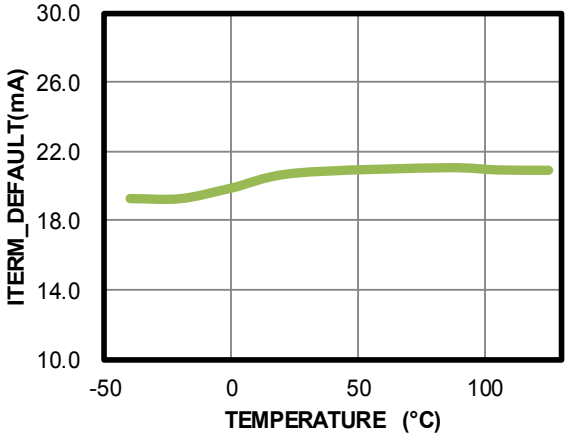

**CC Charge Current vs. Temperature**

$I_{CC}$ = 246mA




**Battery Termination Current vs. Temperature**

$I_{TERM}$ = 20mA

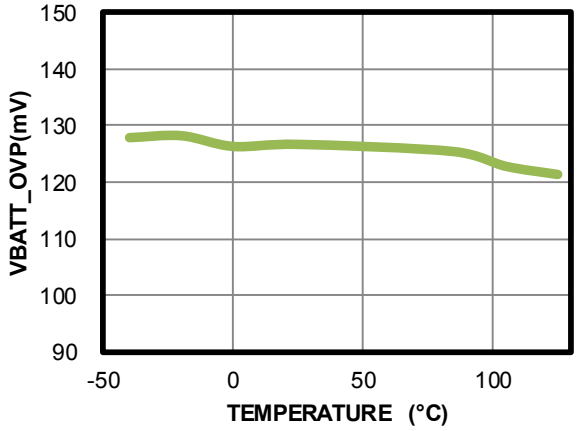


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5V, $T_A$ = 25°C, $I_{IN\_LIM}$ = 455mA, $I_{CC}$ = 246mA, $V_{IN\_MIN}$ = 4.6V, unless otherwise noted.**

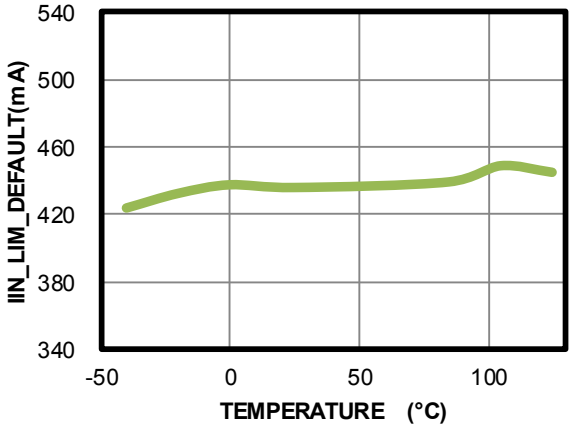
**Battery OVP Voltage vs. Temperature**

Higher than $V_{BATT\_REG}$



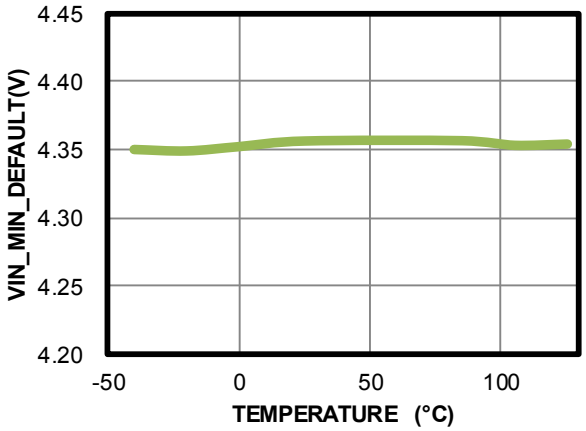

**Input Current Limit vs. Temperature**

$I_{IN\_LIM}$ = 455mA




**Input Minimum Voltage vs. Temperature**

$V_{IN\_MIN}$ = 4.36V

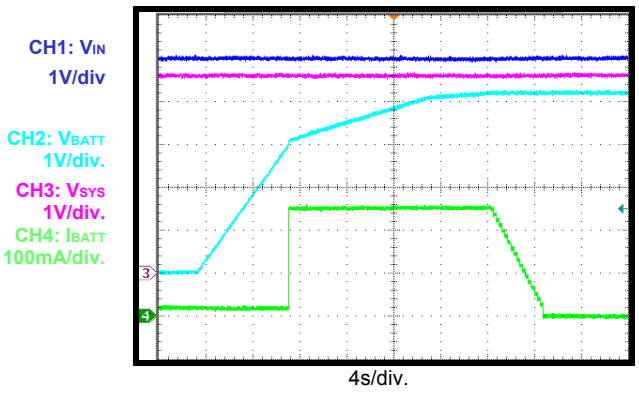


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5V, $T_A$ = 25°C, $I_{IN\_LIM}$ = 455mA, $I_{CC}$ = 246mA, $V_{IN\_MIN}$ = 4.6V, unless otherwise noted.**

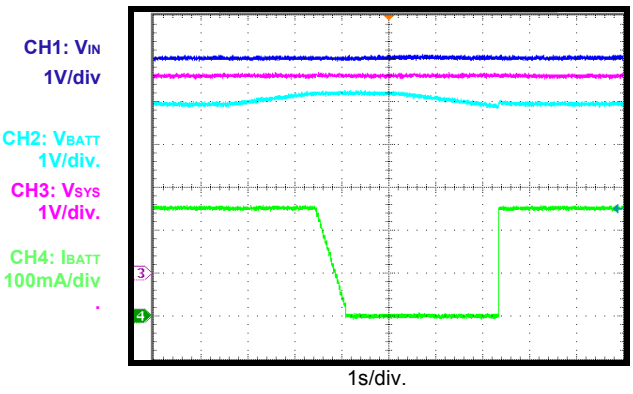
### Battery Charge Curve

$I_{SYS}$ = 0A



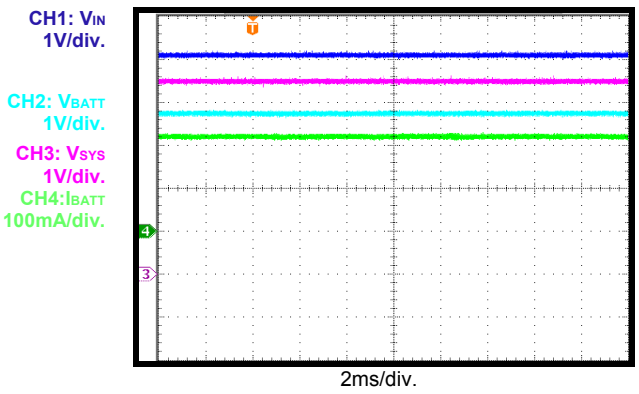

### Auto-Recharge

$I_{SYS}$ = 0A



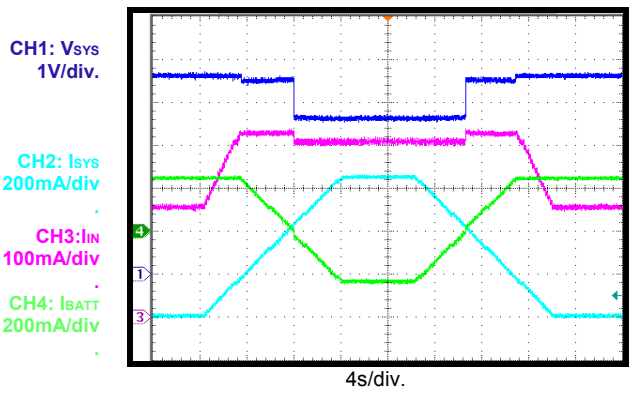

### CC Charge Steady State

$V_{BATT}$ = 3.7V, $I_{SYS}$ = 200mA



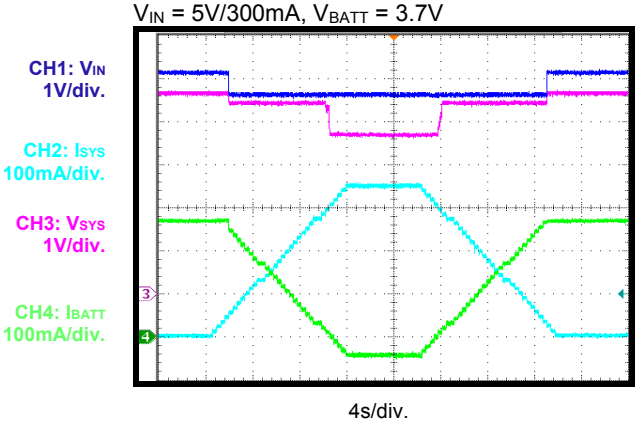

### Input Current Limit-Based PPM

$V_{BATT}$ = 3.7V



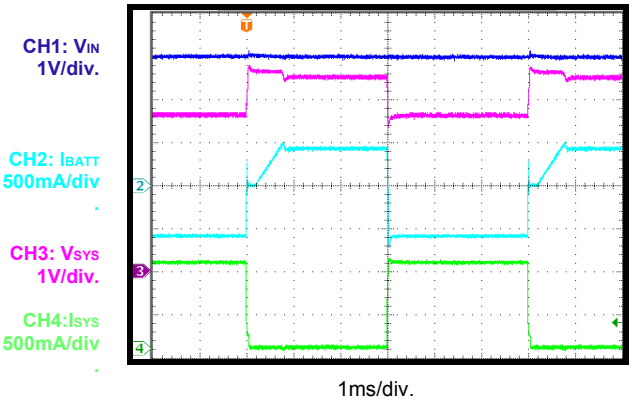

### Input Voltage Regulation-Based PPM

$V_{IN}$ = 5V/300mA, $V_{BATT}$ = 3.7V




### SYS Load Transient

$V_{IN}$ = 5V, $V_{BATT}$ = 3.7V, $I_{CC}$ = 535mA, $I_{SYS}$ = 0 - 1A

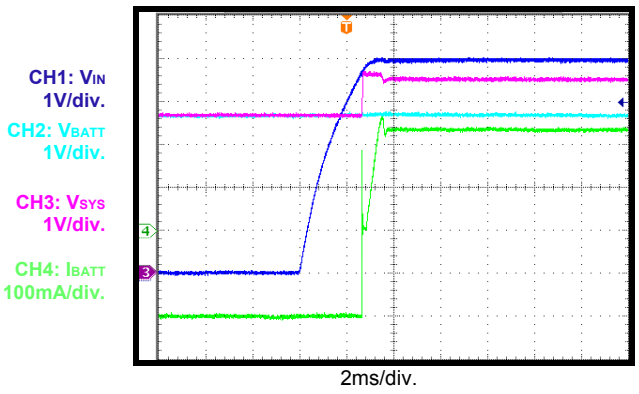


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5V, $T_A$ = 25°C, $I_{IN\_LIM}$ = 455mA, $I_{CC}$ = 246mA, $V_{IN\_MIN}$ = 4.6V, unless otherwise noted.**

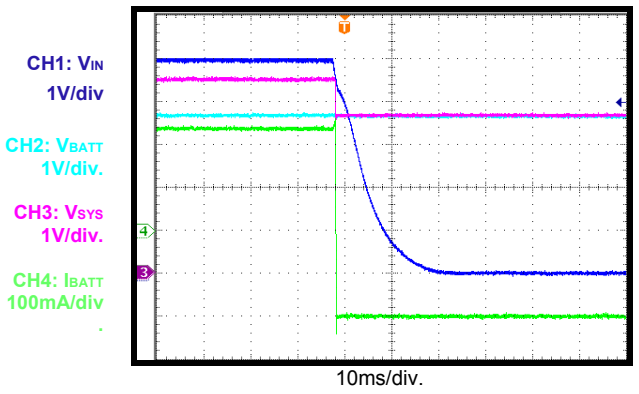
### Power On

$V_{BATT}$ = 3.7V, $I_{SYS}$ = 200mA



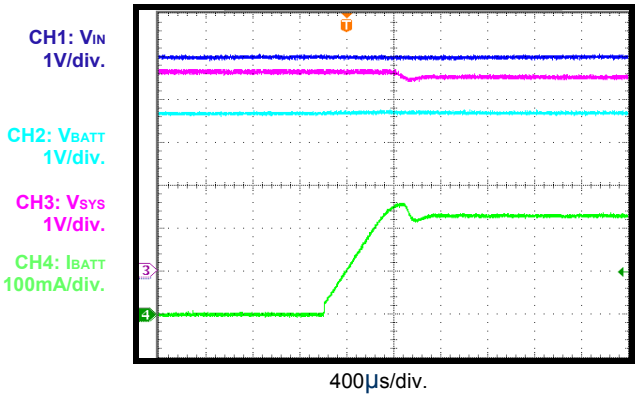

### Power Off

$V_{BATT}$ = 3.7V, $I_{SYS}$ = 200mA



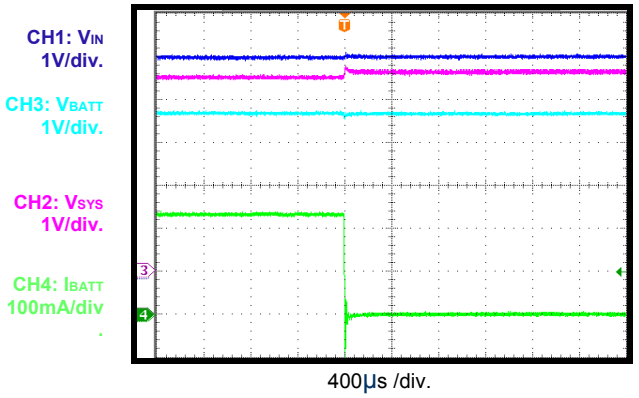

### Charge Enable

$V_{BATT}$ = 3.7V, $I_{SYS}$ = 200mA



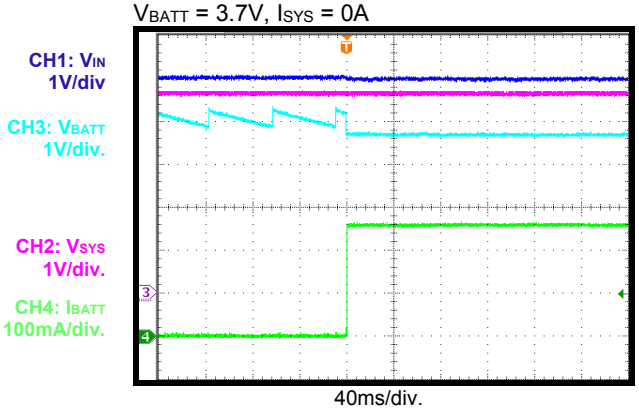

### Charge Disable

$V_{BATT}$ = 3.7V, $I_{SYS}$ = 200mA



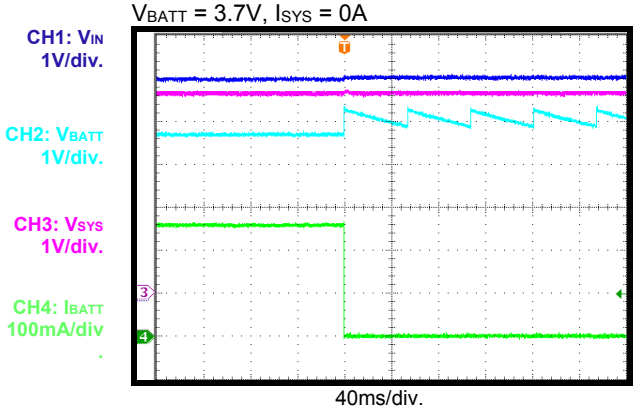

### BATT Insertion

$V_{BATT}$ = 3.7V, $I_{SYS}$ = 0A




### BATT Removal

$V_{BATT}$ = 3.7V, $I_{SYS}$ = 0A

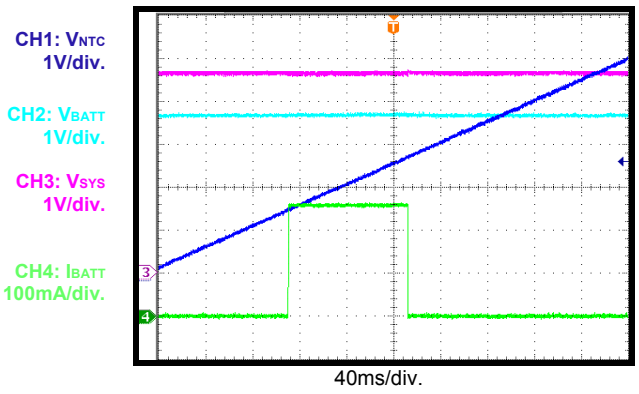


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5V, $T_A$ = 25°C, $I_{IN\_LIM}$ = 455mA, $I_{CC}$ = 246mA, $V_{IN\_MIN}$ = 4.6V, unless otherwise noted.**

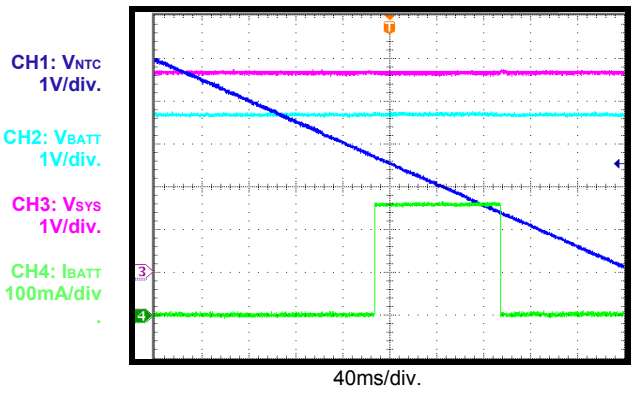
### NTC Rising

$V_{BATT}$ = 3.7V, $I_{SYS}$ = 0A, PCB OTP disable



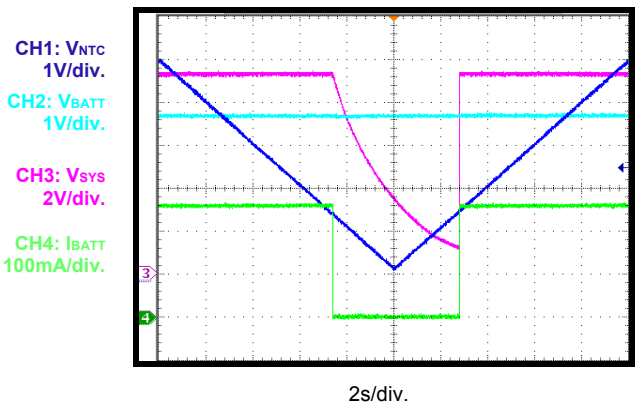

### NTC Falling

$V_{BATT}$ = 3.7V, $I_{SYS}$ = 0A, PCB OTP disable



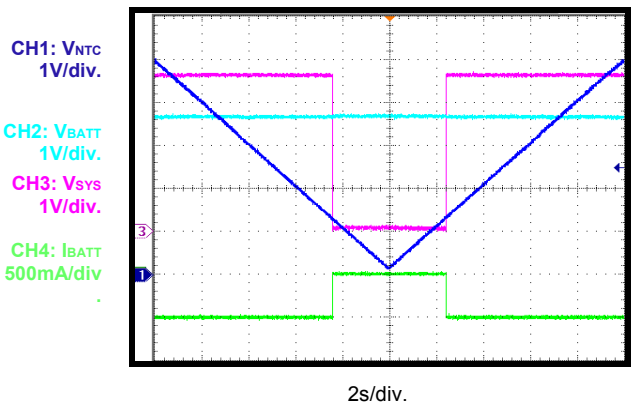

### PCB OTP @ Charge Mode

$V_{BATT}$ = 3.7V, $I_{SYS}$ = 0A



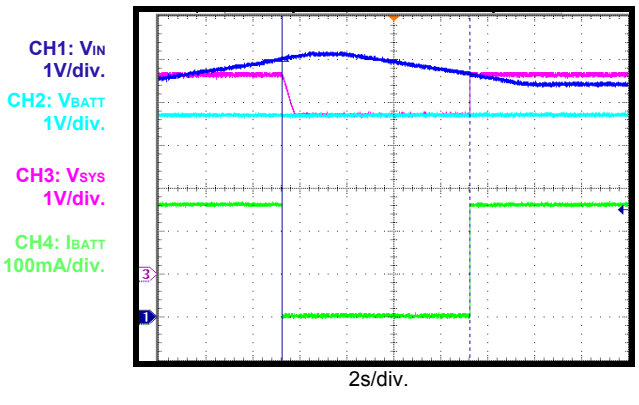

### PCB OTP @ Discharge Mode

$V_{IN}$ = 0V, $V_{BATT}$ = 3.7V, $I_{SYS}$ = 500mA




### $V_{IN}$ OVP Operation

$V_{BATT}$ = 3.7V, $I_{SYS}$ = 0A



## FUNCTIONAL BLOCK DIAGRAM

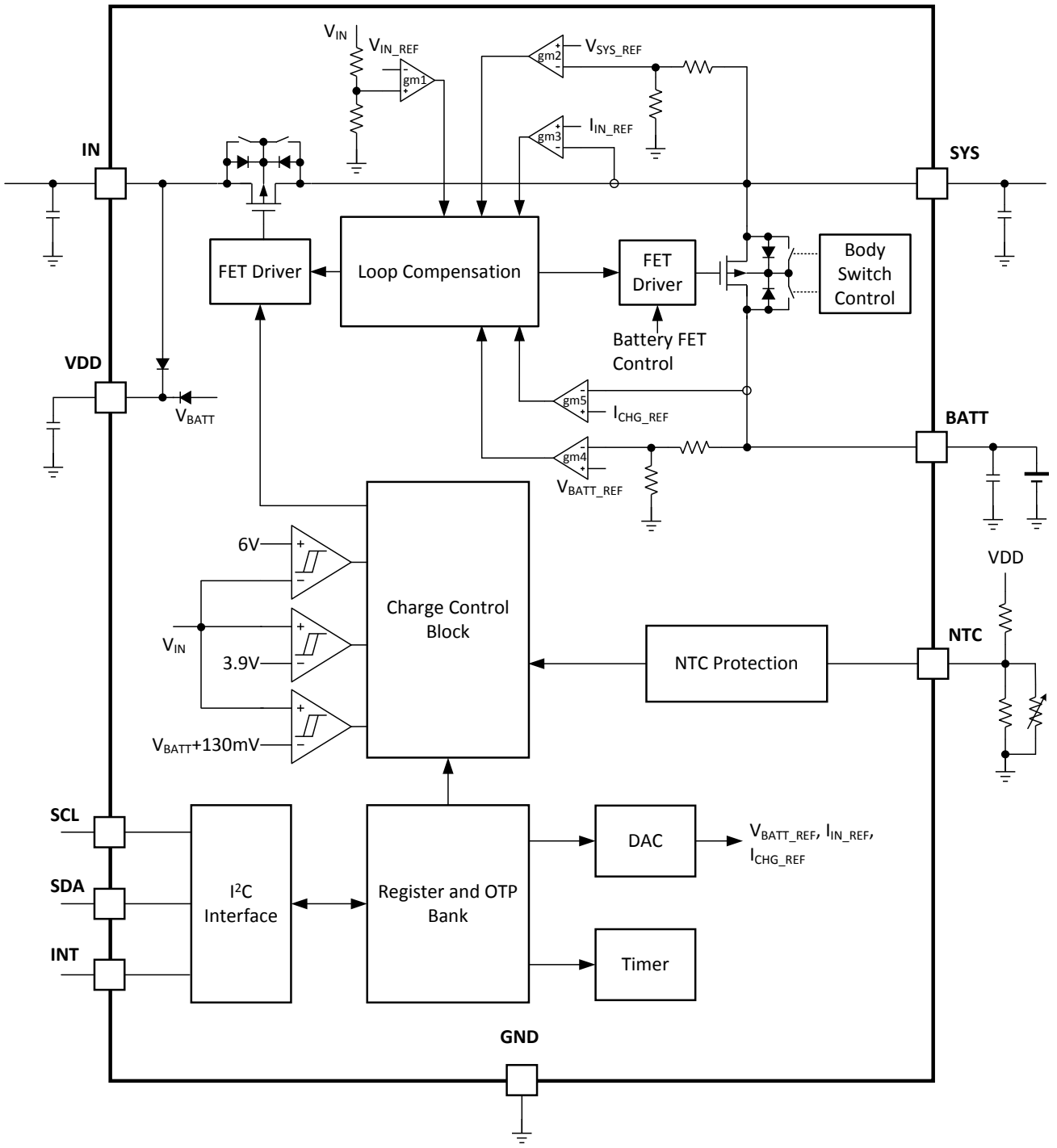



**Figure 2: Function Block Diagram**

## OPERATION

The MP2664 is an I²C-controlled, single-cell, Li-ion or Li-polymer battery charger with complete power path management. The full-charge function features constant current pre-charge (PRE-C), constant current fast-charge (CC) and constant voltage (CV) regulation, charge termination, auto-recharge, and a built-in timer. The power path function allows the input source to power the system and charge the battery simultaneously. If there is a conflict in meeting both the system load and battery charging current, the IC reduces the charging current automatically or uses the battery as a supplemental power to satisfy the system load.

The IC integrates a 300mΩ low-dropout (LDO) FET between IN and SYS and a 100mΩ battery FET between SYS and BATT.

In charging mode, the on-chip 100mΩ battery FET works as a full-featured linear charger with constant current pre-charging, constant current fast-charging and constant-voltage charging, charge termination, auto-recharging, NTC monitoring, built-in timer control, and thermal protection. The charge current can be programmed via the I²C interface. The IC limits the charge current when the die temperature exceeds the thermal regulation threshold (120°C default).

In supplement mode, the 100mΩ battery FET is fully turned on to connect the battery to the system load when the input power is not enough to power the system load. When the input is removed, the 100mΩ battery FET is also fully turned on, allowing the battery to power up the system.

When the system load is satisfied, the remaining current is used to charge the smart power path management battery. The IC reduces the charging current or uses power from the battery to satisfy the system load when its demand is over the input power capacity.

Figure 3 shows the power path management structure of the MP2664.

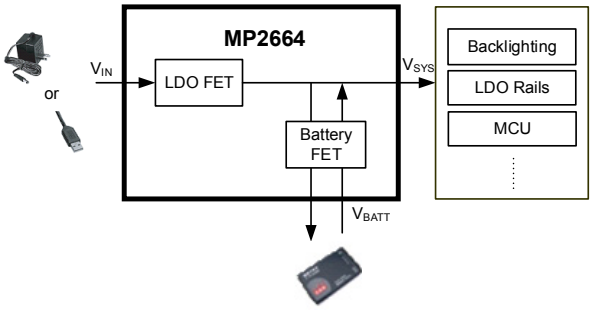



**Figure 3: Power Path Management Structure**

### Power Supply

The internal bias circuit of the IC is powered from IN or BATT, whichever voltage is higher. When IN or BATT exceeds the respective under-voltage lockout (UVLO) threshold, the sleep comparator, battery depletion comparator, and the battery FET driver are active. The I²C interface is ready for communication, and all registers are reset to the default value. The host can access all registers.

### Input OVP and UVLO

The MP2664 has an input over-voltage protection (OVP) threshold and an input UVLO threshold. Once the input voltage ($V_{IN}$) exits the normal input voltage range, the Q1 FET is turned off immediately.

When $V_{IN}$ is identified as a good source, a 200µs immunity timer becomes active. If $V_{IN}$ is still sufficient until the 200µs timer expires, the system starts up. Otherwise, Q1 remains off.

Figure 4 depicts the operation profile.

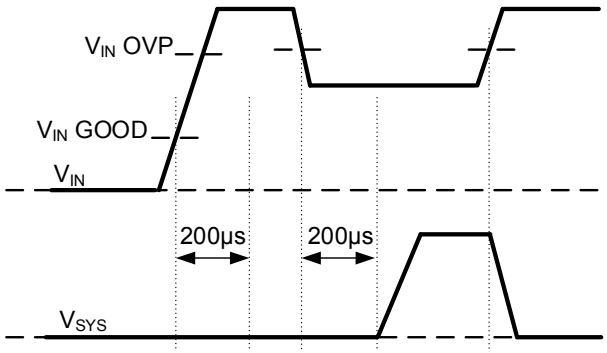



**Figure 4: Input Power Detection Operation Profile**

### Power Path Management

The IC employs a direct power path structure with the battery FET, which decouples the system from the battery and allows for separate control between the system and the battery. The system is given priority to start up even with a deeply discharged or missing battery. When the input power is available, even with a depleted battery, the system voltage ($V_{SYS}$) is always regulated to $V_{SYS\_REG}$ by the integrated LDO FET.

The direct power structure is composed of a frond-end LDO FET between IN and SYS and a battery FET between SYS and BATT (see Figure 3). The LDO FET and battery FET can be controlled by the I²C.

**Table 1: FET Control by I²C**

| FET On/Off Changed By Control | Hi-Z Mode and Charge Control | |
|---|---|---|
| | Set EN_HIZ to 1 | Set CEB to 1 |
| LDO FET | OFF | x |
| Battery FET (charging) | x | OFF |
| Battery FET (discharging) | x | x |

The input LDO (using an LDO FET) provides power to the system, which drives the system load directly and charges the battery through the battery FET.

For the system voltage control, when $V_{IN}$ is above $V_{SYS\_REG}$, $V_{SYS}$ is regulated to $V_{SYS\_REG}$. When $V_{IN}$ is below $V_{SYS\_REG}$, the LDO FET is fully on with the input current limit.

### Battery Charge Profile

The IC provides three main charging phases: constant current pre-charge, constant current fast-charge, and constant-voltage charge (see Figure 5).

1. Phase 1 (constant current pre-charge): The IC is able to pre-charge the deeply depleted battery safely until the battery voltage ($V_{BATT}$) reaches the pre-charge to the fast-charge threshold ($V_{BATT\_PRE}$). The pre-charge current is programmable via REG03h, bits[1:0]. If $V_{BATT\_PRE}$ is not reached before the pre-charge timer (1hr) expires, the charge cycle is stopped, and a corresponding timeout fault signal is asserted.
2. Phase 2 (constant current fast charge): When $V_{BATT}$ exceeds $V_{BATT\_PRE}$, the IC enters a constant current fast-charge phase. The fast-charge current can be programmable via REG02h, bits[4:0].
3. Phase 3 (constant-voltage charge): When $V_{BATT}$ rises to the pre-programmable charge full voltage ($V_{BATT\_REG}$) set via REG04h, bits[7:2], the charge mode changes from CC mode to CV mode, and the charge current begins to taper off.

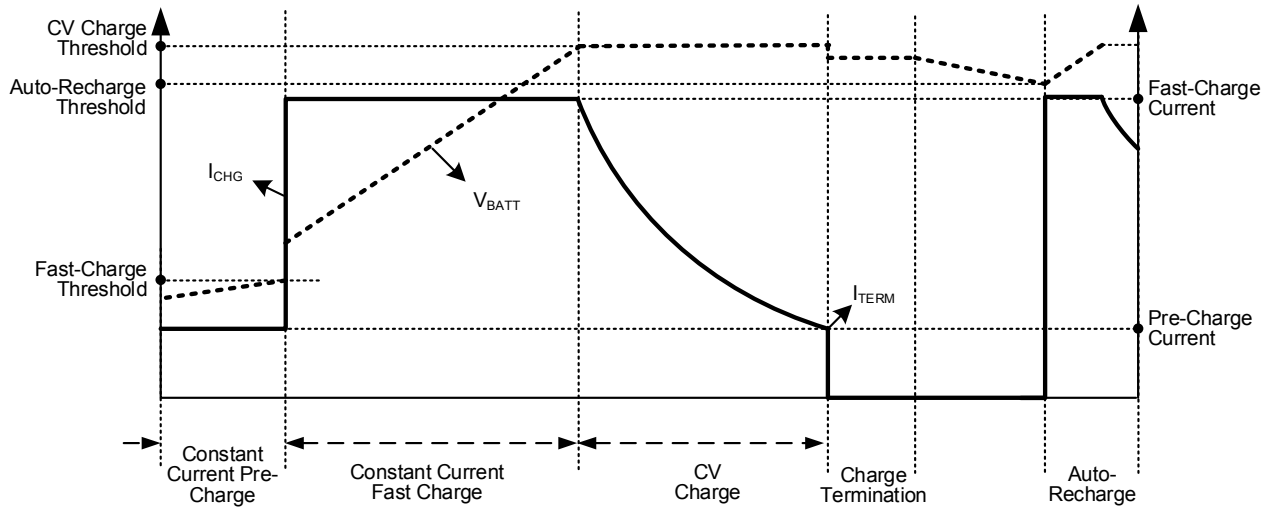



**Figure 5: Battery Charge Profile**

Assuming that the termination function (EN_TERM) is set via REG05h, bit[6] = 1, the charge cycle is considered to be complete when the following conditions are valid:

- The charge current ($I_{BATT}$) reaches the end of charge (EOC) current threshold ($I_{TERM}$), and the 2.5ms delay timer is initiated.
- During the 2.5ms delay period, $I_{BATT}$ is always smaller than $I_{TERM}$ + $I_{TERM\_HYS}$.

The charge status is marked as complete once the 2.5ms delay timer expires.

The charge current is terminated at the same time if TERM_TMR is set via REG05h, bit[0] = 0; otherwise, the charge current continues tapering off.

If EN_TERM = 0, the termination function is disabled, and the above actions will not occur (see Table 2).

**Table 2: Termination Function Selection Table**

| EN_TERM | TERM_TMR | After $I_{BATT}$ Reaches $I_{TERM}$ in CV Mode | |
|---|---|---|---|
| | | Operation | Charge Status |
| 0 | x | Keep CV charge | Charge |
| 1 | 0 | Charge complete | Charge complete |
| 1 | 1 | Keep CV charge | Charge complete |

During the charging process, the actual charge current may be less than the register setting due to other loop regulations, such as dynamic power management (DPM) regulation (input voltage, input current) or thermal regulation. If the input current ($I_{IN}$) or $V_{IN}$ reach their limits during the CV charge, the charge-full termination is not influenced when the charge current is not as close to the EOC current specification.

A new charge cycle starts once all of the following conditions are valid:

- The input power is recycled
- Battery charging is enabled by the I²C
- Auto-recharge kicks in
- No thermistor fault at NTC
- No safety timer fault
- No battery over-voltage
- BATT FET is not forced to turn off

### Automatic Recharge

When the battery is fully charged and the charging is terminated, the battery may be discharged due to system consumption or self-discharge. When $V_{BATT}$ is discharged below the recharge threshold and $V_{IN}$ is still in the operation range, the IC begins another new charging cycle automatically without having to restart the charging cycle manually.

The auto-recharge function is valid only when EN_TERM = 1 and TERM_TMR = 0.

### Battery Over-Voltage Protection (OVP)

The IC is designed with a built-in battery over-voltage (OV) limit about 130mV above $V_{BATT\_REG}$. When a battery OV event occurs, the IC suspends charging immediately and asserts a fault.

### Input Current and Input Voltage-Based Power Management

To meet the input source (typically USB) maximum current-limit specification, the IC uses input current-based power management by monitoring $I_{IN}$ continuously. The total $I_{IN}$ limit can be programmed via the I²C to prevent the input source from overloading.

If the pre-set $I_{IN}$ limit is greater than the input source rating, back-up $V_{IN}$-based power management also works to prevent the input source from being overloaded. If either the $I_{IN}$ limit or the $V_{IN}$ limit is reached, the Q1 FET between IN and SYS are regulated so that the total input power is limited. As a result, $V_{SYS}$ drops. Once the system declines to the minimum value of 4.56V or $V_{IN}$ -160mV, the charge current is reduced to prevent $V_{SYS}$ from dropping further.

Voltage-based DPM regulates $V_{IN}$ to $V_{IN\_MIN}$ when the load is over the input power capacity. $V_{IN\_MIN}$ set via the I²C should be at least 400mV higher than $V_{BATT\_REG}$ to ensure stable operation of the regulator.

### Battery Supplement Mode

The charge current is reduced to keep the $I_{IN}$ or $V_{IN}$ in regulation when DPM occurs. If the charge current is 0A and the input source is still overloaded due to a heavy system load, then $V_{SYS}$ starts to fall off. Once $V_{SYS}$ falls below $V_{BATT}$, the IC enters battery supplement mode. When $V_{SYS}$ is 30mV below $V_{BATT}$, ideal diode mode is enabled. The battery FET is regulated to maintain $V_{BATT}$ - $V_{SYS}$ at 22.5mV. If the supplement current $I_{DSCHG}$ x $R_{ON\_BATT}$ is above 22.5mV, the battery FET is fully turned on to keep the ideal forward voltage. When the system load decreases, once $V_{SYS}$ exceeds $V_{BATT}$ + 20mV, ideal diode mode is disabled. Figure 6 shows the dynamic power management and battery supplement mode operation profile.

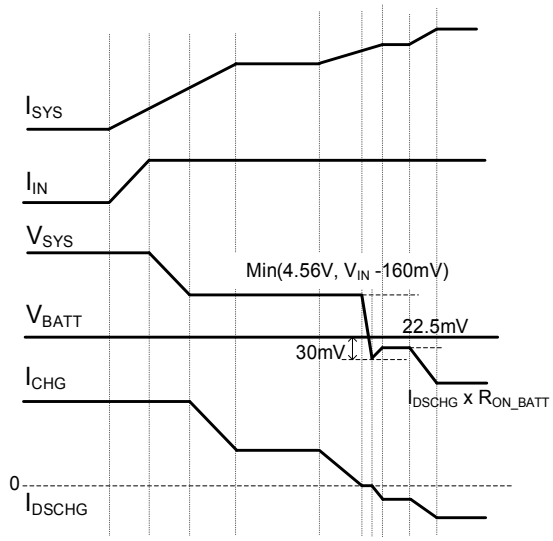



**Figure 6: Dynamic Power Management and Battery Supplement Operation Profile**

When $V_{IN}$ is not available, the IC operates in discharge mode, and the battery FET is always fully on to reduce loss.

### Battery Regulation Voltage

The battery voltage for the constant-voltage regulation phase is $V_{BATT\_REG}$. When $V_{BATT\_REG}$ is 4.2V, it has a ±0.5% accuracy across the ambient temperature range of 0°C to 50°C. When the battery is removed, the battery voltage is between $V_{BATT\_REG}$ - $V_{RECH}$ and $V_{BATT\_REG}$.

### Thermal Regulation and Thermal Shutdown

The IC continuously monitors the internal junction temperature to maximize power delivery and prevent the chip from overheating. When the internal junction temperature reaches the preset limit of $T_{J\_REG}$ (default 120°C), the IC reduces the charge current to prevent higher power dissipation. The multiple thermal regulation thresholds from 60°C to 120°C help the system design meet the thermal requirement in different applications. The junction temperature regulation threshold can be set via REG06h, bits[1:0].

If the junction temperature reaches 150°C, both Q1 and Q2 are turned off.

### Negative Temperature Coefficient (NTC) Temperature Sensor

NTC allows the IC to sense the battery temperature using the thermistor (typically available in the battery pack) to ensure a safe operating environment for the chip. A resistor with an appropriate value should be connected from VDD to NTC, and the thermistor should be connected from NTC to ground. The voltage on NTC is determined by the resistor divider, whose divide ratio depends on the temperature. The IC sets a predetermined upper and lower bound of the divide ratio internally for NTC cold and NTC hot. In the MP2664, the I²C default setting is the PCB OTP. The function can be changed through the I²C (see Table 3).

**Table 3: NTC Function Selection Table**

| I²C Control | | Function |
|---|---|---|
| EN_NTC | EN_PCB OTP | |
| 0 | x | Disabled |
| 1 | 1 | NTC |
| 1 | 0 | PCB OTP |

When PCB OTP is selected, if the NTC voltage ($V_{NTC}$) is below the NTC hot threshold, both the LDO FET and battery FET are turned off. The PCB OTP fault sets the NTC_FAULT status (REG08h, bit[1]) to 1 to indicate the fault. Operation resumes once $V_{NTC}$ exceeds the NTC hot threshold.

The NTC function only works in charge mode. Once $V_{NTC}$ goes out of the divide ratio (the temperature is outside the safe operating range), the IC stops the charging and reports it on the status bits. Charging resumes automatically once the temperature returns to within the safe range.

### Safety Timer

The IC provides both a pre-charge and a fast-charge safety timer to prevent extended charging cycles due to abnormal battery conditions. The safety timer is 1 hour when $V_{BATT}$ is below $V_{BATT\_PRE}$. The fast-charge safety timer begins when the battery enters constant current fast charging. The fast-charge safety timer can be programmed via the I²C. The safety timer feature can be disabled via the I²C.

The following actions can restart the safety timer:

- A new charge cycle is initiated
- Charge enable toggling
- Hi-Z disable toggling

### Host Mode and Default Mode

The IC is a host-controlled device. After the power-on reset (POR), the IC starts in the watchdog timer expiration state or default mode. All of the registers are in the default settings.

Any write to the IC changes it to host mode. All charge parameters are programmable. If the watchdog timer (REG05h, bits[5:4]) is not disabled, the host must reset the watchdog timer regularly by writing 1 to the REG01h, bit[6] before the watchdog timer expires to keep the device in host mode. Once the watchdog timer expires, the IC returns to default mode. The watchdog timer limit can also be programmed or disabled by the host control. When there is no $V_{IN}$, the watchdog timer is suspended (see Figure 19 on page 31).

The operation can also be changed to default mode when one of the following conditions occur:

- Refresh input without battery
- Re-insert battery with no $V_{IN}$
- Register reset REG01h, bit[7] is reset

### Battery Discharge Function

If battery is connected and the input source is missing, the battery FET is fully on once $V_{BATT}$ is above the $V_{BATT\_UVLO}$ threshold. The 100mΩ battery FET minimizes conduction loss during discharge. The quiescent current of the IC is as low as 11μA in this mode. The low on resistance and low quiescent current help extend the running time of the battery.

### Over-Discharge Current Protection

The IC has an over-discharge current protection in discharge mode and supplement mode. Once $I_{BATT}$ exceeds the programmable discharge current limit (default 2A), the battery FET turns off after a 60μs delay, and the MP2664 enters hiccup mode in over-current protection (OCP). The discharge current can be programmed high to 3.2A via the I²C. If the discharge current goes high to reach the internal fixed current limit (about 3.7A), the battery FET is turned off and starts hiccup mode immediately.

Similarly, when $V_{BATT}$ falls below the programmable $V_{BATT\_UVLO}$ threshold (default 2.8V), the battery FET is turned off to prevent over-discharge.

### System Short-Circuit Protection (SCP)

The MP2664 features SYS node short-circuit protection (SCP) for the IN to SYS path and the BATT to SYS path.

$V_{SYS}$ is monitored continuously. If $V_{SYS}$ is below 1.5V, the system (SCP) for the IN to SYS path and the BATT to SYS path are active. $I_{DSCHG}$ is decreased to half of its original value.

1) IN to SYS path: Once $I_{IN}$ exceeds the protection threshold, both the LDO FET and the battery FET are turned off immediately, and the IC enters hiccup mode. Otherwise, the max current limit and the setting input current limit are not reached, and $I_{IN}$ is regulated at $I_{IN\_LIM}$.

Hiccup mode also starts after a 60μs delay. The hiccup mode interval is 800μs.

2) BATT to SYS path: Once $I_{BATT}$ exceeds the 3.7A protection threshold, both the LDO FET and the battery FET are turned off immediately, and the IC enters hiccup mode. When the battery discharge current limit threshold is reached, hiccup mode starts after a 60μs delay. The hiccup mode interval is 800μs.

If a system short-circuit occurs when both the input and battery are present, the protection mechanism of both paths work, with the faster one dominating the hiccup operation (see Figure 22 on page 34).

### Interrupt to Host (INT)

The IC has an alert mechanism that can output an interrupt signal via INT to notify the system of the operation by outputting a 256μs low-state INT pulse. Any of the below events can trigger the INT output:

- Good input source detected(PG_STAT)
- Charge completed
- Charging status change
- Any fault in REG08h (watchdog timer fault, input fault, thermal fault, safety timer fault, battery OVP fault, NTC fault)

When any fault occurs, the IC sends out an INT pulse and latches the fault state in REG08h. After the IC exits the fault state, the fault bit can be released to 0 after the host reads REG08h. The NTC fault is not latched and always reports the current thermistor conditions.

Note that the INT needs the external pull-up resistor for its open-drain connection. The resistance should not be below 300kΩ.

### Battery Disconnect Function

In applications where the battery is not removable, it is essential to disconnect the battery from the system for two reasons: to prevent excessive capacity discharge when the device is in shipping or storage mode, and to allow the system power to reset.

The MP2664 provides both shipping mode and system reset mode for different application requirements.

Register bit FET_DIS (REG06h, bit[5]), allows the IC to enter shipping mode. During normal operation, the battery FET is turned on, and this bit is 0. If this bit is set to 1 via the I²C, the battery FET is turned off and the MP2664 enters shipping mode. The FET_DIS bit is reset to 0 automatically after the battery FET is turned off (see Figure 7).

The IC can exit shipping mode by pulling INT down. When the IC is in shipping mode and only the battery is present, pull INT down by pushing the push button (PB) to wake the MP2664 up from shipping mode (see Table 4 on page 21).

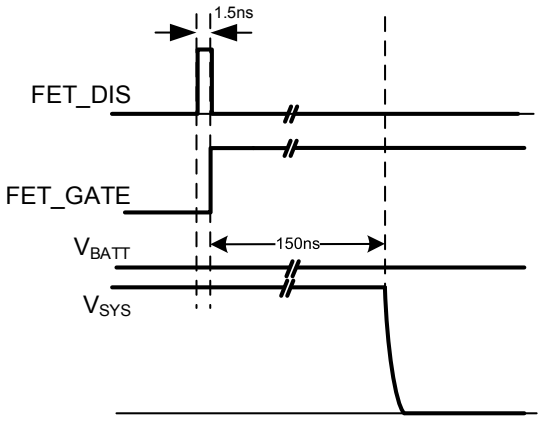



**Figure 7: Time Delay from When FET_DIS Is Written to 1 to the Battery FET Turning Off**

**Table 4: Exit the Shipping Mode with BATT Present Only**

| | INT Signal | IC Exits Shipping Mode |
|---|---|---|
| Case 1 | INT = low twice with the rising edge >600ns | At once |
| Case 2 | INT = low once with the rising edge >600ns | After 4s |
| Case 3 | INT = low for 4s | After 4s |
| Case 4 | INT = low with the rising edge in ms level | At once |

The MP2664 can also wake up from shipping mode when a valid $V_{IN}$ powers on (see Table 5). After $V_{IN}$ is preset, the MP2664 pulls INT low to indicate the event “Good input source detected” if $V_{IN}$ is in the operating range. Then, the MP2664 can be woken up from shipping mode by the INT signal (see Figure 8).

**Table 5: Exiting Shipping Mode when $V_{IN}$ Powers On**

| | INT Signal | IC Exits Shipping Mode |
|---|---|---|
| Case 1 | INT = low twice with the rising edge >600ns | At once |
| Case 2 | INT = low once with the rising edge >600ns | After 4s |
| Case 3 | INT = low with the rising edge in ms level | At once |

If FET_DIS is set to 1 during shipping mode, the IC can wake up after keeping INT low for 4s. In this case, the FET_DIS bit cannot be reset to 0 automatically, it must be reset to 0 manually via the I²C.

The IC can use INT to cut off the path from the battery to the system when a system reset is needed.

Once the logic at INT is set to low for more than 16s, the battery is disconnected from the system by turning off the battery FET.

The off state lasts for 4s, and then the battery FET is turned on automatically. The system is powered by the battery again. During the 4s off period, the INT pin voltage level can be high or low. The IC can reset the system by controlling INT (see Figure 9).

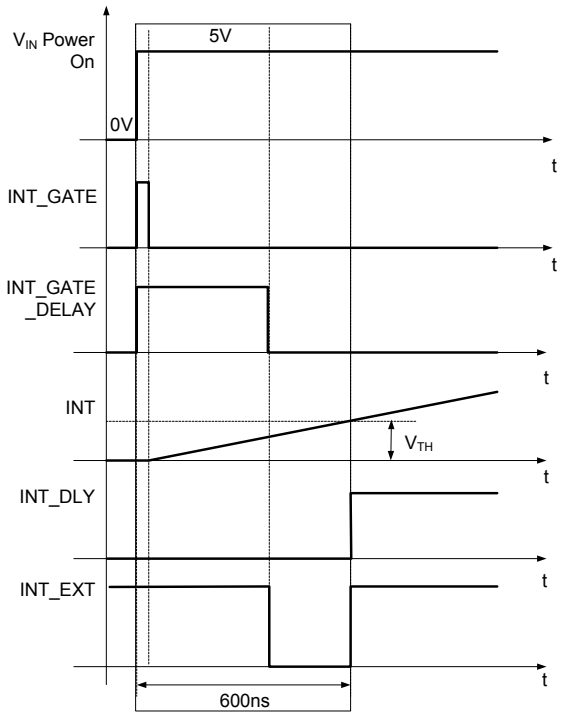



**Figure 8: INT Signal during $V_{IN}$ Power On**

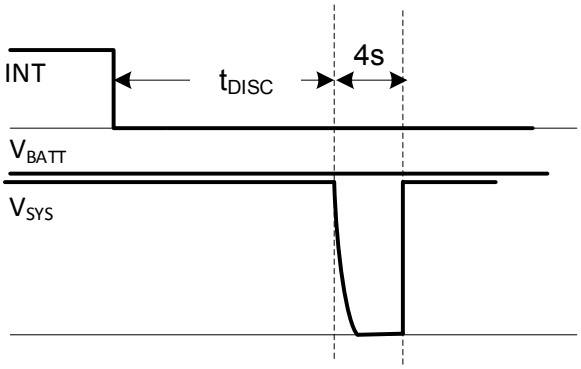



**Figure 9: System Reset Function Operation Profile**

## I²C Serial Interface

The IC uses an I²C serial interface for flexible charging parameter setting and instantaneous device status reporting. The I²C is a two-wire serial interface with two bus lines required: a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL lines are open-drain and need to be connected to the positive supply voltage via a pull-up resistor.

The IC operates as a slave device, receiving control inputs from the master device such as a micro-controller. The SCL line is always driven by the master device. The I²C interface supports both standard mode (up to 100 kbit/s), and fast mode (up to 400 kbit/s).

All transactions begin with a start (S) command and are terminated by a stop (P) command. Start and stop commands are always generated by the master. A high to low transition on the SDA line while SCL is high defines a start command. A low to high transition on the SDA line when the SCL is high defines a stop command.

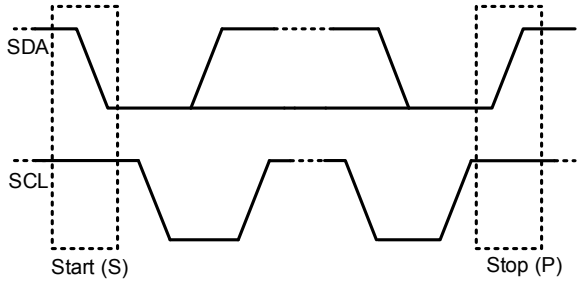



**Figure 10: START and STOP Conditions**

For data validity, the data on the SDA line must be stable during the high period of the clock. The high or low state of the SDA line can only change when the clock signal on the SCL line is low. Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Data is transferred with the most significant bit (MSB) first.

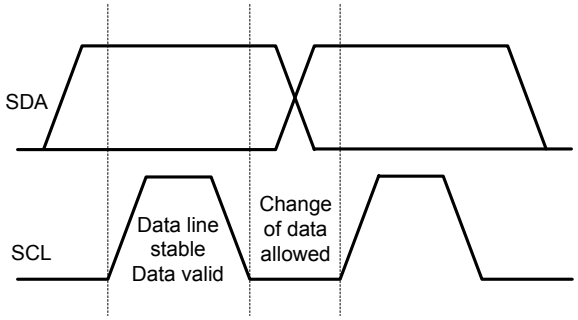



**Figure 11: Bit Transfer on the I²C Bus**

Each byte has to be followed by an acknowledge (ACK) bit, which is generated by the receiver, to signal to the transmitter that the byte was successfully received.

The ACK signal is defined as the transmitter releasing the SDA line during the acknowledge clock pulse so that the receiver can pull the SDA line low. This line remains low during the high period of the 9th clock pulse.

If SDA line is high during the 9th clock pulse, this is defined as the not acknowledge (NACK) signal. The master can then generate either a stop to abort the transfer or a repeated start (Sr) to start a new transfer.

After the start signal, a slave address is sent. This address is 7 bits long, followed by an 8th data direction bit (bit R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). The address bit arrangement is shown below.

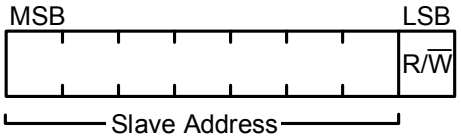



**Figure 12: 7-Bit Address**

See Figure 13, Figure 14, Figure 15, Figure 16, and Figure 17 on page 23 for detailed signal sequences.

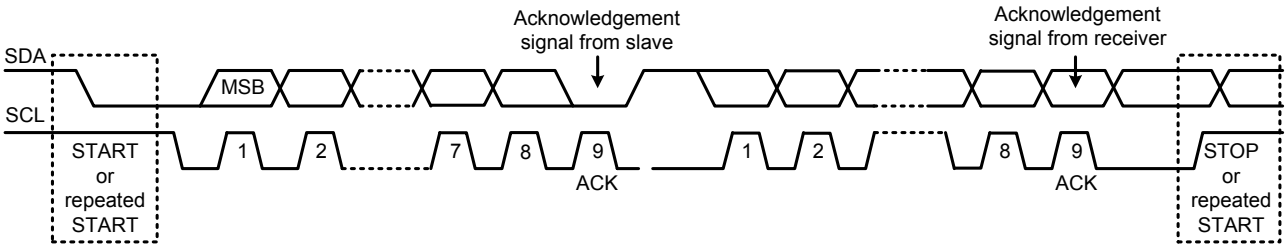



**Figure 13: Data Transfer on the I²C Bus**

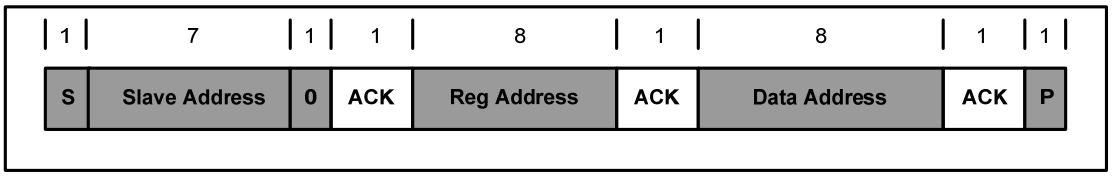



**Figure 14: Single Write**

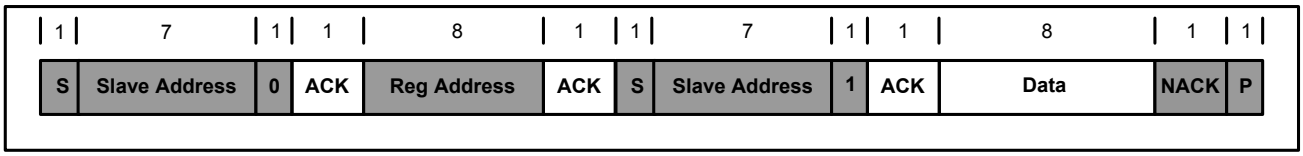



**Figure 15: Single Read**

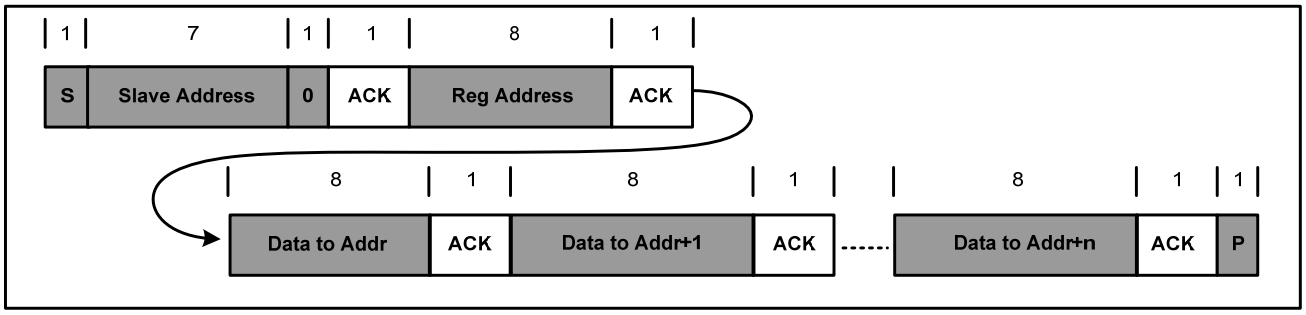



**Figure 16: Multi-Write**


**Figure 17: Multi-Read**

## I²C REGISTER MAP

IC Address: 09h (reserved some trim options)

**Input Source Control Register/Address: 00h (Default: 0100 1111)**

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Bit 7 | EN_HIZ(7) | 0: Disable<br>1: Enable | R/W | Disable (0) |
| Input Minimum Voltage Regulation | | | | |
| Bit 6 | $V_{IN\_MIN}$ [3] | 640mV | R/W | Offset: 3.88V<br>Range: 3.88V - 5.08V<br>Default: 4.60V (1001) |
| Bit 5 | $V_{IN\_MIN}$ [2] | 320mV | | |
| Bit 4 | $V_{IN\_MIN}$ [1] | 160mV | | |
| Bit 3 | $V_{IN\_MIN}$ [0] | 80mV | | |
| Input Current Limit | | | | |
| Bit 2 | $I_{IN\_LIM}$ [2] | 000: 85mA<br>001: 130mA<br>010: 175mA<br>011: 220mA<br>100: 265mA<br>101: 310mA<br>110: 355mA<br>111: 455mA | R/W | 455mA (111) |
| Bit 1 | $I_{IN\_LIM}$ [1] | | | |
| Bit 0 | $I_{IN\_LIM}$ [0] | | | |

**Note:**

7) This bit only controls the on and off of the LDO FET.

**Power-On Configuration Register/Address: 01h (Default: 0000 0100)**

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Bit 7 | Register reset | 0: Keep current setting<br>1: Reset | R/W | Keep current setting (0) |
| Bit 6 | I²C watchdog timer reset | 0: Normal<br>1: Reset | R/W | Normal (0) |
| Bit 5 | Reserved | | R/W | Reserved |
| Bit 4 | Reserved | | R/W | Reserved |
| Charger Configuration | | | | |
| Bit 3 | CEB | 0: Charge enable<br>1: Charge disable | R/W | Charge enable (0) |
| Battery UVLO Threshold | | | | |
| Bit 2 | $V_{BATT\_UVLO}$ [2] | 0.4V | R/W | Offset: 2.4V<br>Range: 2.4V - 3.1V<br>Default: 2.8V (100) |
| Bit 1 | $V_{BATT\_UVLO}$ [1] | 0.2V | | |
| Bit 0 | $V_{BATT\_UVLO}$ [0] | 0.1V | | |

### Charge Current Control Register/Address: 02h (Default: 0000 1110)

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Bit 7 | Reserved | | R/W | Reserved |
| Bit 6 | Reserved | | R/W | Reserved |
| Bit 5 | Reserved | | R/W | Reserved |
| Fast-Charge Current Setting | | | | |
| Bit 4 | $I_{CC}$ [4] | 272mA | R/W | Offset: 8mA<br>Range: 8mA - 535mA<br><br>Default: 246mA (01110) |
| Bit 3 | $I_{CC}$ [3] | 136mA | | |
| Bit 2 | $I_{CC}$ [2] | 68mA | | |
| Bit 1 | $I_{CC}$ [1] | 34mA | | |
| Bit 0 | $I_{CC}$ [0] | 17mA | | |

### Pre-Charge/Termination Current/Address: 03h (Default: 0100 1010)

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Bit 7 | Reserved | | R/W | Reserved |
| BATT to SYS Discharge Current Limit | | | | |
| Bit 6 | $I_{DSCHG}$ [3] | 1600mA | R/W | Offset: 200mA<br>Range: 400mA - 3.2A<br>Valid range: 0001 - 1111<br>Default: 2000mA (1001) |
| Bit 5 | $I_{DSCHG}$ [2] | 800mA | | |
| Bit 4 | $I_{DSCHG}$ [1] | 400mA | | |
| Bit 3 | $I_{DSCHG}$ [0] | 200mA | | |
| PCB OTP Enable | | | | |
| Bit 2 | EN_PCB OTP | 0: Enable<br>1: Disable | R/W | Enable(0) |
| Pre-Charge Current | | | | |
| Bit 1 | $I_{PRE}$ [1] | 14mA | R/W | Offset: 6mA<br>Range: 6mA - 27mA<br>Default: 20mA (10)<br>$I_{PRE}$[1:0] also sets termination current |
| Bit 0 | $I_{PRE}$ [0] | 7mA | | |

### Charge Voltage Control Register/Address: 04h (Default: 1010 0011)

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Battery Regulation Voltage | | | | |
| Bit 7 | $V_{BATT\_REG}$ [5] | 480mV | R/W | Offset: 3.60V<br>Range: 3.60V - 4.545V<br>Default: 4.2V (101000) |
| Bit 6 | $V_{BATT\_REG}$ [4] | 240mV | | |
| Bit 5 | $V_{BATT\_REG}$ [3] | 120mV | | |
| Bit 4 | $V_{BATT\_REG}$ [2] | 60mV | | |
| Bit 3 | $V_{BATT\_REG}$ [1] | 30mV | | |
| Bit 2 | $V_{BATT\_REG}$ [0] | 15mV | | |
| Pre-Charge to Fast Charge Threshold | | | | |
| Bit 1 | $V_{BATT\_PRE}$ | 0: 2.8V<br>1: 3.0V | R/W | 3.0V (1) |
| Battery Recharge Threshold (below $V_{BATT\_REG}$) | | | | |
| Bit 0 | $V_{RECH}$ | 0: 150mV<br>1: 300mV | R/W | 300mV (1) |

### Charge Termination/Timer Control Register/Address: 05h (Default: 0100 1010)

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Bit 7 | Reserved | | R/W | Reserved |
| Termination Setting (the termination is allowed or not) | | | | |
| Bit 6 | EN_TERM | 0: Disable<br>1: Enable | R/W | Enable (1) |
| I²C Watchdog Timer Limit | | | | |
| Bit 5 | WATCHDOG [1] | 00: Disable timer<br>01: 40s<br>10: 80s<br>11: 160s | R/W | Disable timer (00) |
| Bit 4 | WATCHDOG [0] | | | |
| Safety Timer Setting | | | | |
| Bit 3 | EN_TIMER | 0: Disable<br>1: Enable | R/W | Enable timer (1) |
| Fast-Charge Timer | | | | |
| Bit 2 | CHG_TMR [1] | 00: 3hrs<br>01: 5hrs<br>10: 8hrs<br>11: 12hrs | R/W | 5hrs (01) |
| Bit 1 | CHG_TMR [0] | | | |
| Termination Timer Control (when TERM_TMR is enabled, the IC will not suspend the charge current after charge termination) | | | | |
| Bit 0 | TERM_TMR | 0: Disable<br>1: Enable | R/W | Disable (0) |

### Miscellaneous Operation Control Register/Address: 06h (Default: 0100 1011)

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Bit 7 | Reserved | | R/W | Read/write |
| Bit 6 | TMR2X_EN | 0: Disable 2X extended safety timer during PPM<br>1: Enable 2X extended safety timer during PPM | R/W | Enable (1) |
| Bit 5 | FET_DIS (8) | 0: Enable<br>1: Turn off | R/W | Enable (0) |
| Bit 4 | Reserved | | R/W | (0) |
| Bit 3 | EN_NTC | 0: Disable<br>1: Enable | R/W | Enable (1) |
| Bit 2 | Reserved | | R/W | |
| Thermal Regulation Threshold | | | | |
| Bit 1 | $T_{J\_REG}$ [1] | 00: 60°C<br>01: 80°C<br>10: 100°C<br>11: 120°C | R/W | 120°C (11) |
| Bit 0 | $T_{J\_REG}$ [0] | | | |

**Note:**

8) This bit only controls the turn off function of the battery FET, including the charging and discharging.

### System Status Register/Address: 07h (Default: 0000 0000)

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Bit 7 | Reserved | | R | Reserved |
| Revision | | | | |
| Bit 6 | Rev [1] | Revision number | R | (00) |
| Bit 5 | Rev [0] | | | |
| Bit 4 | CHG_STAT [1] | 00: Not charging<br>01: Pre-charge<br>10: Charge<br>11: Charge done | R | Not charging (00) |
| Bit 3 | CHG_STAT [0] | | | |
| Bit 2 | PPM_STAT | 0: No PPM<br>1: In PPM | R | No PPM (0)<br>(no power-path management happens) |
| Bit 1 | PG_STAT | 0: Power fail<br>1: Power good | R | Power fail (0) |
| Bit 0 | THERM_STAT | 0: No thermal regulation<br>1: In thermal regulation | R | No thermal regulation (0) |

**Fault Register/Address: 08h (Default: 0000 0000)**

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Bit 7 | Reserved | | R | Reserved |
| Bit 6 | WATCHDOG_FAULT | 0: Normal<br>1: Watchdog timer expiration | R | Normal (0) |
| Bit 5 | VIN_FAULT | 0: Normal<br>1: Input fault (OVP or bad source) | R | Normal (0) |
| Bit 4 | THEM_SD | 0: Normal<br>1: Thermal shutdown | R | Normal (0) |
| Bit 3 | BAT_FAULT | 0: Normal<br>1: Battery OVP | R | Normal (0) |
| Bit 2 | STMR_FAULT | 0: Normal<br>1: Safety timer expiration | R | Normal (0) |
| Bit 1 | NTC_FAULT [1] | 0: Normal<br>1: NTC hot | R | Normal (0) |
| Bit 0 | NTC_FAULT [0] | 0: Normal<br>1: NTC cold | R | Normal (0) |

## ONE-TIME PROGRAMMABLE MAP

| # | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|
| 0x02 | N/A | | | $I_{CC}$: 8mA - 535mA / 17mA step | | | | |
| 0x03 | N/A | | | | | EN_PCB_OTP | $I_{PRE}$ | |
| 0x04 | $V_{BATT\_REG}$: 3.6V - 4.545V / 15mV step | | | | | | N/A | |
| 0x05 | N/A | | WATCHDOG | | N/A | | | |

## ONE-TIME PROGRAMMABLE DEFAULT

| One-Time Programmable Items | Default |
|---|---|
| $I_{CC}$ | 246mA |
| $I_{PRE}$ | 20mA |
| $V_{BATT\_REG}$ | 4.2V |
| WATCHDOG | Disable timer |
| EN_PCB OTP | Enable |

## STATE CONVERSION CHART

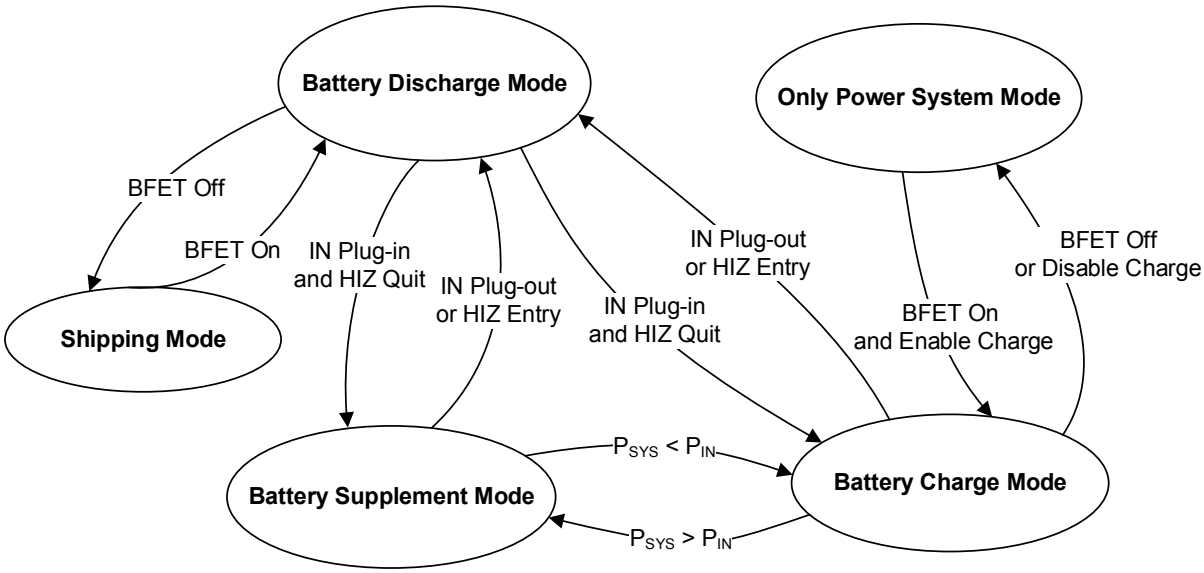



**Figure 18: State Machine Conversion Chart**

## CONTROL FLOWCHART

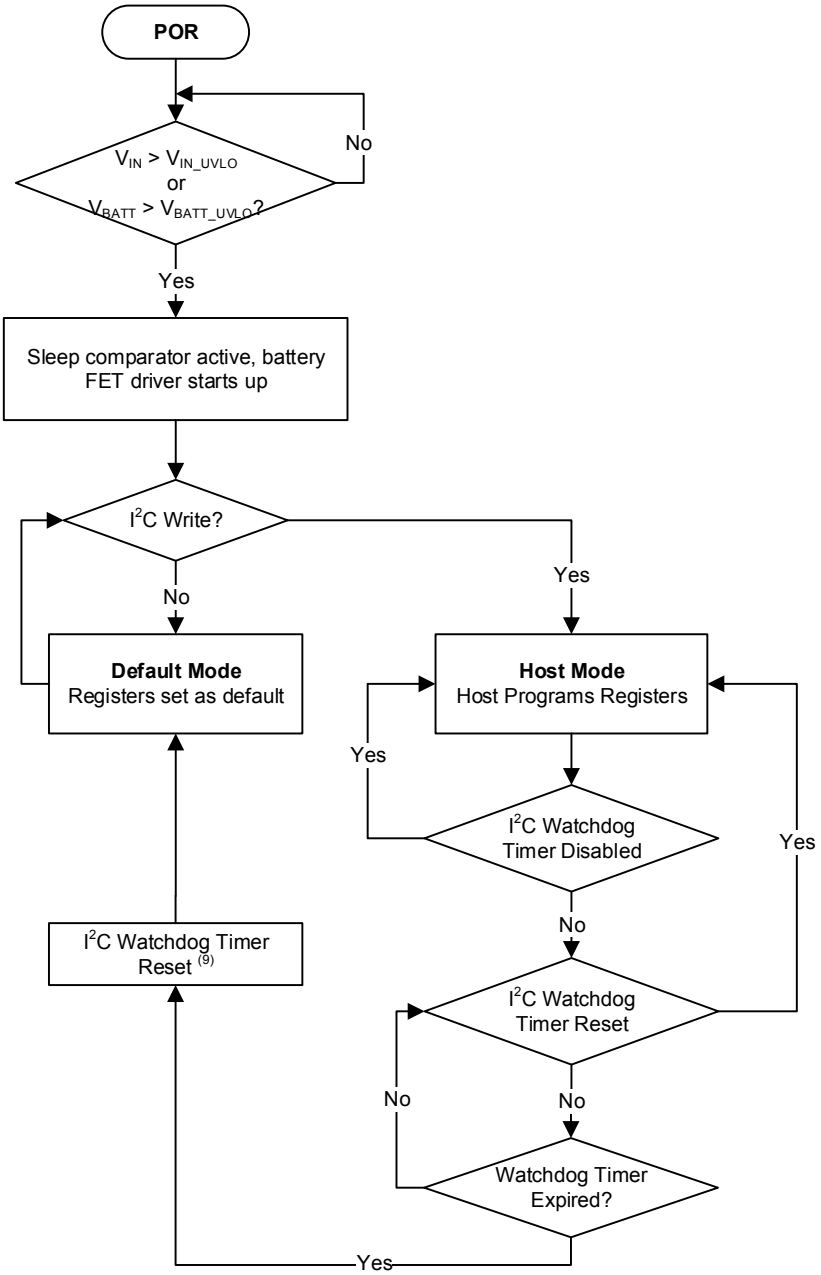



**Figure 19: Default Mode and Host Mode Selection** (10)

**Notes:**

9) Once the watchdog timer expires, the I²C watchdog timer must be reset, or the watchdog timer will not be valid in the next cycle.
10) The watchdog timer is held when $V_{IN}$ is not present.

## CONTROL FLOWCHART *(continued)*

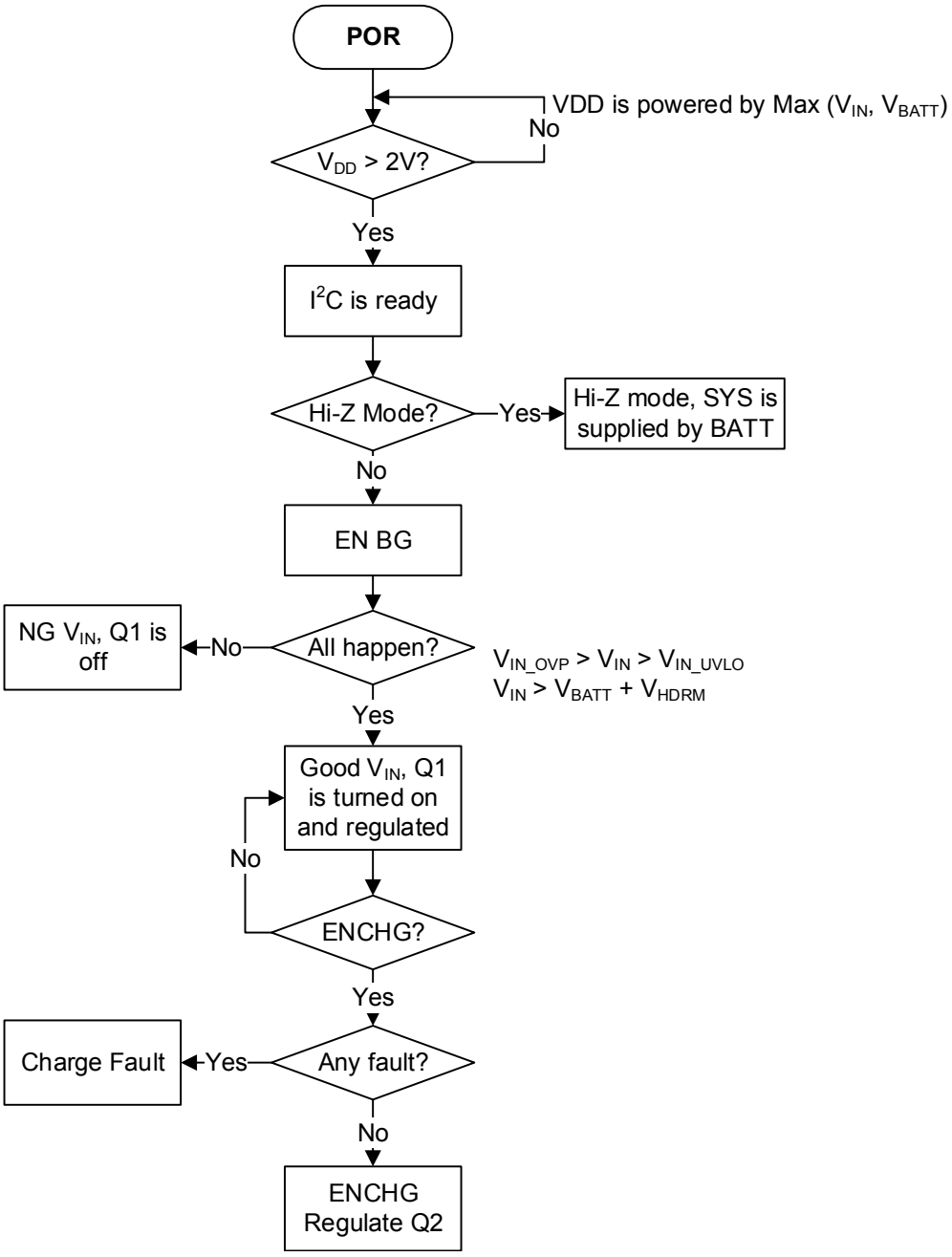



**Figure 20: Input Power Start-Up Flowchart**

## CONTROL FLOWCHART *(continued)*

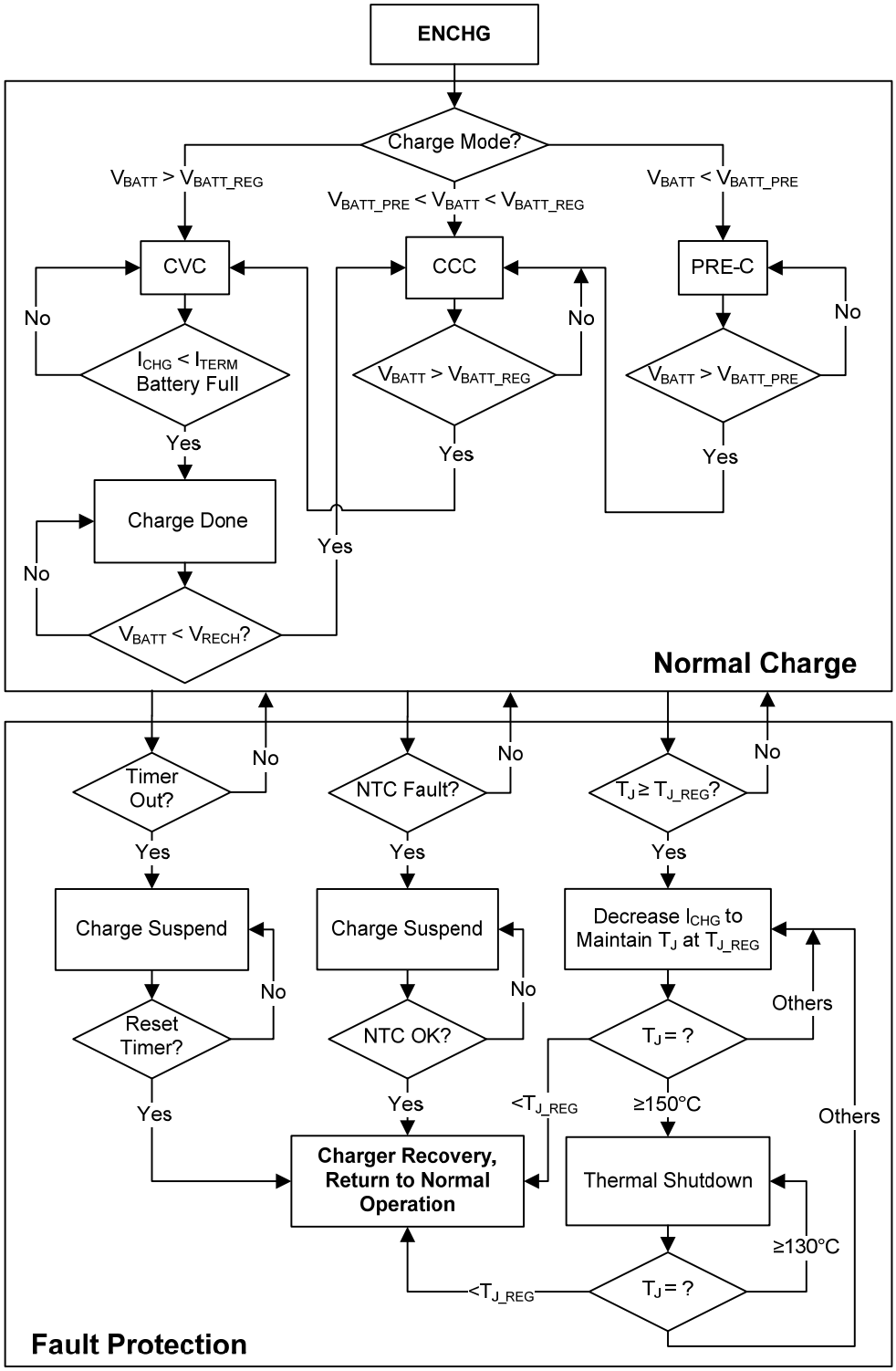



**Figure 21: Charging Process**

## CONTROL FLOWCHART *(continued)*

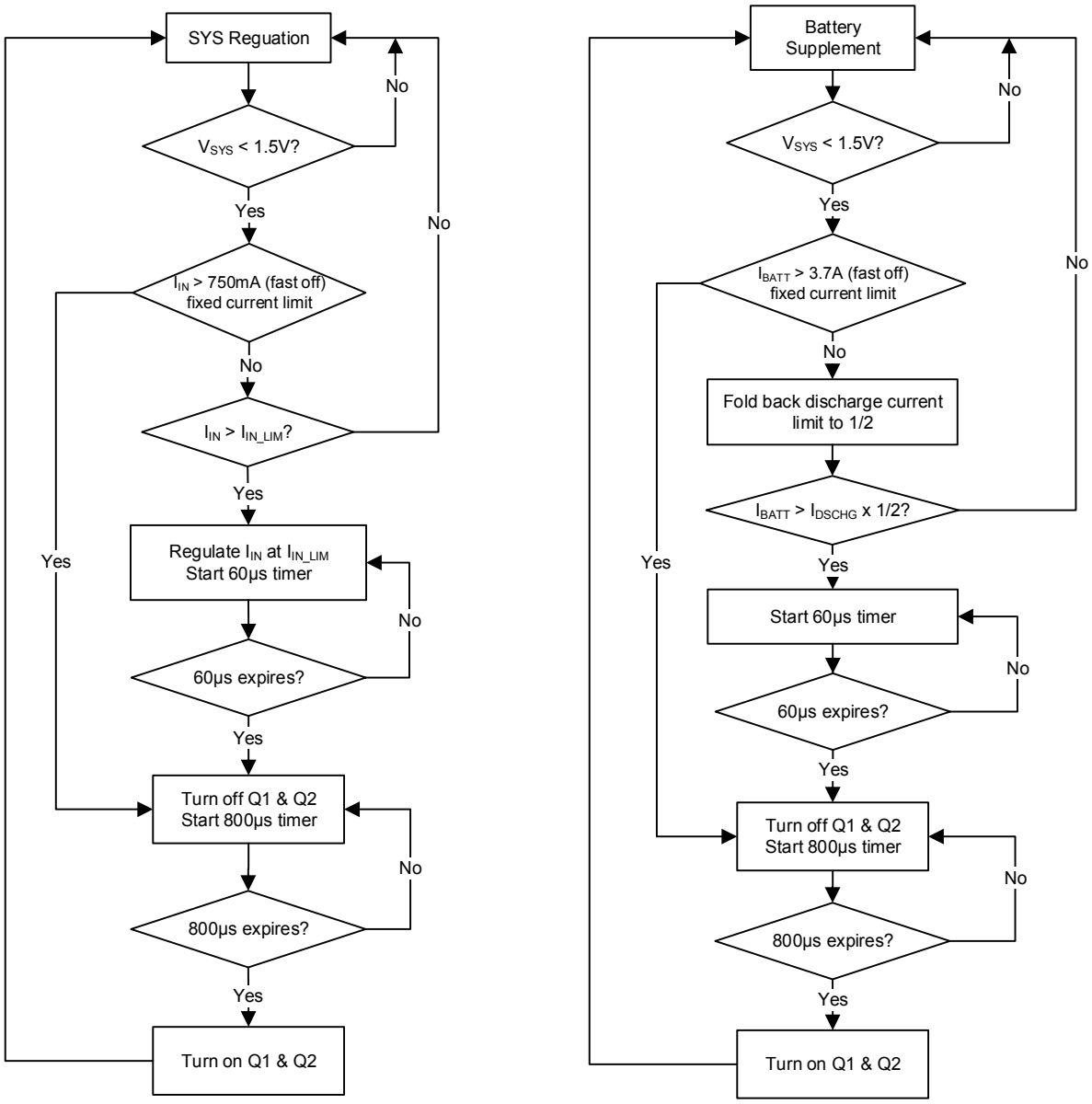



**Figure 22: System Short-Circuit Protection**

# APPLICATION INFORMATION

### Selecting a Resistor for the NTC Sensor

NTC uses a resistor divider from the input source (VDD) to sense the battery temperature. The two resistors ($R_{T1}$ and $R_{T2}$) allow the high temperature limit and low temperature limit to be programmed independently (see Figure 23). In other words, the IC can fit most types of NTC resistors and different temperature operation range requirements with the two extra resistors.

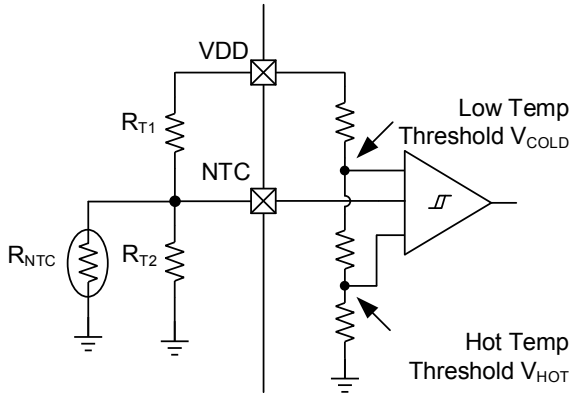



**Figure 23: NTC Function Block**

For a given NTC thermistor, $R_{T1}$ and $R_{T2}$ depend on the type of NTC resistor used. $R_{T2}$ can be calculated with Equation (1):

$$R_{T2} = \frac{(V_{COLD} - V_{HOT}) \times R_{NTCH} \times R_{NTCL}}{(V_{HOT} - V_{COLD}V_{HOT}) \times R_{NTCL} - (V_{COLD} - V_{COLD}V_{HOT}) \times R_{NTCH}} \quad (1)$$

$R_{T1}$ can be calculated with Equation (2):

$$R_{T1} = \frac{1\text{-}V_{COLD}}{V_{COLD}} \times (R_{T2} // R_{NTCL}) \quad (2)$$

Where $R_{NTCH}$ is the value of the NTC resistor at the high temperature of the required temperature operating range, and $R_{NTCL}$ is the value of the NTC resistor at a low temperature.

For example, for thermistor NCP18XH103, $R_{NTCL}$ is 27.219kΩ at 0°C, and $R_{NTCH}$ is 4.161kΩ at 50°C. Equation (1) and Equation (2) determine that $R_{T1}$ = 7.33kΩ and $R_{T2}$ = 27.22kΩ (assuming that the NTC window is between 0°C and 50°C and using the $V_{COLD}$ and $V_{HOT}$ values from the EC table).

### Selecting the External Capacitor

Like most low-dropout regulators, the MP2664 requires external capacitors for regulator stability and voltage spike immunity. The MP2664 is designed specifically for portable applications requiring a minimal board space and small components. These capacitors must be selected correctly for optimal performance.

An input capacitor is required for stability. Connect a 1µF (minimum) capacitor between IN and GND for stable operation over the entire load current range. There can be more output capacitance than input as long as the input is at least 1µF.

The IC is designed specifically to work with a very small ceramic output capacitor. A 10µF ceramic capacitor with X5R or X7R type dielectrics is suitable in the MP2664 application circuit. For the MP2664, the output capacitor should be connected between SYS and GND with thick traces and a small loop area.

A capacitor from BATT to GND is necessary for the MP2664. A 4.7µF ceramic capacitor with X5R or X7R type dielectrics is suitable for the application circuit.

A capacitor between VDD and GND is used to stabilize the VDD voltage to power the internal control and logic circuit. The typical value of this capacitor is 100nF.

## PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 24 and follow the guidelines below:

1. Place the external capacitors as close to the IC as possible to reduce input inductance and ground impedance.
2. Place the PCB trace connected between the VDD and GND pins close to the IC.
3. Keep the I²C wire ground clean, and away from the GND pin.
4. Place the I²C wires (SCL and SDA) in parallel.

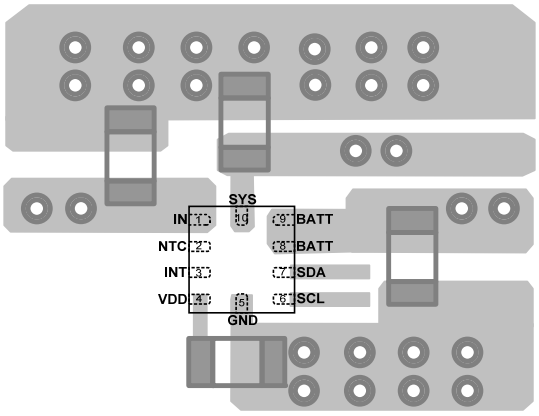



**Figure 24: Recommended PCB Layout**

## TYPICAL APPLICATION CIRCUIT

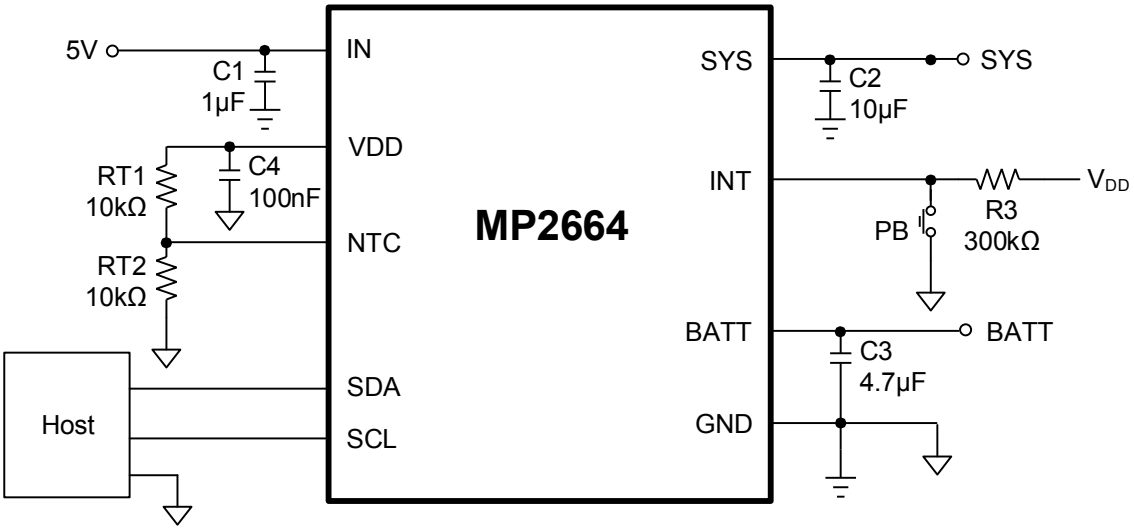


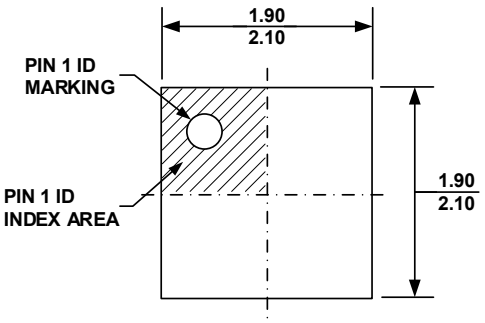

**Figure 25: MP2664 Typical Application Circuit with a 5V Input**

**Table 6: Bill of Materials Key for Figure 25**

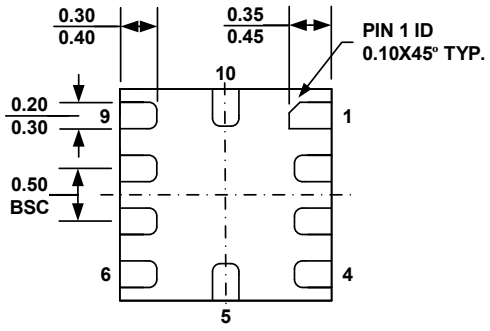
| Qty | Ref | Value | Description | Package | Manufacturer |
|---|---|---|---|---|---|
| 1 | C1 | 1µF | Ceramic capacitor, 16V, X5R or X7R | 0603 | Any |
| 1 | C2 | 10µF | Ceramic capacitor, 16V, X5R or X7R | 0603 | Any |
| 1 | C3 | 4.7µF | Ceramic capacitor, 16V, X5R or X7R | 0603 | Any |
| 1 | C4 | 100nF | Ceramic capacitor, 16V, X5R or X7R | 0603 | Any |

# PACKAGE INFORMATION

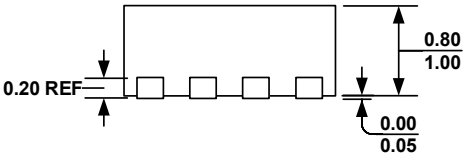
## QFN-10 (2mmx2mm)



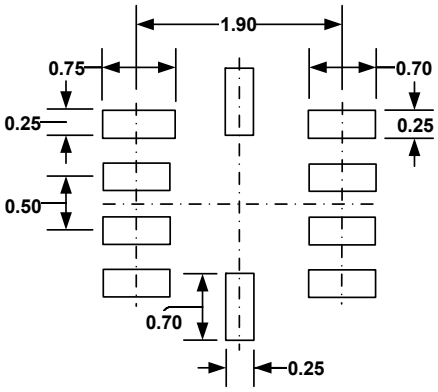

TOP VIEW




BOTTOM VIEW




SIDE VIEW




RECOMMENDED LAND PATTERN

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.1 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220, VARIATION VCCD.
5) DRAWING IS NOT TO SCALE.

## REVISION HISTORY

| Revision # | Revision Date | Description | Pages Updated |
|---|---|---|---|
| 1.0 | 10/10/2018 | Initial release | - |
| 1.1 | 6/3/2021 | Updated the Pin Functions section | 4 |
| | | Updated “CE = L” to “CEB = 0” and “CE = H” to “CEB = 1” | 6–8 |
| | | Updated the Operation sections | 15–21 |
| | | Updated Table 2 | 17 |
| | | Added the Series Interface section | 22–23 |
| | | Updated Figures 18–22 | 30–34 |
| | | Updated Equation 1 and Equation 2 introductions | 35 |
| | | Added PCB Layout Guidelines section | 36 |
| | | Formatting and clerical updates; updated headers and footers; updated figure titles | All |

# X-ON Electronics

Largest Supplier of Electrical and Electronic Components

***Click to view similar products for*** Battery Management ***category:***

***Click to view products by*** Monolithic Power Systems ***manufacturer:***

Other Similar products are found below :

NCP1851BFCCT1G NCP1855FCCT1G FAN54063UCX MP2615GQ-P LC05132C01NMTTTG ISL95522HRZ BD8665GW-E2 ISL9538HRTZ ISL95522AIRZ S-82D1AAA-A8T2U7 S-8224ABA-I8T1U MP2615CGQ-P ISL6251HRZ ISL6253HRZ ISL6292-2CR3 ISL6292BCRZ-T ISL6299AIRZ ISL9211AIRU58XZ-T ISL9214IRZ ISL9220IRTZ-T FAN54161UCX SY6982CQDC IP6566_AC_30W_ZM WS3221C-6/TR ADBMS1818ASWAZ-RL ADBMS6815WCSWZ ML5245-005AMBZ07CX BQ25672RQMR ADBMS1818ASWZ-R7 KA49503A-BB SC33771CTA1MAE BQ24060DRCR BQ7695202PFBR BQ21080YBGR BQ771809DPJR BQ24179YBGR BQ7693002DBTR BQ25170DSGR TP4586 FM2119L FM1623A DW01 BQ25172DSGR DW01S TP4054 MP2723GQC-0000-Z MP26124GR-Z MP2664GG-0000-Z MP26029GTF-0000-Z MP2695GQ-0000-Z