MP28310

300mA, 2V to 5.5V, 500nA I_Q, Step-Down Converter with 300nA I_Q, 2V to 5.5V, 100mA LDO Regulator in CSP-12 (1.2mmx1.6mm)

DESCRIPTION

The MP28310 is a monolithic power management unit containing a 300mA, high-efficiency, switching step-down converter and a 100mA low-dropout (LDO) regulator. The ultra-low 500nA quiescent current (I_Q) provides extremely high efficiency when the load current is within the µA range. The MP28310's low 2V minimum input voltage allows the system to operate directly from the battery.

Constant-on-time (COT) control provides fast transient response and high light-load efficiency, and requires minimal capacitance. Good regulation is achieved by integrating an error amplifier (EA) to correct the output voltage (V_{OUT}).

The 100mA LDO regulator provides easy system configuration and a clean V_{OUT}. The control (CTRL) pins control the on/off and V_{OUT} selection functions.

Fault protection features include under-voltage lockout (UVLO), over-current protection (OCP), and thermal shutdown.

The MP28310 requires a minimal number of readily available, standard external components, and is available in a small CSP-12 (1.2mmx1.6mm) package.

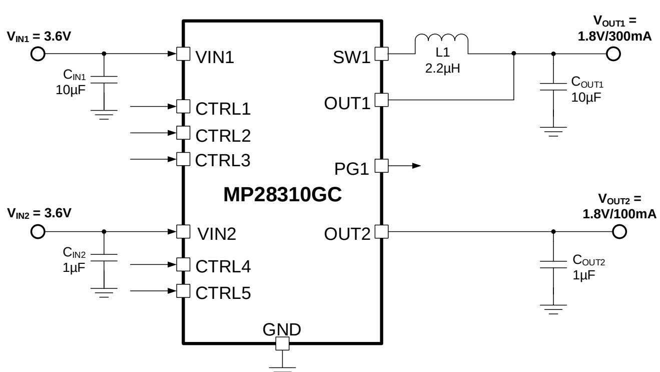
FEATURES

- **300mA Buck Converter**
  - Ultra-Low 500nA Quiescent Current (I_Q)
  - Wide 2V to 5.5V Operating Input Range
  - 7 Selectable Output Voltages
  - Up to 300mA of Output Current
  - 1.5MHz Switching Frequency in Continuous Conduction Mode (CCM)
  - 100% Duty Cycle in Low-Dropout Mode
  - 0.25Ω and 0.25Ω Internal Power MOSFET Switches
  - Cycle-by-Cycle Over-Current Protection (OCP)
  - Short-Circuit Protection (SCP) with Hiccup Mode
- **100mA LDO**
  - Ultra-Low 300nA I_Q
  - 2V to 5.5V Operating Input Range
  - 3 Selectable Output Voltages
  - Over-Temperature Protection (OTP)
- Available in a CSP-12 (1.2mmx1.6mm) Package

APPLICATIONS

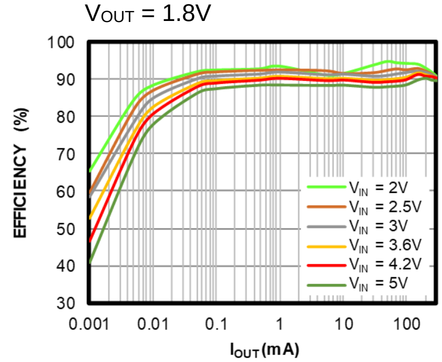
- Wearables
- Internet of Things (IoT)
- Portable Instruments
- Battery-Powered Devices

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 1.8V



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP28310GC	CSP-12 (1.2mmx1.6mm)	*See Below*	1

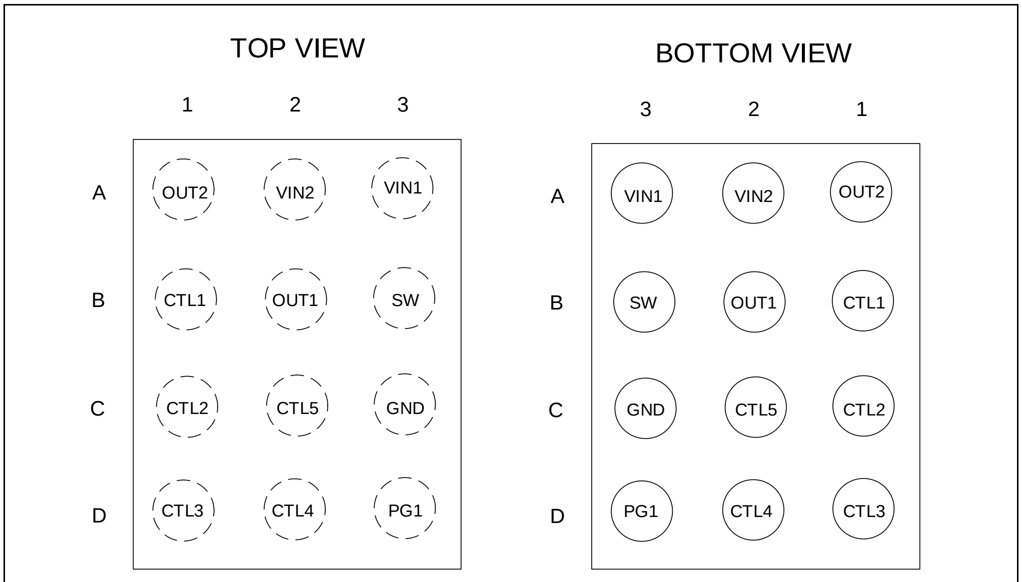
* For Tape & Reel, add suffix –Z (e.g. MP28310GC–Z).

TOP MARKING

FAY
LLL

FA: Product code of MP28310GC
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



CSP-12 (1.2mmx1.6mm)

PIN FUNCTIONS

Pin #	Name	Description
A1	OUT2	**LDO output voltage sensor.** OUT2 is the output of the linear regulator. Use a 1μF output capacitor to bypass OUT2 to GND.
A2	VIN2	**LDO input supply voltage.** Place a small decoupling capacitor as close to VIN2 and GND as possible.
A3	VIN1	**Step-down converter input supply voltage.** Place a small decoupling capacitor as close to VIN1 and GND as possible.
B1	CTL1	**Step-down converter control signal (CTL means CTRL).** These pins dynamically adjust the step-down converter's output voltage (V_{OUT}). Do not float the CTRL pins. When used, ensure that the CTRL voltage is above the input voltage (V_{IN}). If unused, tie the CTRL pin(s) to GND. See Table 1 on page 15 to set the buck output value.
C1	CTL2	
D1	CTL3	
D2	CTL4	**LDO control signal (CTL means CTRL).** These pins dynamically adjust the LDO V_{OUT}. Do not float the CTRL pins. When used, ensure that the CTRL voltage is above V_{IN}. If unused, tie the CTRL pin(s) to GND. See Table 1 on page 15 to set the LDO output value.
C2	CTL5	
C3	GND	**Ground.**
D3	PG1	**Step-down converter power good (PG) indicator.** PG1 is an open-drain output.
B2	OUT1	**Step-down converter output voltage sensor.** Connect the load to OUT1. Use an output capacitor to reduce the output voltage ripple.
B3	SW	**Step-down converter switch output.** SW is the drain of the internal high-side MOSFET (HS-FET). Connect the inductor to SW to complete the converter.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage ($V_{IN1/2}$) 6V
V_{SW1}.................................... -0.3V to VIN + 0.3V
.....................................-0.3V (-5V for <10ns) to +6V (8V for <10ns or 10V for <3ns)
All other pins .... -0.3V to +6V
Continuous power dissipation (T_A = +25°C) (2)(4)
EV28310-C-00A..................................... 2.27W
Junction temperature .... 150°C
Lead temperature .... 260°C
Storage temperature .... -65°C to +150°C

ESD Ratings

Human body model (HBM) 2000V
Charged device model (CDM) .... ±1750V

Recommended Operating Conditions (3)

Supply voltage ($V_{IN1/2}$) .... 2.0V to 5.5V
Operating junction temp (T_J) ... -40°C to +125°C

Thermal Resistance

Thermal Resistance	θ_{JA}	θ_{JC}	
EV28310-C-00A (4)	55	8.2	°C/W
CSP-12 (1.2mmx1.6mm) (5)	95	30	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation may produce an excessive die temperature, which can cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV28310-C-00A, 2-layer, 63mmx63mm PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN1} = 3.6V, V_{IN2} = 3.6V, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C. The limit over-temperature is guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Buck Converter						
Input voltage range	V_{IN1}		2		5.5	V
Buck under-voltage lockout (UVLO) rising threshold	$V_{IN1\_UVLO\_R}$		1.65	1.8	1.95	V
Buck UVLO threshold hysteresis	$V_{IN1\_UVLO\_H}$			150		mV
Shutdown supply current	I_{SD_25}	CTRL1/2/3 = 0V, or EN = 0		70		nA
Quiescent supply current	I_{Q_BUCK}	No load, CTRL4/5 = 0V, CTRL1/2/3 = H/H/L, OUT1 = 1.8V, no switching		500		nA
High-side MOSFET (HS-FET) switch on resistance	$R_{DS(ON)1\_H}$			0.25		Ω
Low-side MOSFET (LS-FET) switch on resistance	$R_{DS(ON)1\_L}$			0.25		Ω
Switch leakage current	I_{LK_SW1}	CTRL1/2/3 = 0V, V_{IN1} = 5.5V, V_{SW} = 0V and 5.5V, T_J = 25°C	-100	0	+100	nA
HS-FET current limit	I_{LIM1_H}		480	600	720	mA
LS-FET valley source current	I_{LIMV1_L}		300	400		mA
LS-FET zero-current detection	I_{ZCD}		0	20		mA
On time	t_{ON}	V_{IN1} = 3.6V, V_{OUT} = 1.8V	280	330	380	ns
LDO input voltage range	V_{IN2}	When V_{IN1} > V_{IN1_UVLO}	2.0		5.5	V
Minimum on time	t_{MIN_ON}			60		ns
Minimum off time	t_{MIN_OFF}			100		ns
Maximum duty cycle (7)	D_{MAX}		100			%
Output voltage accuracy	V_{OUT}	CTRL1/2/3 = H/H/L, T_J = 25°C, I_{OUT} = 0.1A	1.782	1.8	1.818	V
		CTRL1/2/3 = H/H/L, T_J = -40°C to +85°C, I_{OUT} = 0.1A	1.773		1.827	
Buck line-load regulation (7)		From 2.5V to 5.5V, from 0A to 300mA	-1		+1	%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = 3.6V, V_{IN2} = 3.6V, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C. The limit over-temperature is guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
LDO						
Quiescent supply current	I_{Q_LDO}	No load, CTRL1/2/3 = 0V, CTRL4/5 = H/L, no load current from V_{IN2}		300		nA
Shutdown supply current	I_{SD_25}	CTRL4/5 = 0V, or EN = 0		50		nA
LDO voltage dropout	V_{DP}	I_{LDO} = 0.1A, V_{OUT} = 3.3V		50		mV
LDO current limit	I_{LIM_LDO}		150	200		mA
DC output voltage accuracy	V_{OUT}	CTRL4/5 = H/L, T_J = 25°C	1.782	1.8	1.818	V
		CTRL4/5 = H/L, T_J = -40°C to +85°C	1.773		1.827	
		Internal reference, T_A = -40°C to +85°C	0.591	0.6	0.609	
LDO line regulation		I_{OUT} = 1mA		0		%
LDO load regulation		I_{OUT} = 1mA to 100mA	-1		+1	%
Power supply rejection ratio (7)	PSRR	10Hz, I_{OUT} = 100mA		40		dB
		100Hz, I_{OUT} = 100mA		20		
		1kHz, I_{OUT} = 100mA		15		
Buck and LDO						
Internal soft-start time	t_{SS}	Buck		0.5		ms
	t_{SS}	LDO: V_{OUT} = 3.3V, I_{OUT} = 100mA, C_{OUT} = 1µF		2		ms
Discharge resistance during shutdown	R_{DIS_OFF}			50		Ω
Control (CTRL) high logic	$CTRL_H$		1.2			V
CTRL low logic	$CTRL_L$				0.4	V
CTRL input current	I_{CTRL}	V_{CTRL} = 3.6V		1		nA
		V_{CTRL} = 0		0		
		V_{EN} = 0V		0		
CTRL turn-on delay	t_D			300		µs
CTRL pull-down resistor	R_{PD}	Not present when CTRL is high to avoid I_Q impact		2		MΩ
Power good (PG) threshold	PG	Feedback with respect to the regulation		90		%
PG hysteresis	PG_{HYS}			10		%
PG delay	PG_{TD}			75		µs
PG sink current capability	V_{PG_LO}	Sink 1mA			0.4	V
PG leakage current	I_{PGLK}	V_{PGBUS} = 1.8V			10	nA
Thermal shutdown (7)	T_{SD}			150		°C
Thermal hysteresis (7)	T_{SDHY}			30		°C

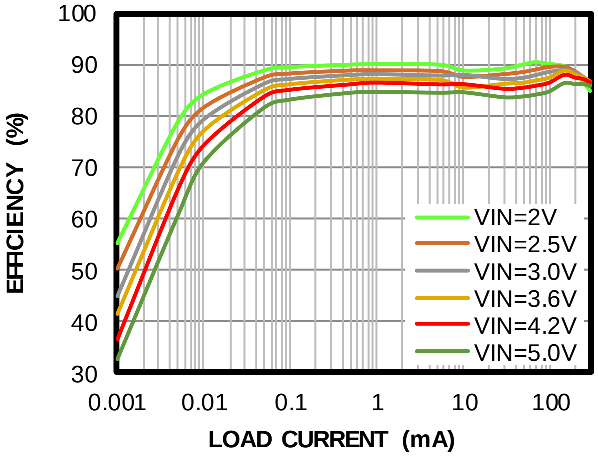
Notes:

6) Not tested in production. Guaranteed by over-temperature correlation.
7) Guaranteed by engineering sample characterization.

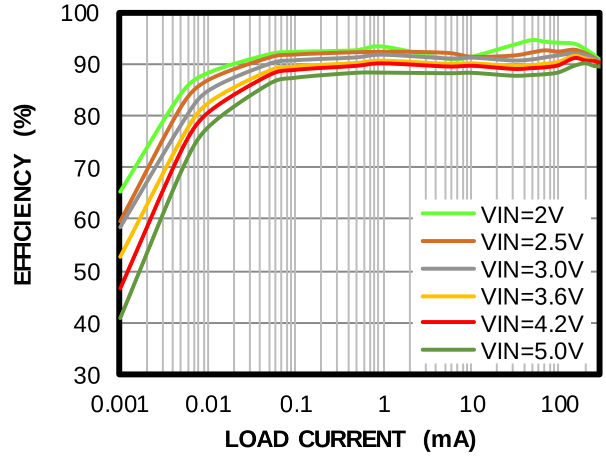
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN1} = 3.6V, V_{OUT1} = 1.8V, L_1 = 2.2µH, C_{IN1} = 10µF, C_{OUT1} = 10µF, V_{IN2} = 3.6V, V_{OUT2} = 1.8V, C_{IN2} = 1µF, C_{OUT2} = 1µF, T_A = 25°C, unless otherwise noted.

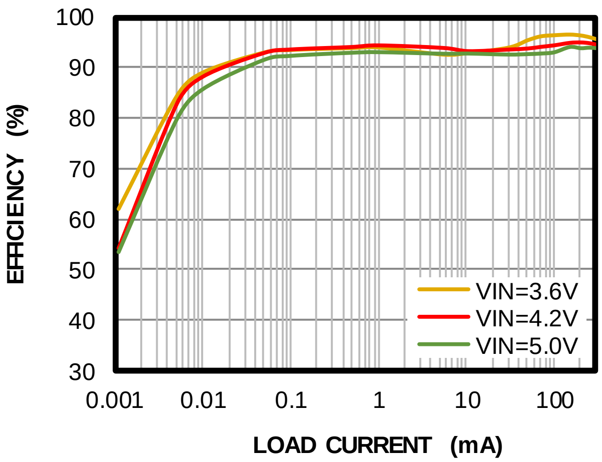
Efficiency vs. Load Current
V_{OUT} = 1.2V



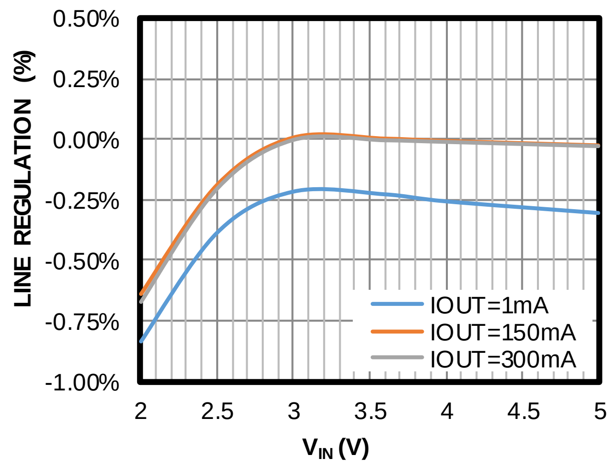
Efficiency vs. Load Current
V_{OUT} = 1.8V



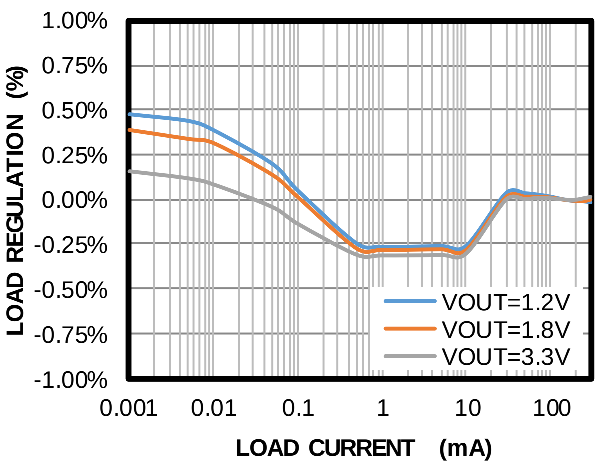
Efficiency vs. Load Current
V_{OUT} = 3.3V



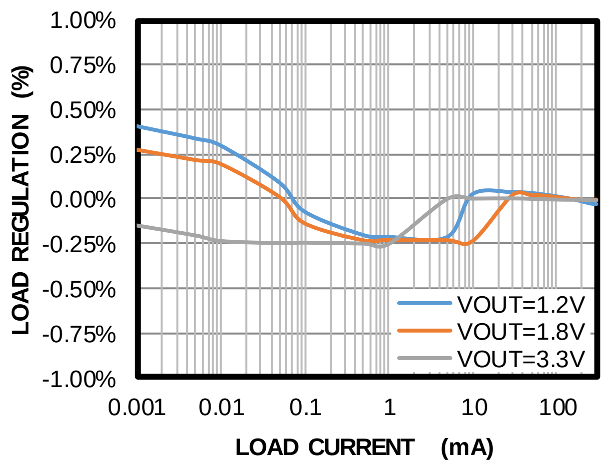
Line Regulation vs. V_{IN}



Load Regulation vs. Load Current
V_{IN} = 5V



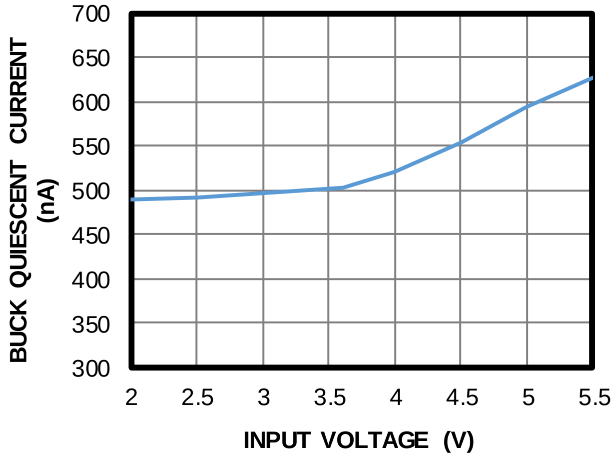
Load Regulation vs. Load Current



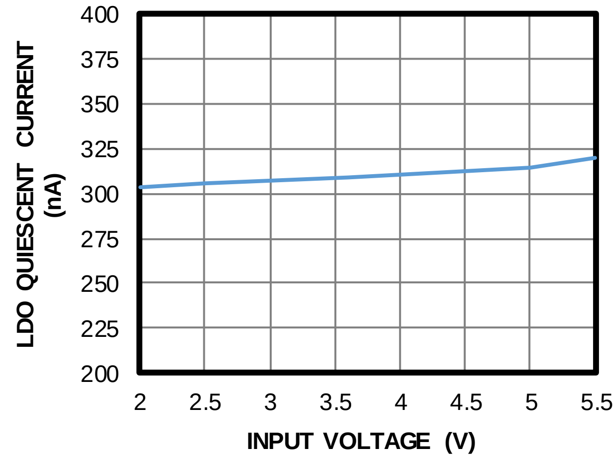
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 3.6V, V_{OUT1} = 1.8V, L_1 = 2.2µH, C_{IN1} = 10µF, C_{OUT1} = 10µF, V_{IN2} = 3.6V, V_{OUT2} = 1.8V, C_{IN2} = 1µF, C_{OUT2} = 1µF, T_A = 25°C, unless otherwise noted.

Buck Quiescent Current vs. V_{IN}

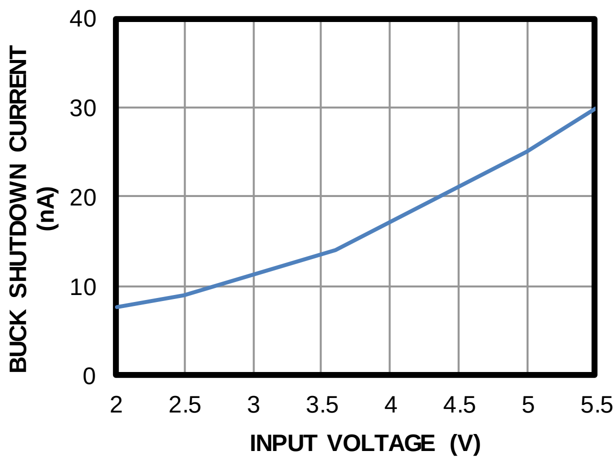


LDO Quiescent Current vs V_{IN}



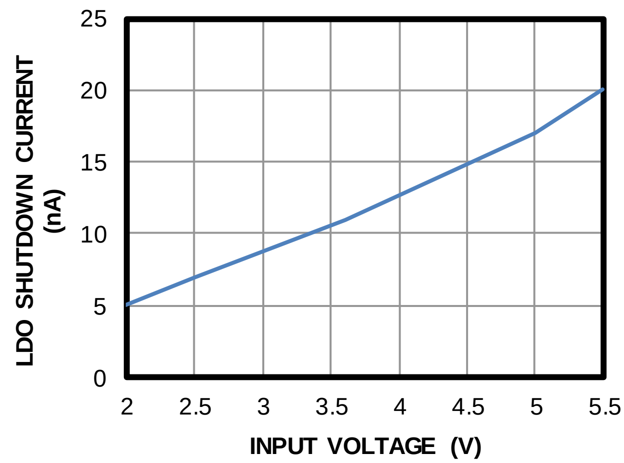
Buck Shutdown Current vs. V_{IN}

CTRL1/2/3 = 0V

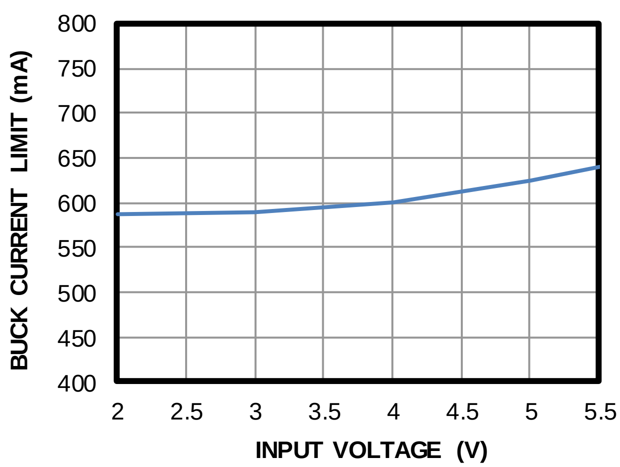


LDO Shutdown Current vs. V_{IN}

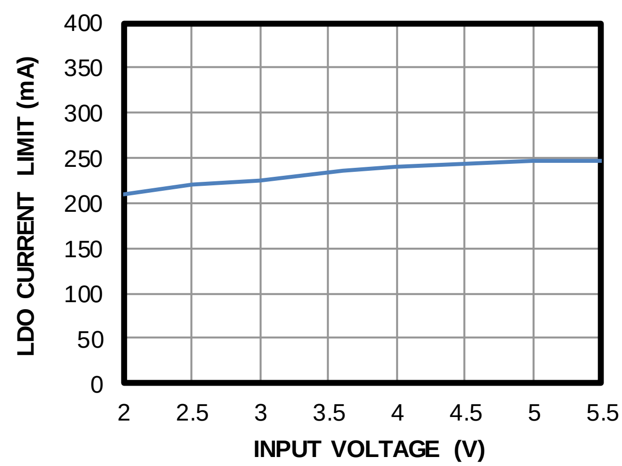
CTRL4/5 = 0V



Buck Current Limit vs. V_{IN}



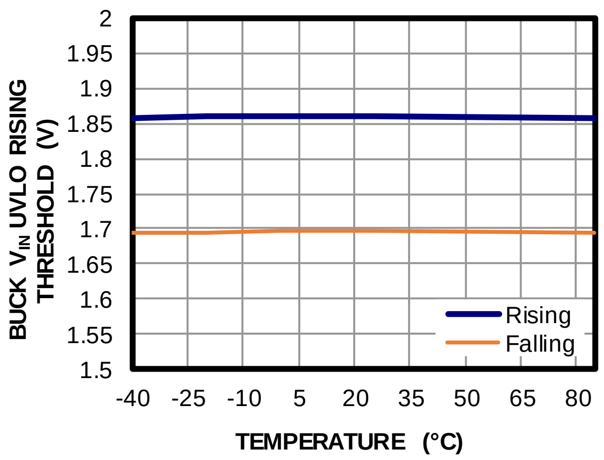
LDO Current Limit vs. V_{IN}



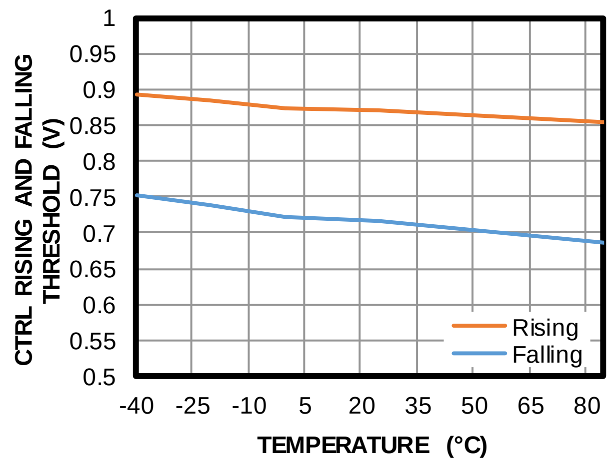
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 3.6V, V_{OUT1} = 1.8V, L_1 = 2.2µH, C_{IN1} = 10µF, C_{OUT1} = 10µF, V_{IN2} = 3.6V, V_{OUT2} = 1.8V, C_{IN2} = 1µF, C_{OUT2} = 1µF, T_A = 25°C, unless otherwise noted.

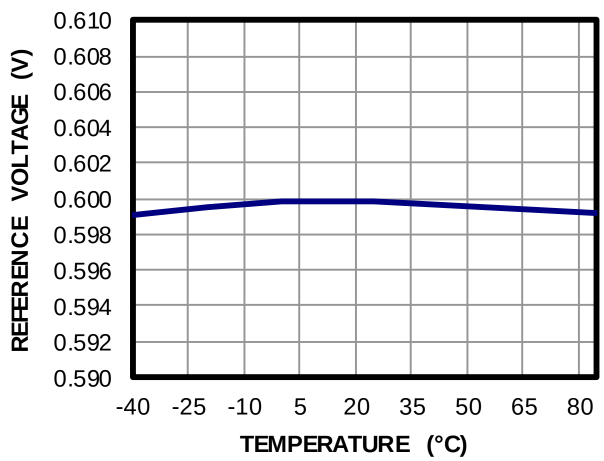
Buck V_{IN} UVLO Rising Threshold vs. Temp



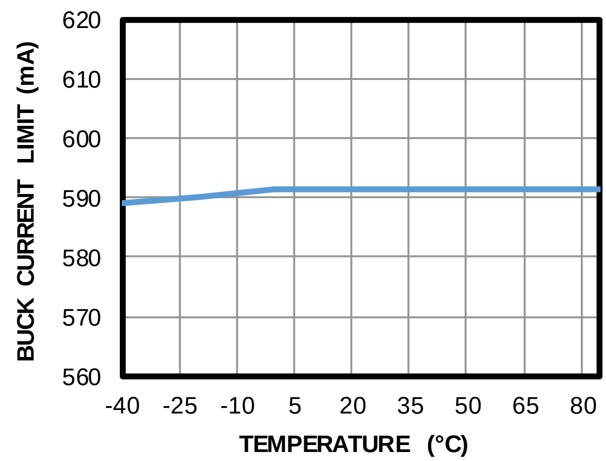
CTRL Rising and Falling Threshold vs. Temp



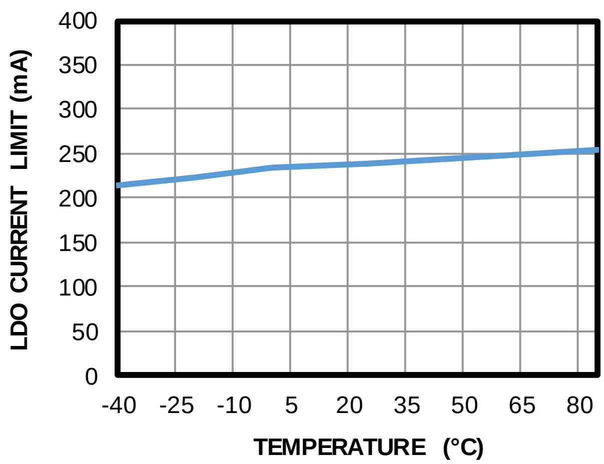
Reference Voltage vs. Temp



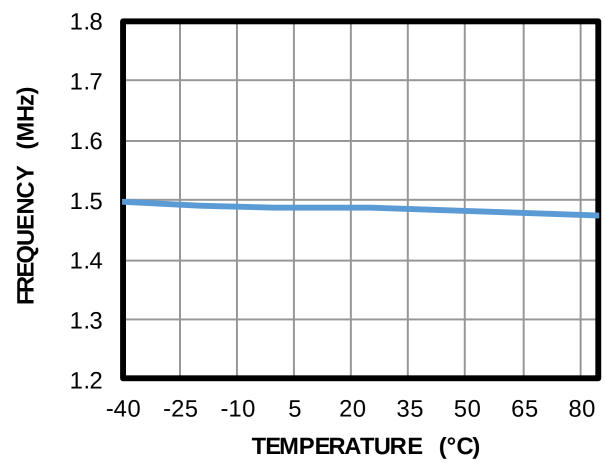
Buck Current Limit vs. Temp



LDO Current Limit vs. Temp



Frequency vs. Temp

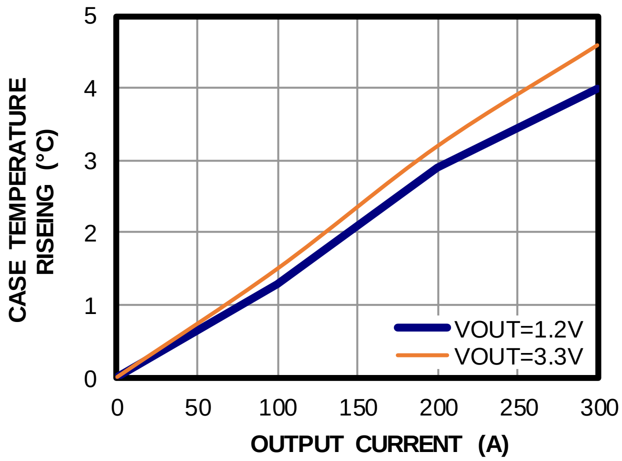


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 3.6V, V_{OUT1} = 1.8V, L_1 = 2.2μH, C_{IN1} = 10μF, C_{OUT1} = 10μF, V_{IN2} = 3.6V, V_{OUT2} = 1.8V, C_{IN2} = 1μF, C_{OUT2} = 1μF, T_A = 25°C, unless otherwise noted.

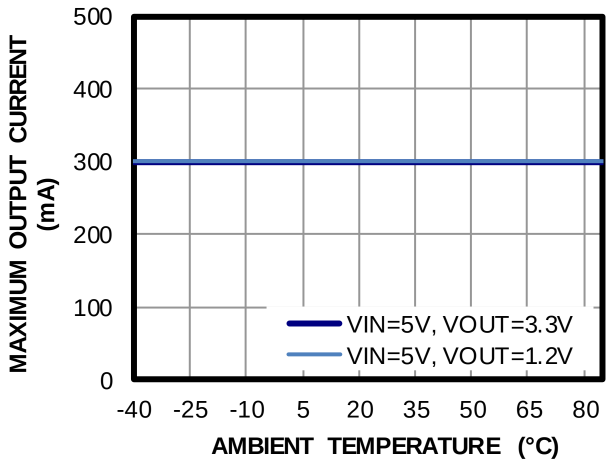
Case Temp Rising vs. Output Current

V_{IN} = 5V



Maximum Output Current vs. Ambient Temp

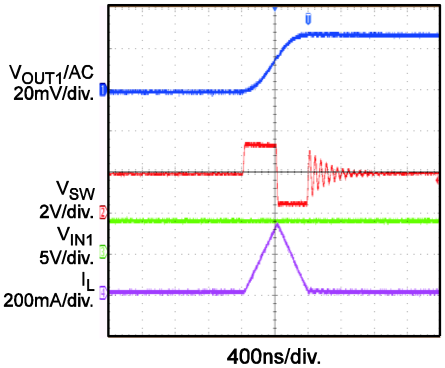
T_J ≤ 125°C



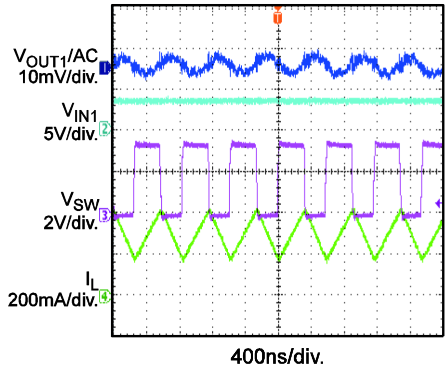
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 3.6V, V_{OUT1} = 1.8V, L_1 = 2.2µH, C_{IN1} = 10µF, C_{OUT1} = 10µF, V_{IN2} = 3.6V, V_{OUT2} = 1.8V, C_{IN2} = 1µF, C_{OUT2} = 1µF, T_A = 25°C, unless otherwise noted.

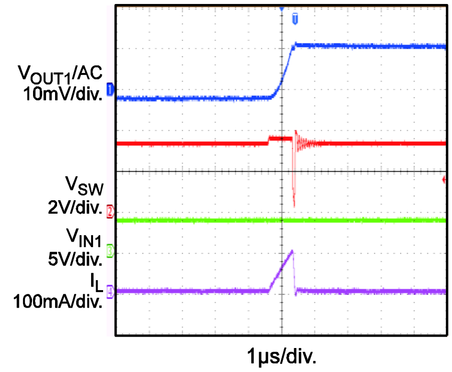
Steady State
I_{OUT1} = 0A



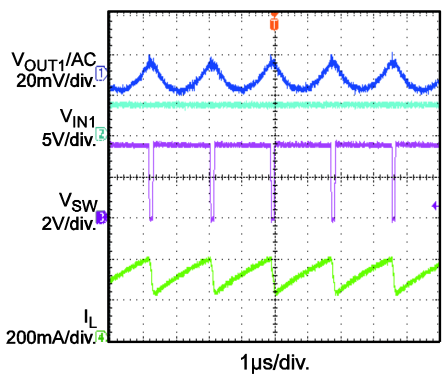
Steady State
I_{OUT1} = 0.3A



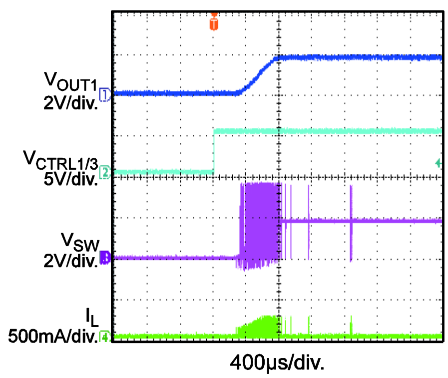
Steady State
V_{OUT1} = 3.3V, I_{OUT1} = 0A



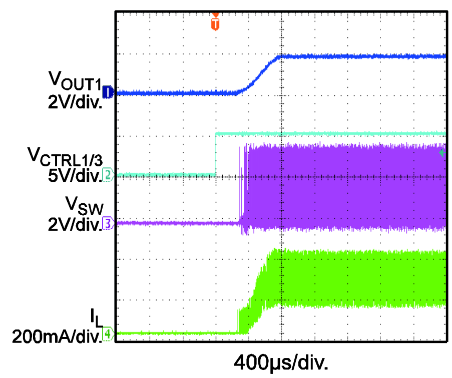
Steady State
V_{OUT1} = 3.3V, I_{OUT1} = 0.3A



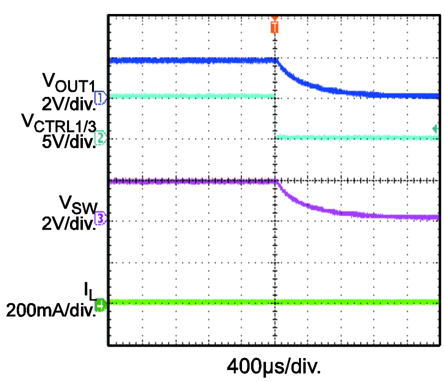
CTRL On
I_{OUT1} = 0A



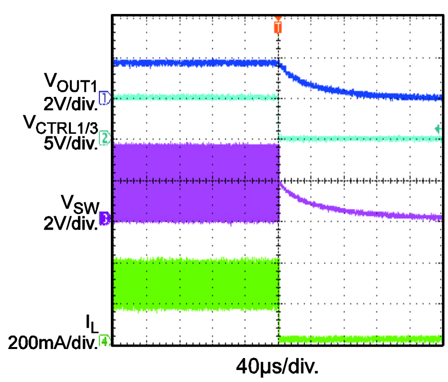
CTRL On
I_{OUT1} = 0.3A



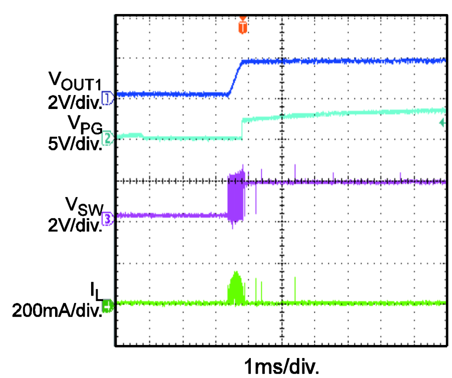
CTRL Off
I_{OUT1} = 0A



CTRL Off
I_{OUT1} = 0.3A



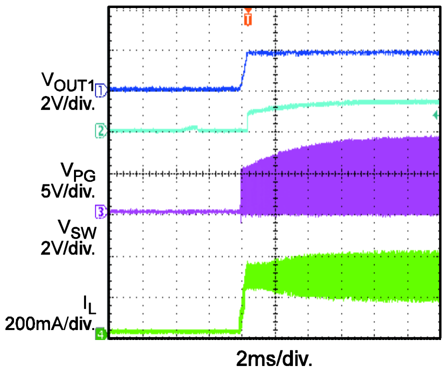
PG On
I_{OUT1} = 0A



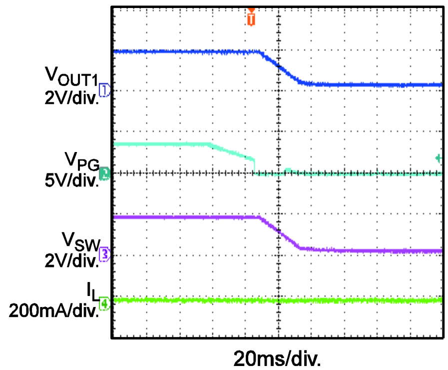
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 3.6V, V_{OUT1} = 1.8V, L_1 = 2.2µH, C_{IN1} = 10µF, C_{OUT1} = 10µF, V_{IN2} = 3.6V, V_{OUT2} = 1.8V, C_{IN2} = 1µF, C_{OUT2} = 1µF, T_A = 25°C, unless otherwise noted.

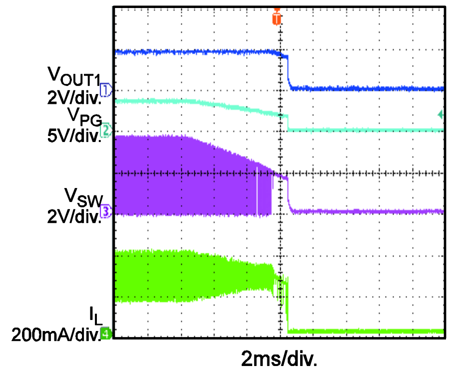
PG On
I_{OUT1} = 0.3A



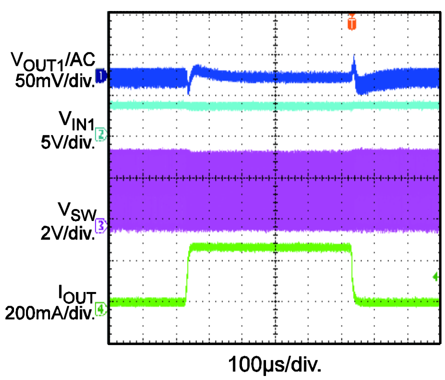
PG Off
I_{OUT1} = 0A



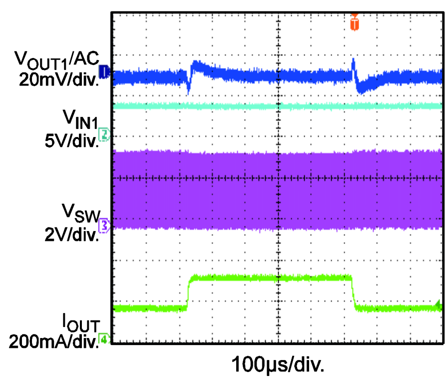
PG Off
I_{OUT1} = 0.3A



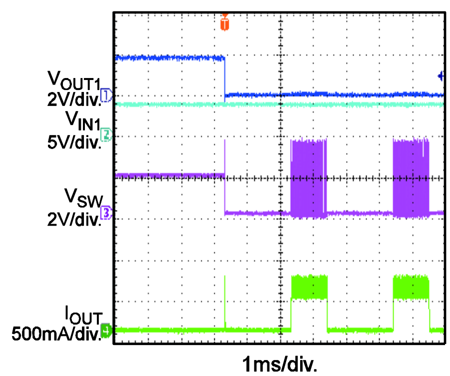
Load Transient
I_{OUT1} = 30mA-300mA, 0.25A/µs



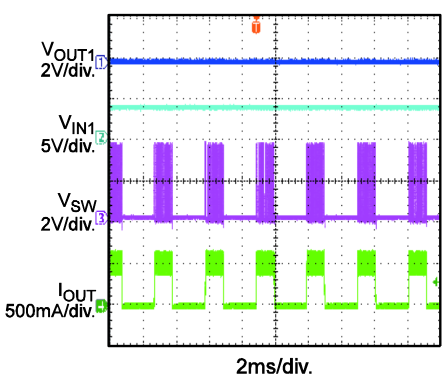
Load Transient
I_{OUT1} = 150mA-300mA, 0.25A/µs



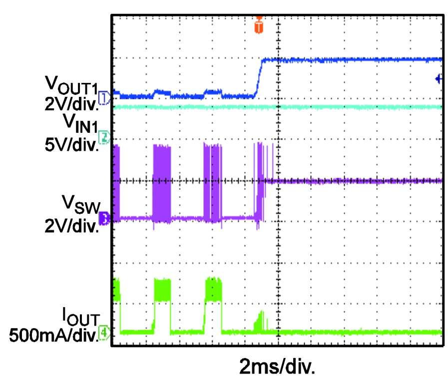
Short-Circuit Entry



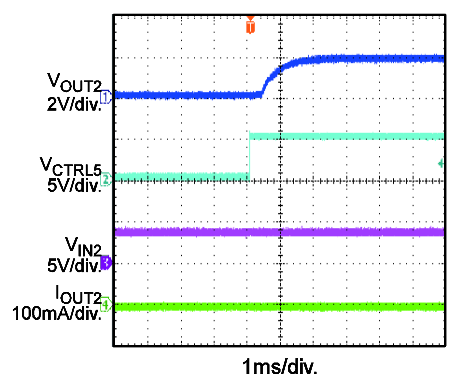
Short-Circuit Steady State



Short-Circuit Recovery



CTRL On
I_{OUT2} = 0A

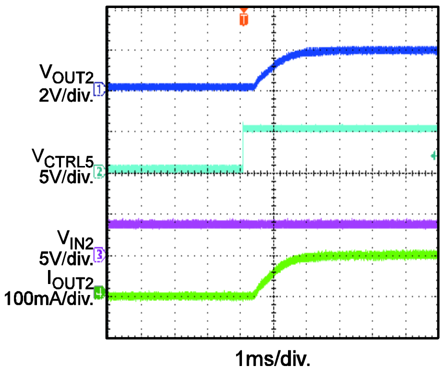


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 3.6V, V_{OUT1} = 1.8V, L_1 = 2.2µH, C_{IN1} = 10µF, C_{OUT1} = 10µF, V_{IN2} = 3.6V, V_{OUT2} = 1.8V, C_{IN2} = 1µF, C_{OUT2} = 1µF, T_A = 25°C, unless otherwise noted.

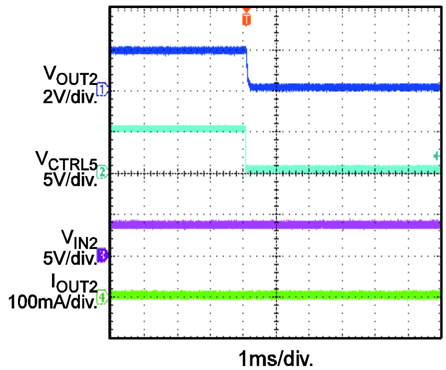
CTRL On

I_{OUT2} = 0.1A



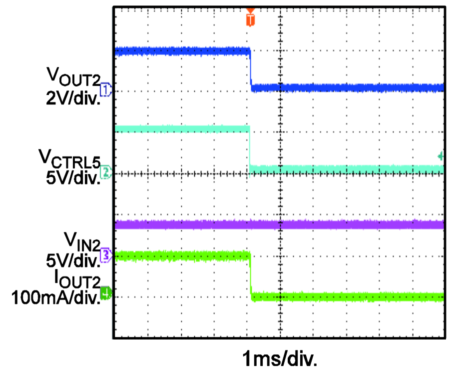
CTRL Off

I_{OUT2} = 0A



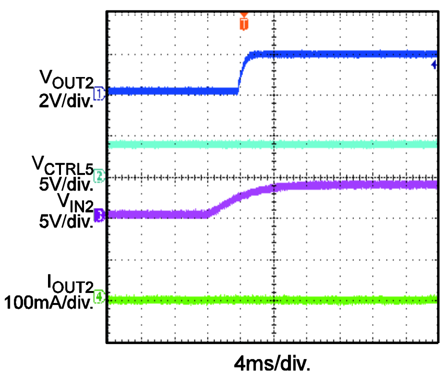
CTRL Off

I_{OUT2} = 0.1A



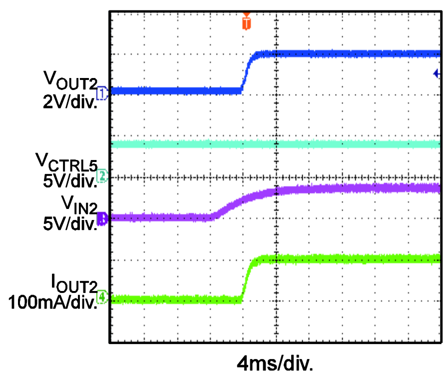
VIN On

I_{OUT2} = 0A



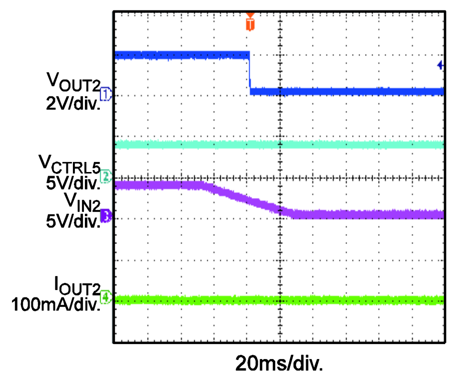
VIN On

I_{OUT2} = 0.1A



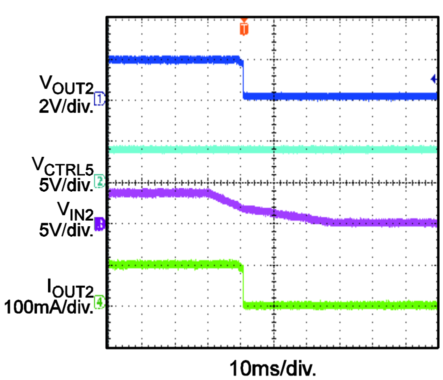
VIN Off

I_{OUT2} = 0A



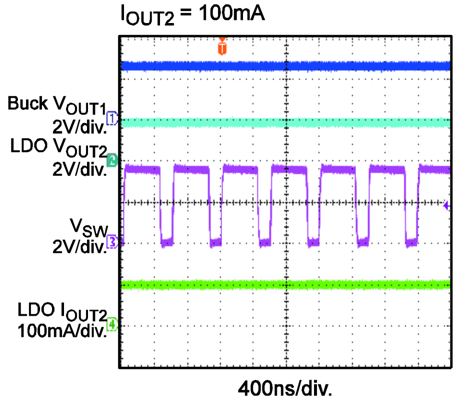
VIN Off

I_{OUT2} = 0.1A



Buck + LDO

V_{IN1} = 3.6, V_{OUT1} = 2.5V, V_{IN2} = V_{OUT1},
V_{OUT2} = 1.8V, I_{OUT1} = 200mA,
I_{OUT2} = 100mA



FUNCTIONAL BLOCK DIAGRAM

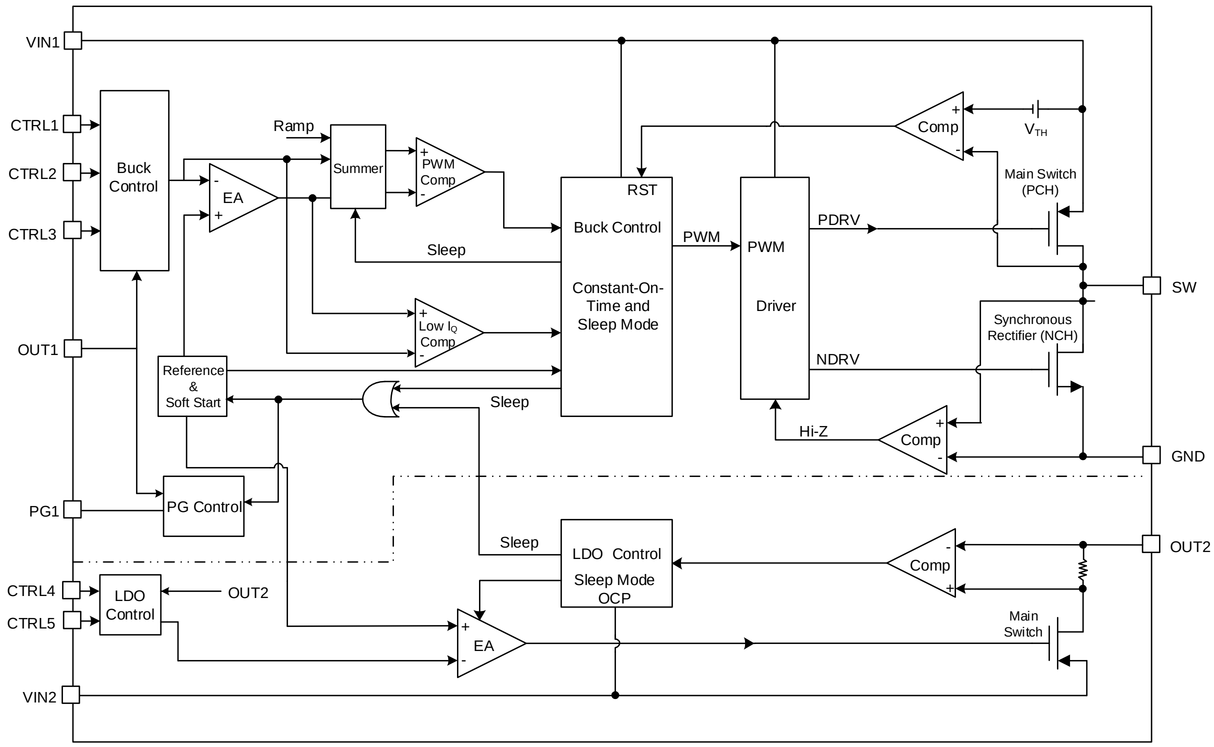


Figure 1: Functional Block Diagram

OPERATION

The MP28310 is a monolithic power management unit containing a step-down converter with an ultra-low quiescent current (I_Q) and a low-dropout (LDO) regulator. The step-down converter has 500nA of I_Q, allowing the MP28310 to achieve extremely high efficiency under ultra-light load conditions. The 300nA low-I_Q LDO provides easy system configuration.

Buck Constant-On-Time (COT) Control

The MP28310 uses constant-on-time (COT) control to regulate the output voltage (V_{OUT}) and stabilize the switching frequency (typically 1.5MHz) across the full input voltage (V_{IN}) range. The one-shot on-timer is controlled by V_{IN} and V_{OUT}. COT control allows the device to achieve a low output ripple and fast load transient response. COT control enables the use of output and input capacitors with lower capacitance. The MP28310 automatically enters pulse-skip mode (PSM) when the low-side MOSFET (LS-FET) current reaches 0A. PSM improves light-load efficiency. COT control provides a seamless transition between pulse-width modulation (PWM) mode and pulse-frequency modulation (PFM) mode.

Light-Load Operation

If the load current decreases and the LS-FET current reaches 0A, both the high-side MOSFET (HS-FET) and LS-FET turn off. The output capacitors provide output energy during this period until V_{OUT} drops to the regulation voltage and triggers another on pulse.

Typically, the switching frequency during PFM mode depends on the load current. The switching frequency is lower when the load current is lighter. With PFM mode under light load, plus the ultra-low I_Q operation current, the MP28310 can achieve the highest efficiency during extremely light-load operation. This extends the charge cycle of any battery-powered system.

The buck needs a minimum of 5µs to exit light-load operation. When a large, sharp load increase occurs during light-load operation, V_{OUT} decreases as the buck exits light-load operation. The LDO exits light-load operation after a load exceeds 20mA.

Control (CTRL)

The Control 1, Control 2, and Control 3 pins (CTRL1/2/3) control the start-up parameters and set V_{OUT} of the step-down converter. When CTRL1/2/3 are low, the MP28310's step-down converter turns off. If one of the CTRL1/2/3 pins is pulled high, the converter turns on. The step-down converter's set V_{OUT} is configurable, and is based on which CTRL1/2/3 pin is pulled high.

When the Control 4 and Control 5 pins (CTRL4/5) are low, the LDO turns off. If one of the CTRL4/5 pins is pulled high, the regulator turns on. The LDO's set V_{OUT} is configurable, and is based on which CTRL4/5 pin is pulled high.

Table 1 shows the programmable output voltages for all CTRL pins.

Table 1: CTRL Pins vs. Output Voltages

Step-Down Converter			
CTRL3	**CTRL2**	**CTRL1**	**OUT1**
0	0	0	Disabled
0	0	1	1.2V
0	1	0	1.5V
0	1	1	1.8V
1	0	0	2.5V
1	0	1	2.8V
1	1	0	3.0V
1	1	1	3.3V

LDO		
CTRL5	**CTRL4**	**OUT2**
0	0	Disabled
0	1	1.8V
1	0	2.8V
1	1	3.0V

V_{OUT} can be configured during normal operation, and supports dynamic V_{OUT} scaling. Do not float the CTRL pins. Any used CTRL voltage must not be below V_{IN}, and any unused CTRL pin must be tied to GND.

Soft Start (SS)

When the converter turns on, the internal reference starts up. After a set delay time, the device enters soft start (SS). The step-down converter V_{OUT} reaches the regulation voltage in about 0.5ms. The LDO's SS time is about 2ms when V_{OUT2} is 3.3V and C_{OUT2} is 1µF.

Power Good (PG) Indicators for the Buck Converter

The MP28310 has an open-drain output power good (PG) indicator with a maximum $R_{DS(ON)}$ of 400Ω. The PG pin requires a 100kΩ to 500kΩ external pull-up resistor for PG indication. This resistor can be pulled up to VIN or tied to CTRL if the CTRL voltages do not need to be adjusted dynamically.

The PG comparator is active when the device is on. The comparator is driven to a high impedance if V_{OUT} reaches the PG threshold (typically 90% of the regulation voltage). It is pulled low if V_{OUT} drops below the PG hysteresis threshold (typically 80% of the regulation voltage). V_{OUT} is also pulled low if V_{IN} is lost or the part turns off.

Output Discharge Function

The step-down converter and LDO feature an output discharge function. Once the step-down converter is off, it utilizes the output discharge function. This function prevents residual charge voltages on the capacitors, which may impact a proper system start-up. Output discharge is active when V_{IN} is high and the related converters are off.

100% Duty Cycle Mode

When V_{IN} drops below the regulation output voltage, V_{OUT} drops and the on time increases. Reducing V_{IN} further drives the MP28310 into 100% duty cycle mode. The HS-FET is always on, and V_{OUT} is determined by the load current multiplied by $R_{DS(ON)}$, which is determined by the HS-FET and inductor.

Low-Dropout (LDO) Mode

The low-dropout (LDO) regulator turns on once CTRL4 or CTRL5 pulls high and VIN1's input voltage (V_{IN1}) reaches the UVLO threshold. CTRL4/5 can be programmed to select one of three preset output voltages.

Current Limit

The MP28310's step-down converter and LDO each have an internal current limit.

The HS-FET current is monitored cycle by cycle and compared to the current-limit threshold. Once the current-limit comparator is triggered, the HS-FET turns off and the LS-FET turns on, reducing the inductor current. The HS-FET cannot turn on again until the LS-FET current drops below the low-side current limit.

If the LDO current reaches its current limit, the LDO current clamps at the current limit and output regulation stops.

Short Circuit and Recovery

If the buck converter's V_{OUT} is shorted to GND, the current limit is triggered. If the current limit is triggered every cycle for 200µs, the MP28310's buck converter enters hiccup mode.

The short-circuit condition is also triggered if V_{OUT} drops below 50% of the regulation V_{OUT} as the device reaches the current limit. The buck converter disables the output power stage, discharges V_{OUT}, and then attempts to recover after hiccup mode. If the short-circuit condition remains, the MP28310 repeats this operation until the short circuit is removed and V_{OUT} returns to its regulation level.

When a short circuit occurs in the LDO, the short-circuit protection (SCP) mechanism is similar to the over-current protection (OCP) mechanism. The current is clamped at the LDO current limit level.

Thermal Shutdown Circuit and Recovery

If the thermal shutdown signal is triggered, the MP28310 turns off immediately. Once the temperature returns to below the thermal hysteresis threshold, the device restarts and resumes normal operation.

APPLICATION INFORMATION

Selecting the Inductor

Most applications work best with a 1µH to 2.2µH inductor. Select an inductor with a DC resistance below 200mΩ to optimize efficiency.

High-frequency, switch-mode power supplies with magnetic devices create strong electromagnetic inference (EMI) in the system. Unshielded power inductors should be avoided since they have poor magnetic shielding. Metal alloy or multiplayer chip power shield inductors are recommended in application, as they effectively decrease EMI influence. Table 2 lists our inductor recommendations. Select a part number based on your design requirements.

Table 2: Recommended Inductors

Inductance	Manufacturer P/N	Package	Manufacturer
2.2µH	DFE201612P-2R2M	2016	Tokyo
2.2µH	74479775222A	2012	Wurth

For most designs, the inductance value can be calculated with Equation (1):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (1)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (2):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (2)$$

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input, as well as the switching noise from the device. Select an input capacitor with a switching frequency impedance below the input source impedance to prevent high-frequency switching current from passing through the input source. It is recommended to use low-ESR ceramic capacitors with X5R or X7R dielectrics due to their small temperature coefficients. For most applications, a 10µF capacitor is sufficient.

The input capacitor requires an adequate ripple current rating to absorb the input switching current.

The RMS current in the input capacitor can be estimated with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst-case scenario occurs when $V_{IN} = 2V_{OUT}$, and can be calculated with Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, 0.1µF, ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Output Capacitor Selection

The output capacitor limits the output voltage ripple and ensures a stable regulation loop. Select an output capacitor with low impedance at the switching frequency. For most applications, a 10µF capacitor is sufficient. The output voltage ripple can be calculated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (6)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple.

For simplification, the output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

PCB Layout Guidelines

Designing an efficient PCB layout for the switching power supply, especially the high switching frequency converter, is critical for stable operation. Without careful placement, the regulator could exhibit poor line or load regulation and stability issues.

For the best results, refer to Figure 2 and follow the guidelines below:

1. Place the input capacitor as close to the IC pins as possible. This helps the high-speed step-down regulator provide clean control voltage for the chip.
2. Place C_{IN1} close to VIN1 and GND to absorb noise.

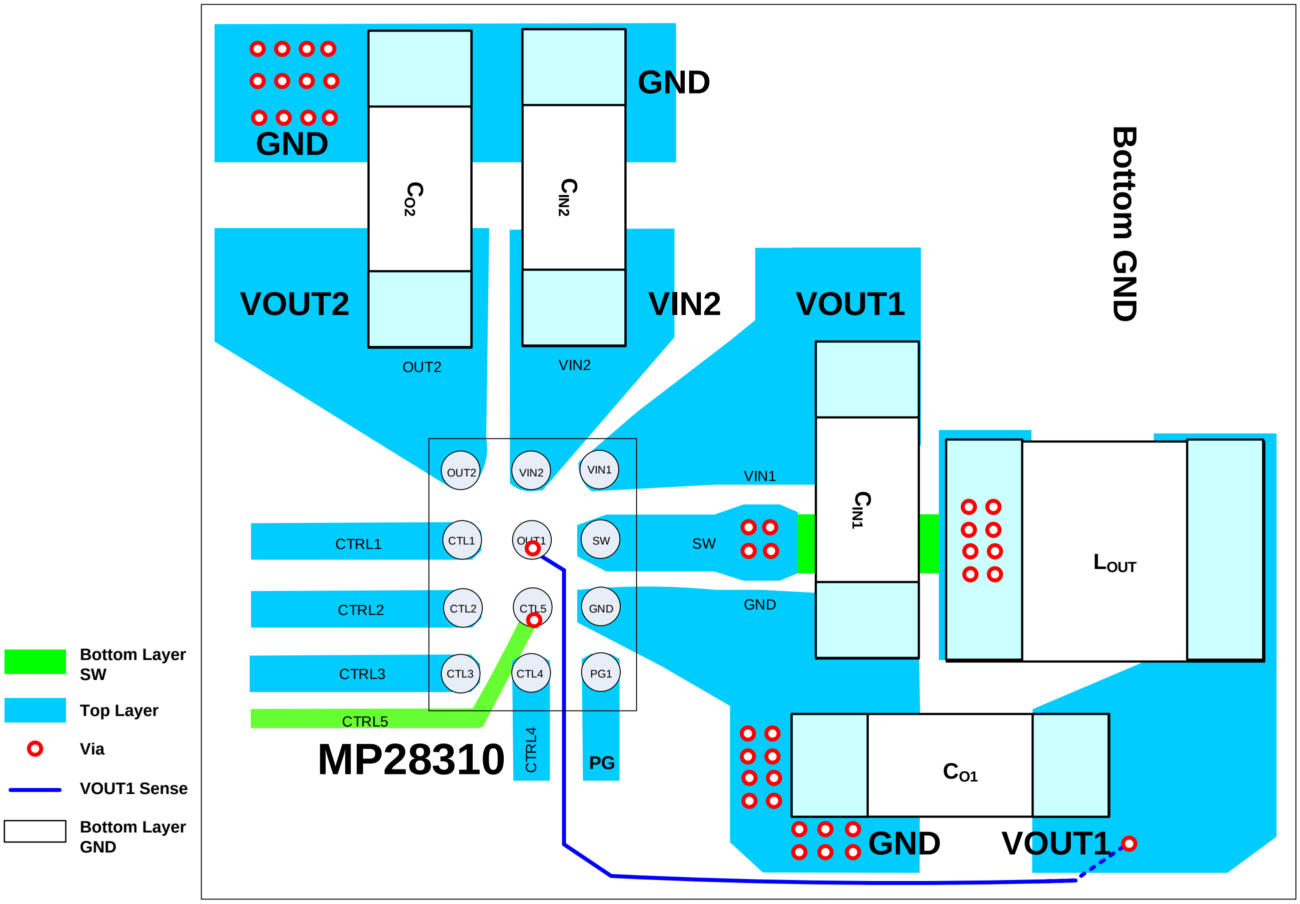


Figure 2: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

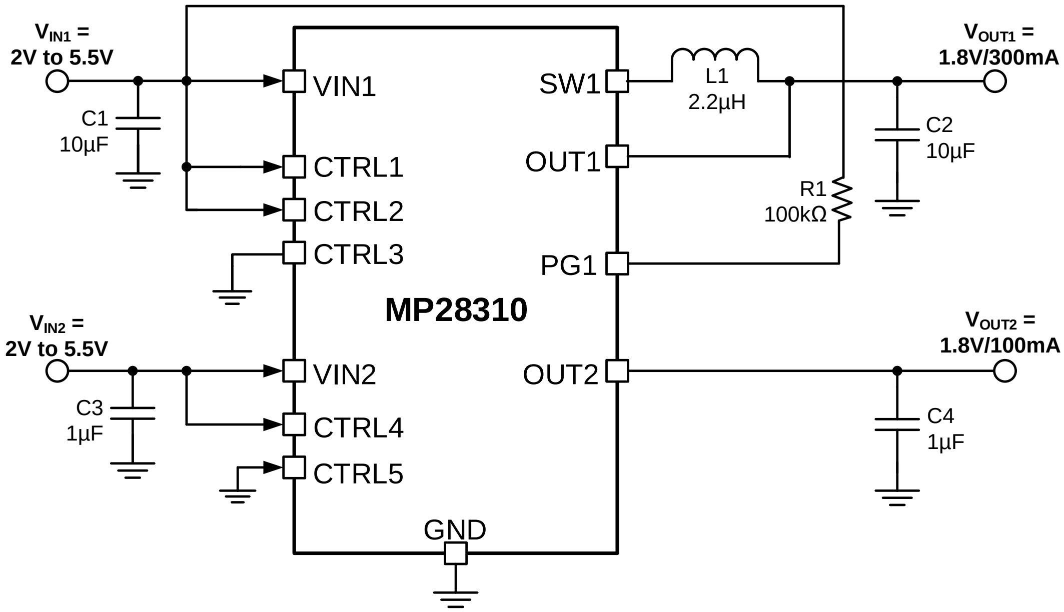


Figure 3: Typical Application Circuit for MP28310GC (8)

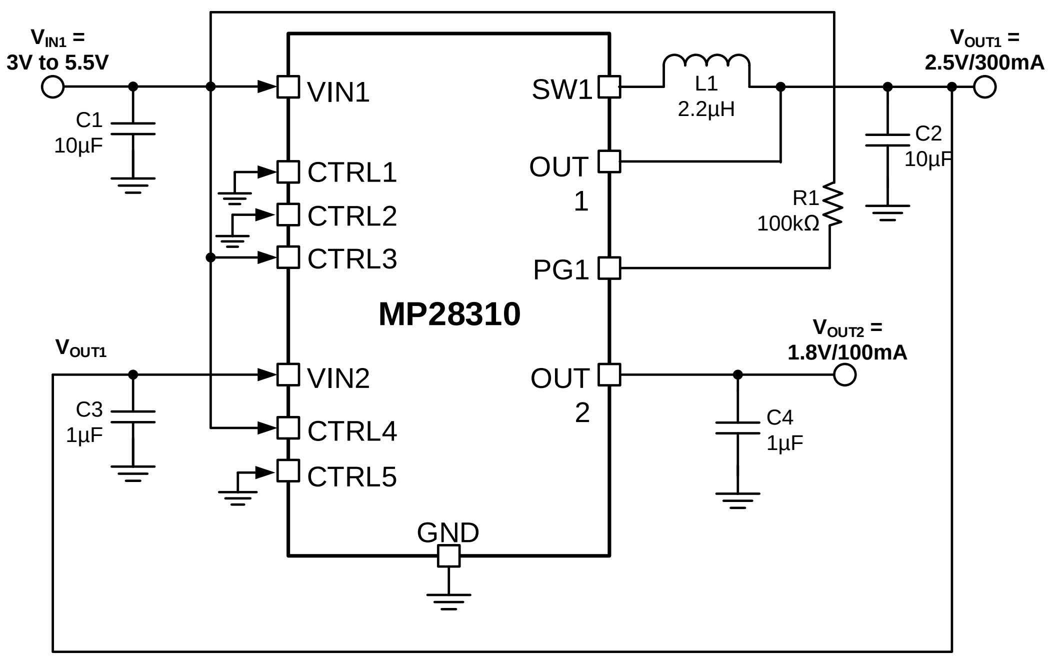


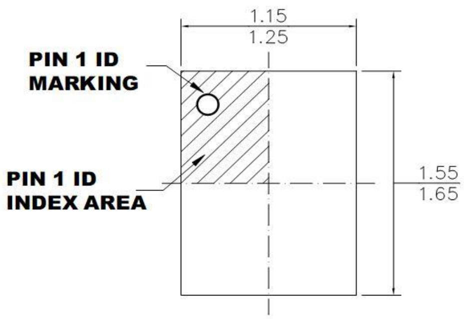
Figure 4: Buck and LDO in Sequence (9)

Notes:

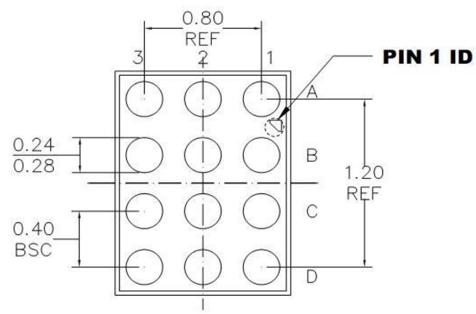
8) VIN1 and VIN2 have dependent power supplies. VIN1 must exceed the VIN under-voltage lockout (UVLO) threshold.
9) CTRL4/5 must be connected to VIN1 in sequence.

PACKAGE INFORMATION

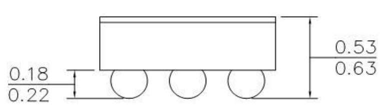
CSP-12 (1.2mmx1.6mm)



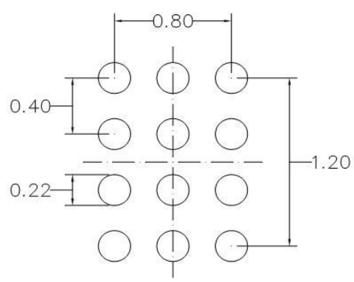
TOP VIEW



BOTTOM VIEW



SIDE VIEW

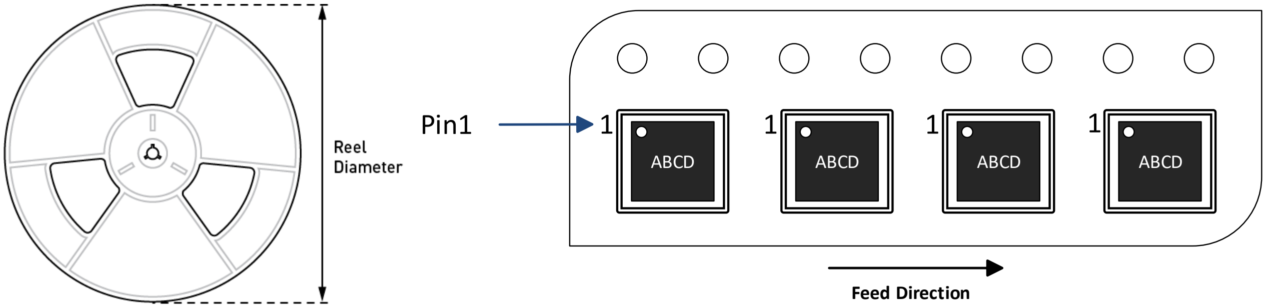


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP28310GC–Z	CSP-12 (1.2mmx1.6mm)	3000	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/23/2020	Initial Release	-