

DESCRIPTION

The MP3416 is a low quiescent current, step-up converter that uses peak-current control and variable frequency architecture to regulate the output voltage. The MP3416 can work with an input voltage as low as 0.86V to provide an output voltage from 1.8V to 5.5V.

The MP3416 works in peak-current-control mode and provides good transient response. The integrated P-channel synchronous rectifier improves efficiency and eliminates the need for an external Schottky diode.

In light-load condition, the peak current declines to about 350mA, and the device enters pulse-skip mode to save power loss. When the MP3416 shuts down, the output is disconnected from the input, allowing the output to draw less than 0.65µA in shutdown mode.

The MP3416 is available in 8-pin TSOT23 and 8-pin QFN (1.5mmx2.0mm) packages.

FEATURES

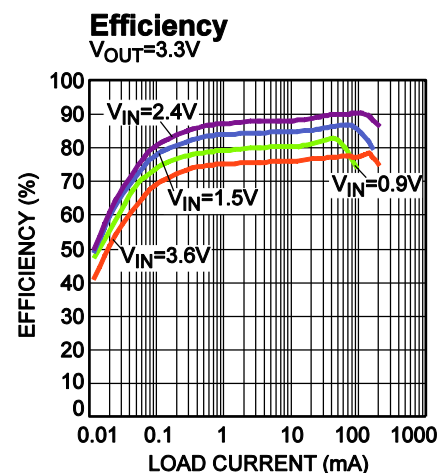
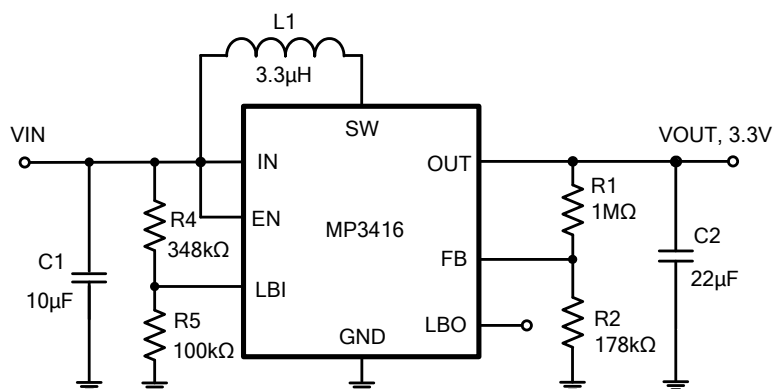
- Input Voltage Range: 0.86V to 5.5V
- Start-Up Voltage Range: 1.25V to 5.5V
- Output Voltage Range: 1.8V to 5.5V
- 9.5µA Quiescent Current
- <650nA Shutdown Current
- Up to 80% Efficiency at 100µA-200µA Light-Load Condition
- Output Disconnect in Shutdown
- Down Mode When $V_{IN} > V_{OUT}$
- Adjustable Low Battery Detection
- Internal Synchronous Rectifier
- Over-Temperature Protection (OTP) with Thermal Shutdown at 155°C
- Available in TSOT23-8 and QFN-8 (1.5mmx2.0mm) Packages

APPLICATIONS

- Medical Devices
- Digital Retail Displays
- Gaming Controllers
- Remote Controllers
- Battery-Powered Products
- Handheld Computers and Smart Phones

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TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking
MP3416GJ*	TSOT23-8	See Below
MP3416GQH**	QFN-8 (1.5mmx2.0mm)	See Below

* For Tape & Reel, add suffix-Z(e.g. MP3416GJ-Z)

** For Tape & Reel, add suffix-Z(e.g. MP3416GQH-Z)

TOP MARKING (MP3416GJ)

| AHTY

AHT: Product code of MP3416GJ

Y: Year code

TOP MARKING (MP3416GQH)

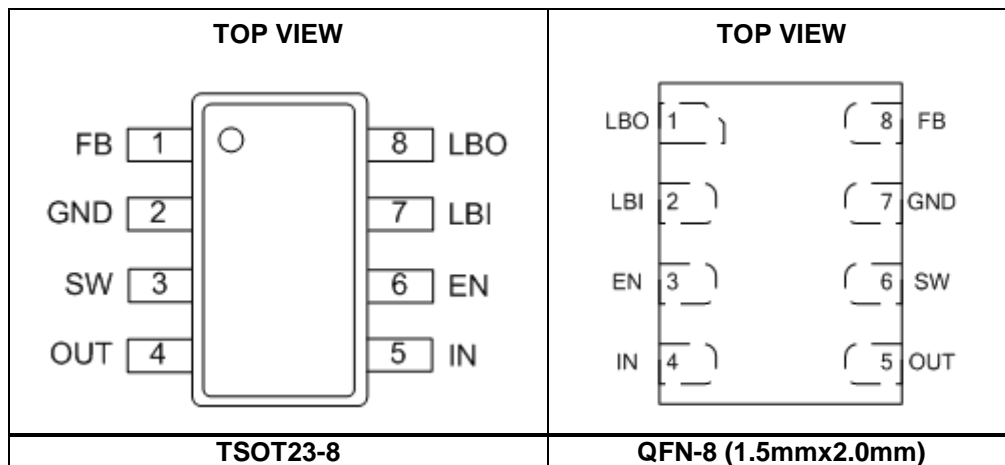
FK

LL

FK: Product code of MP3416GQH

LL: Lot number

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

SW	-0.3V to +6.5V (8.5V for <5ns)
All other pins	-0.3V to +6.5V
Continuous power dissipation (T _A = +25°C) ⁽²⁾	
TSOT23-8	1.25W
QFN-8	1.14W
Junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to +150°C

Recommended Operating Conditions ⁽³⁾

Start-up voltage (V _{ST})	1.25V to 5.5V
Operation voltage (V _{IN})	0.86V to 5.5V
V _{OUT}	1.8V to 5.5V
Operating junction temp. (T _J)	-40°C to +125°C

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}
TSOT23-8	100	55 ... °C/W
QFN-8 (1.5mmx2.0mm)	110	55 ... °C/W

NOTES:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN}= V_{EN}=1.8V, V_{OUT} = 3.3V, T_J= -40°C to +125°C, typical value is tested at T_J= +25°C. The limit over temperature is guaranteed by characterization unless otherwise noted.

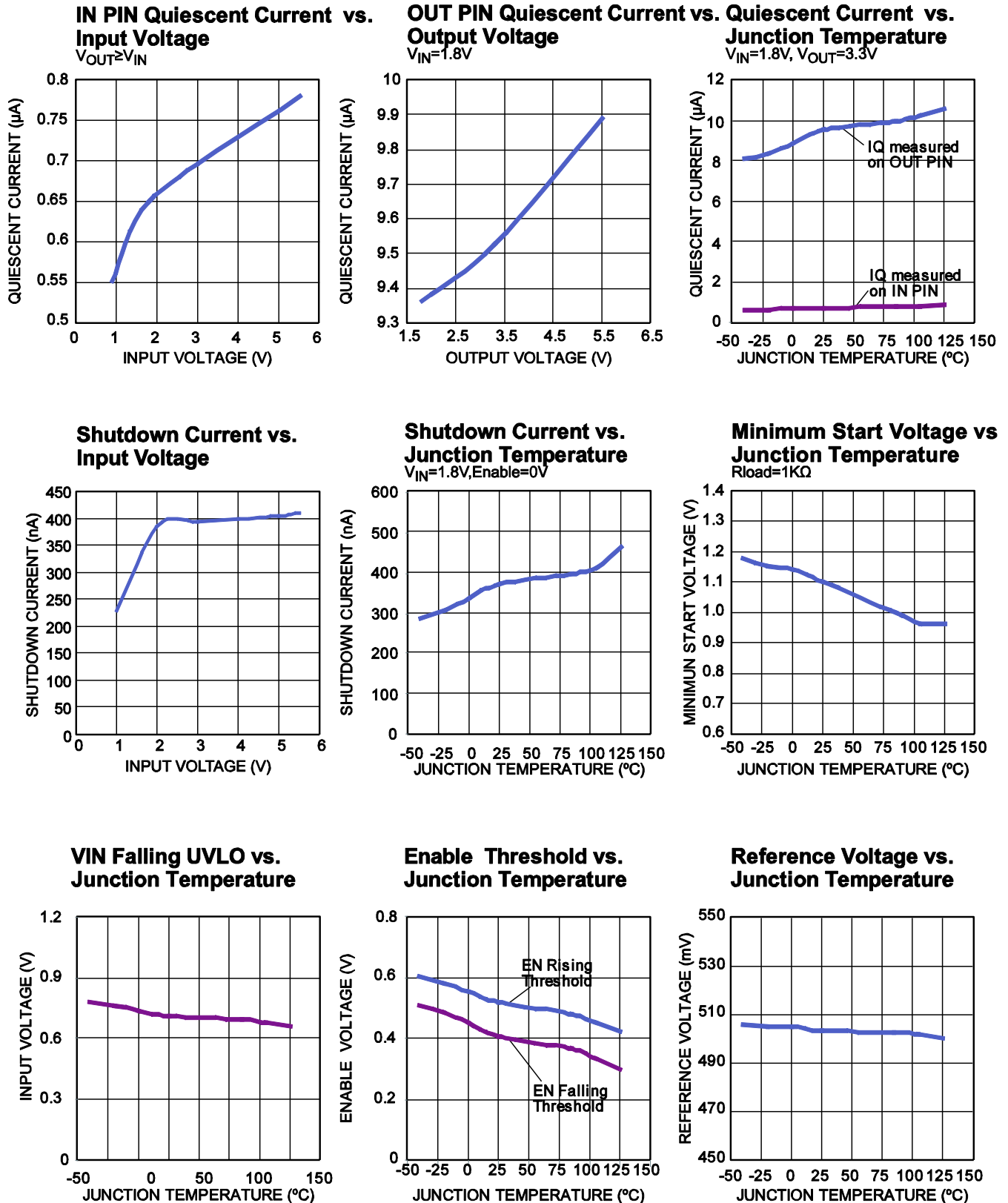
Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Voltage						
Minimum start-up voltage	V _{ST}	R _{LOAD} =1000Ω, T _J =25°C		1.1	1.25	V
Operating input voltage	V _{IN}		0.86		5.5	V
V _{IN} off under-voltage lockout	V _{UVLO}	V _{IN} falling		0.7	0.86	V
Output Voltage						
Feedback voltage	V _{FB}	T _J =25°C	494	504	514	mV
		T _J = -40°C to 125°C	491	504	517	mV
Feedback input current	I _{FB}	V _{FB} =0.55V		10	70	nA
Operation Current						
Quiescent current	I _Q	V _{EN} =V _{IN} =1.8V, V _{OUT} =3.3V, no load, measured on IN		0.65	1.1	μA
		V _{EN} =V _{IN} =1.8V, V _{OUT} =3.3V, no load, measured on OUT		9.5	12	μA
Shutdown current	I _{SD}	V _{EN} =V _{OUT} =0V, measured on IN		360	650	nA
Switch MOSFET						
NMOS on-resistance	R _{N_ON}			100		mΩ
PMOS on-resistance	R _{P_ON}			800		mΩ
NMOS current limit	I _{SW_LIMIT}	T _J =25°C, duty=50%	900	1100	1300	mA
		T _J = -40°C to 125°C, duty=50%	790	1100	1410	mA
NMOS max on period	T _{ON_MAX}			10		μs
EN Control						
EN input high level	V _{EN_H}		0.7			V
EN input low level	V _{EN_L}				0.2	V
EN input current	I _{EN}	Connect to V _{IN}			100	nA
LBI Detection						
Low battery threshold	V _{LBI}	Falling edge		0.4		V
LBI hysteresis	V _{LBI-HYS}			70		mV
LBI input leakage current	I _{LBI}	Connect to V _{IN}			100	nA
LBO low voltage level	V _{LBO}	I _{LBO} =1mA		20	50	mV
LBO input leakage current	I _{LBO}	Connect to V _{OUT} , LBO logic high			100	nA
Thermal Protection						
Thermal shutdown ⁽⁵⁾				155		°C
Thermal shutdown hysteresis ⁽⁵⁾				20		°C

NOTE:

5) Guaranteed by characterization, not production tested.

TYPICAL CHARACTERISTICS

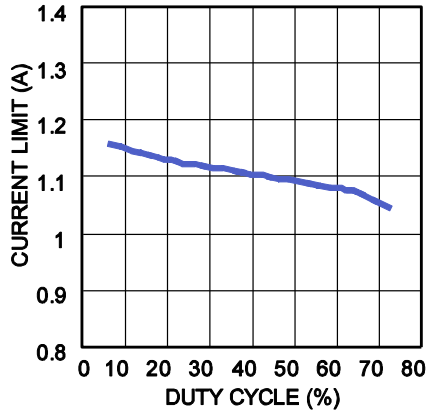
V_{IN} = 1.8V, V_{OUT} = 3.3V, L = 3.3μH, T_A = 25°C, unless otherwise noted.



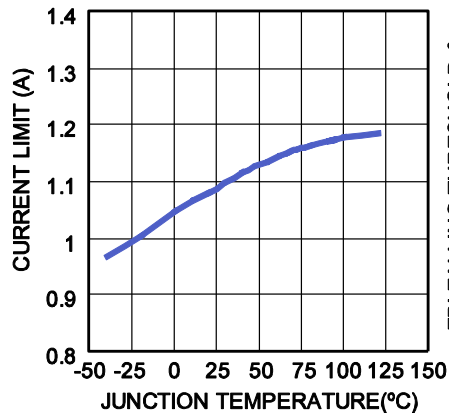
TYPICAL CHARACTERISTICS*(continued)*

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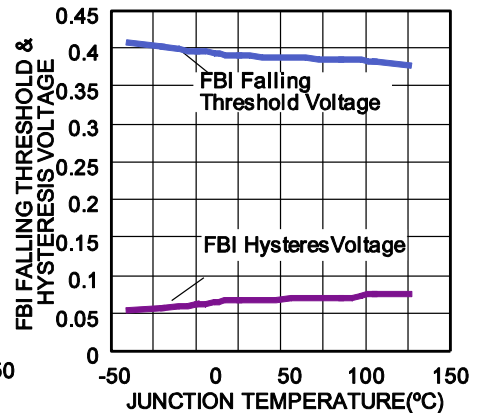
Current Limit vs. Duty Cycle



Current Limit vs. Junction Temperature

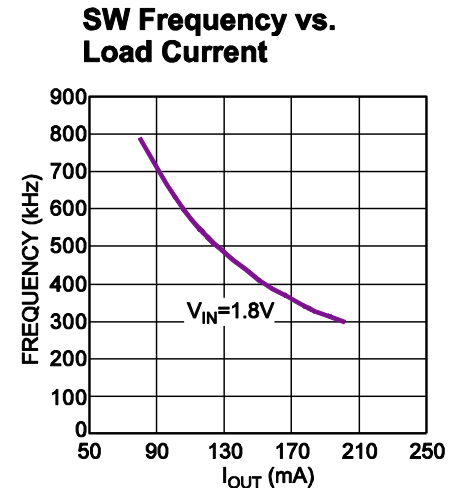
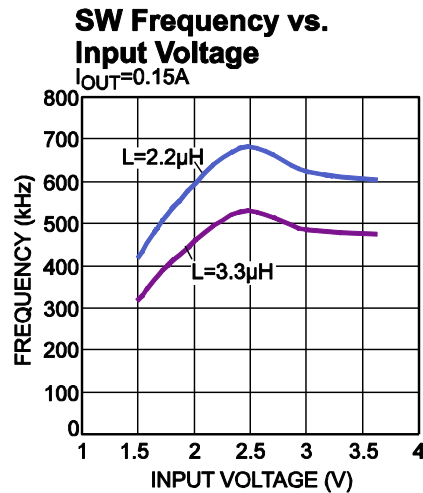
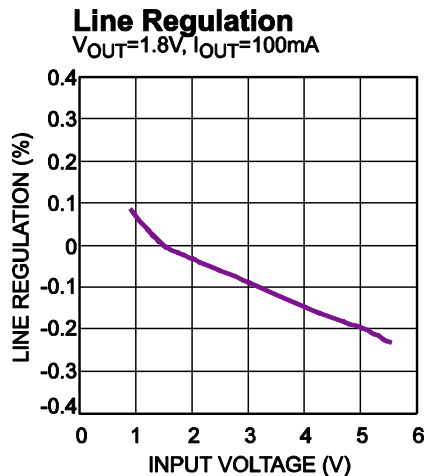
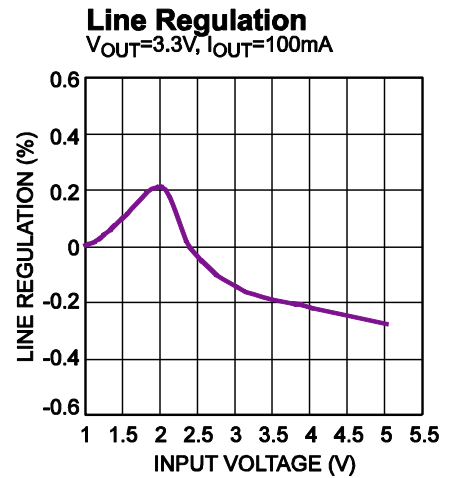
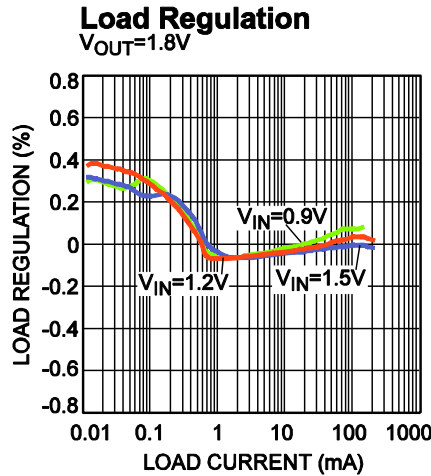
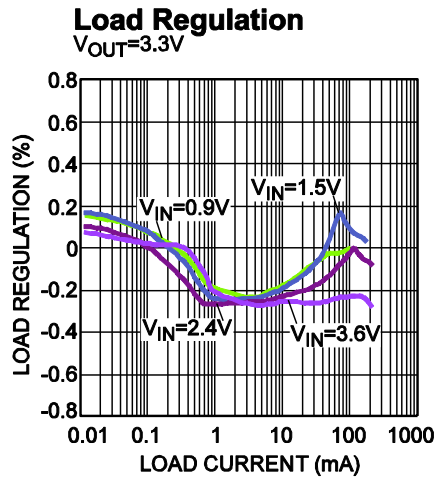
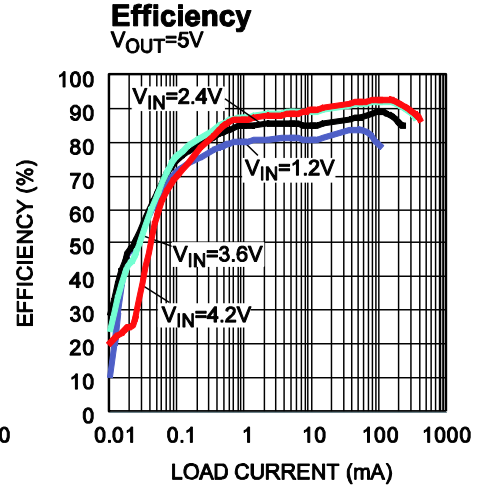
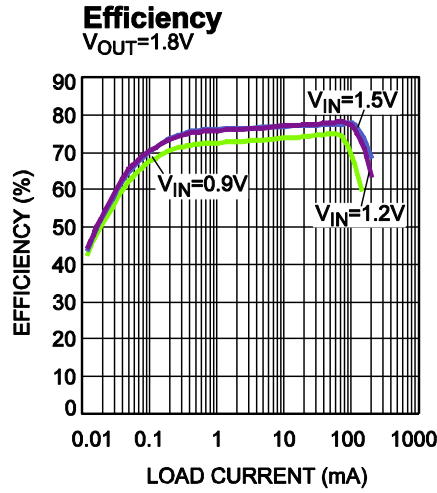
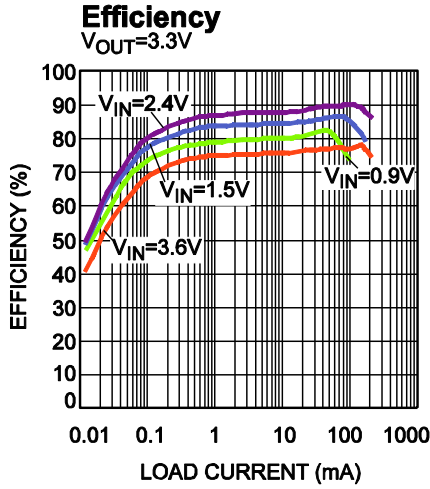


FBI Falling Threshold & Hysteresis Voltage vs. Junction Temperature

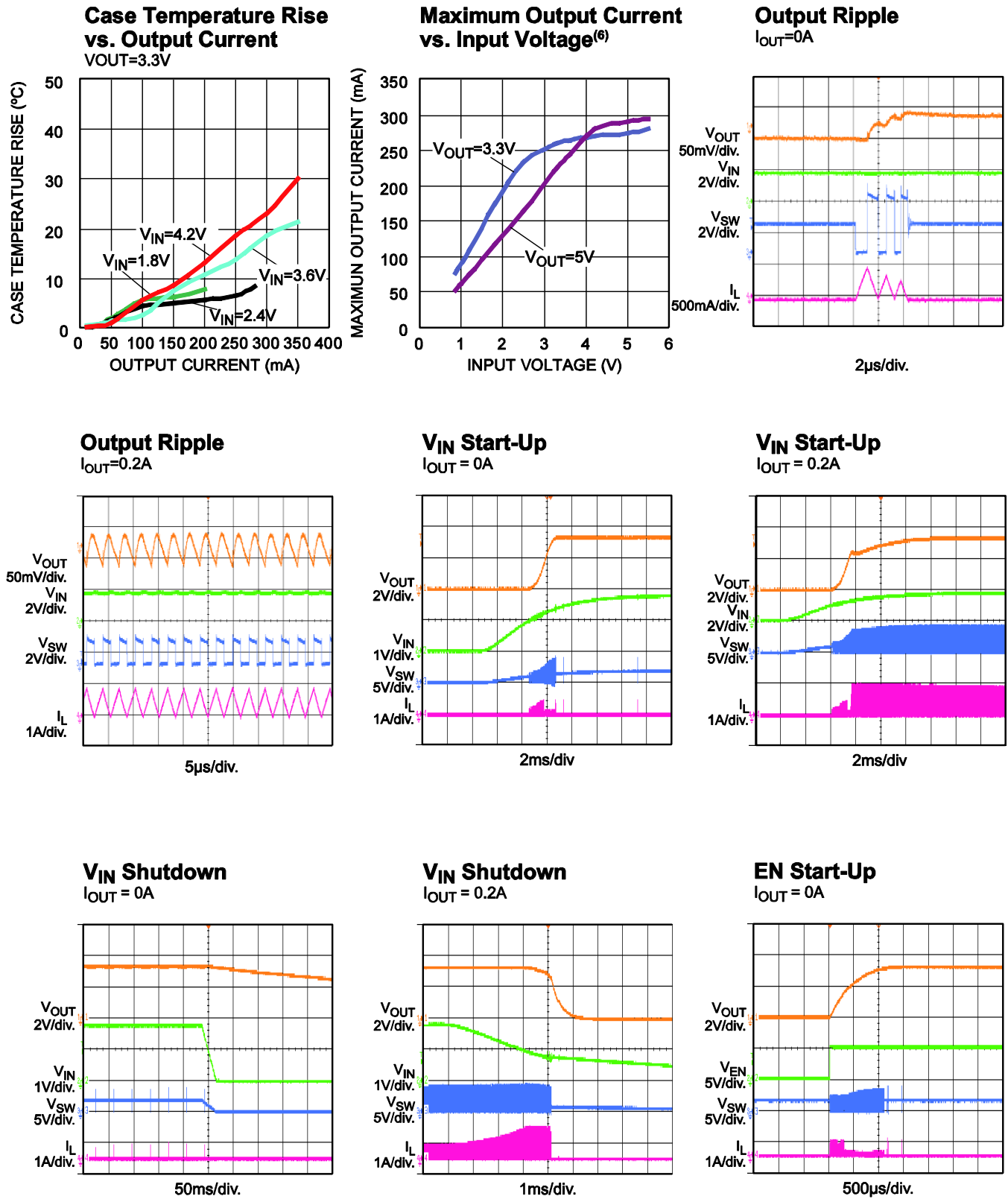


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 1.8V, V_{OUT} = 3.3V, L = 3.3μH, T_A = 25°C, unless otherwise noted.

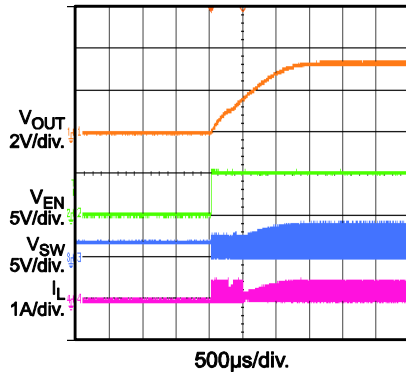
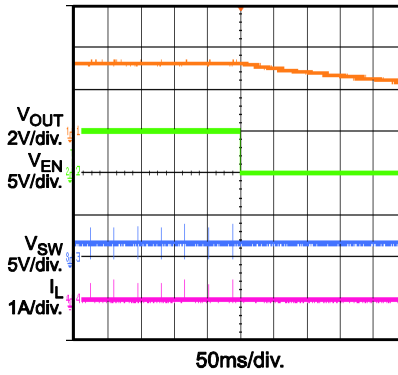
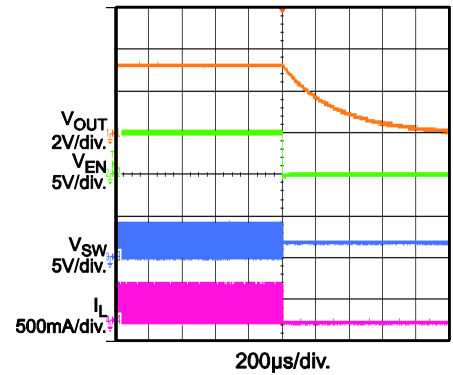
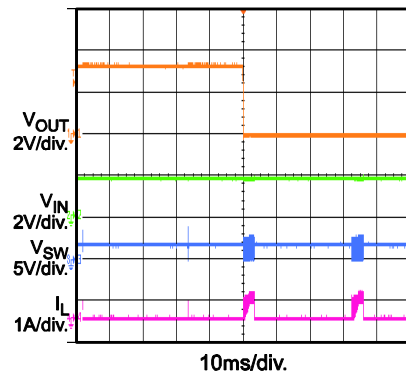
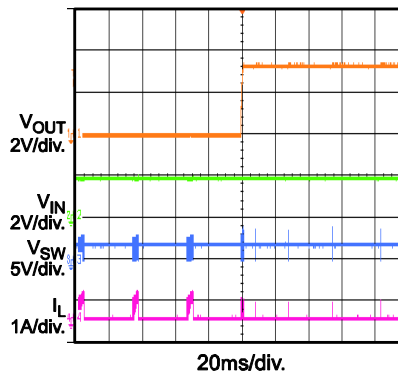
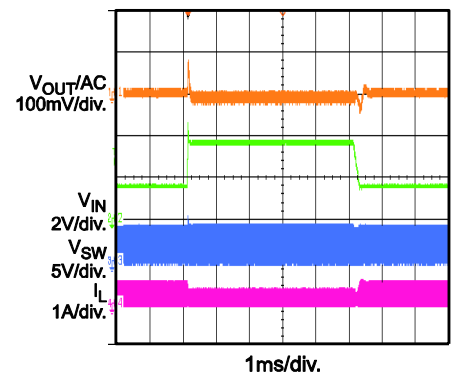
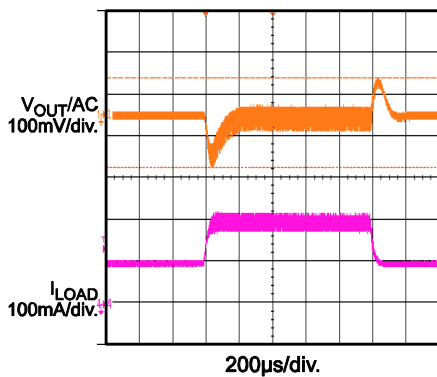


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

 $V_{IN} = 1.8V$, $V_{OUT} = 3.3V$, $L = 3.3\mu H$, $T_A = 25^\circ C$, unless otherwise noted.


TYPICAL PERFORMANCE CHARACTERISTICS(continued)

 $V_{IN} = 1.8V$, $V_{OUT} = 3.3V$, $L = 3.3\mu H$, $T_A = 25^\circ C$, unless otherwise noted.

EN Start-Up
 $I_{OUT} = 0.2A$

EN Shutdown
 $I_{OUT} = 0A$

EN Shutdown
 $I_{OUT} = 0.2A$

SCP Enter

SCP Recover

Line Transient
 $V_{IN} = 1.8V$ to $3.6V$, $I_{OUT} = 0.1A$

Load Transient
 $I_{OUT} = 0.1A$ to $0.2A$

NOTE:

 6) Tested under a 0.79A switching current limit. The test schematic is the same as Figure 5 when V_{OUT} is 3.3V and the same as Figure 6 when V_{OUT} is 5V.

PIN FUNCTIONS

Pin # TSOT23-8	Pin # QFN-8	Name	Description
1	8	FB	Feedback input for the error amplifier. Connect the resistor divider tap to FB.
2	7	GND	Ground. GND is the reference ground of the regulated output voltage.
3	6	SW	Output switch node. Connect the inductor to SW to complete the step-up converter.
4	5	OUT	Output node. OUT is the source of the internal synchronous rectifier. Place the output capacitor between OUT and GND.
5	4	IN	Input supply. IN requires a bypass capacitor.
6	3	EN	Enable input. EN turns the regulator on or off. Logic high (>0.7V) turns on the regulator; logic low (<0.2V) turns off the regulator. It is not recommended to leave EN floating.
7	2	LBI	Low battery detection input. Do not leave LBI floating. Connect LBI to VIN through a resistor divider to detect a low battery condition. The divided LBI voltage should be higher than 0.2V during application. Pull LBI up to V _{IN} if the LBI function is not used.
8	1	LBO	Low battery detection output. The output of LBO is an open-drain signal. LBO requires a pull-up resistor to a DC voltage to indicate high if the input voltage is higher than the threshold of the low battery detection voltage. LBO maintains a high impedance when the IC is off.

BLOCKDIAGRAM

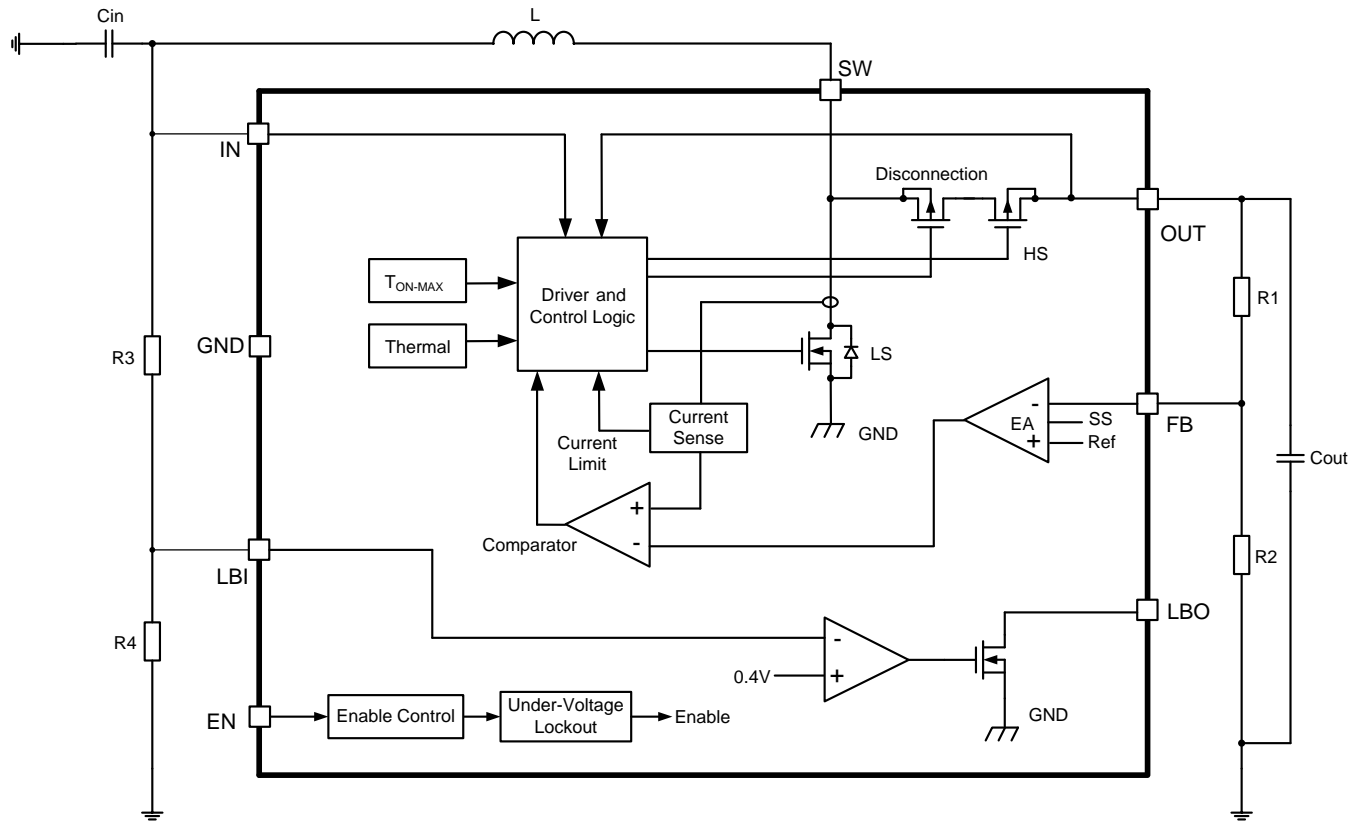


Figure 1: Functional Block Diagram

OPERATION

The MP3416 is a peak-current mode, step-up converter in a compact TSOT23-8 or QFN-8 package with true output disconnect. The MP3416 can operate at input voltages as low as 0.86V and features peak current and boundary conduction mode (BCM) control for exceptional line and load regulation. Internal softstart and loop compensation simplify the design process and minimize external components. The internal low R_{DS(ON)} MOSFETs combined with power-save mode (PSM) operation enable the device to maintain high efficiency over a wide current load range.

PWM Operation

The MP3416 utilizes a peak-current control scheme. The output voltage is monitored by FB, which is connected to the internal error amplifier (EA). The error amplifier compares the feedback voltage and reference voltage, and the EA output voltage controls the peak inductor current.

At the beginning of each cycle, the low-side MOSFET (LS-FET) turns on, the inductor current rises up to the peak current which is decided by the EA output, and then the LS-FET turns off, and the high-side MOSFET (HS-FET) turns on. The inductor current charges the output capacitor while the HS-FET is on. After the inductor current reduces to zero, the LS-FET initiates one new cycle to raise the inductor current.

In light load, the EA output drops and limits the peak inductor current at about 350mA. If the EA output voltage continues decreasing due to a high V_{OUT}, the LS-FET locks and does not turn on again until the EA output rises up to a 350mA peak inductor current. This allows the device to work in PSM smoothly to achieve high efficiency in light-load condition. While the load current increases, the peak inductor current increases and transfers more energy to the output.

Down Mode (V_{IN} > V_{OUT})

The MP3416 integrates one disconnection MOSFET (DIS-FET) for down-mode condition. When V_{IN} is lower than V_{OUT}-0.2V, the DIS-FET is on and does not differ from a normal converter's operation. While V_{IN} rises higher, the gate of the DIS-FET is connected to a voltage level of V_{IN}-0.4V. In this condition, the SW voltage is charged high by the inductor current. The DIS-FET no longer acts as a low-impedance path, but only turns on when the SW voltage is charged high by the inductor current. If the inductor current is zero, the SW voltage is equal to V_{IN}, so the DIS-FET does not turn on. In shutdown, the LS-FET never turns on to setup the inductor current, so the DIS-FET can disconnect the output terminal from the input to prevent battery discharge.

Start-Up

There are three steps for start-up. Firstly, after the input voltage rises up to the minimum start-up voltage, the MP3416 enters open-loop work mode. In this mode, the switching on time is constant, and the output voltage is charged high by increasing the switching frequency. When V_{OUT} rises to about 1.7V, the MP3416 switches to close-loop work mode with soft-start control. In this second stage, the inductor peak current is controlled by the internal COMP voltage (V_{COMP}), and the minimum peak current is not limited, so the switching frequency may be high, and the rising output voltage has a very small voltage ripple. Finally, when the output voltage is close to its set value, the MP3416 enters BCM close-loop mode, while the minimum peak inductor current is limited above 350mA. Due to the 350mA minimum peak current, the MP3416 may enter pulse-skip mode in steady state if the load is light. The loop is powered by the input before V_{OUT} rises up to 1.7V. It is then powered by the output after V_{OUT} is higher than 1.7V.

Enable Control (EN)

The device operates when EN is high (>0.7V). In shutdown mode with a low EN voltage, the regulator stops switching and halts all internal control circuitry, and the DIS-FET turns off as well. This isolates the load from the input, so the output voltage can drop below the input voltage during shutdown.

Current Limit

The MP3416 uses current limit to prevent an inductor current runaway. If the inductor current triggers the current limit, the LS-FET is turned off immediately. When the load current increases, the inductor current triggers the limit level and limits the output energy. To prevent the LS-FET from running away, the max turn on time is limited to 10 μ s.

Short-Circuit and Overload Protection

Unlike most step-up converters, the MP3416 allows for short circuits on the output. In the event of a short circuit, the MP3416 enters hiccup protection. During an overload, V_{OUT} may drop to about 1.6V. If the load continues increasing, the MP3416 enters hiccup protection. If overload is defined as V_{OUT} higher than 1.6V but still smaller than $V_{IN}+0.2V$, the MP3416 treats this as down mode operation with current limit. The internal temperature of the MP3416 may rise, causing the device to enter OTP.

Low Battery Detection

The MP3416 includes one LBI pin to detect the battery voltage, and the function is active only when the device is enabled. LBI is connected to V_{IN} through the external resistor divider. If the LBI voltage is lower than 0.4V, LBO goes low to indicate the power failure. During application, the LBI voltage should always be higher than 0.2V; otherwise, the LBO function may indicate falsely.

Thermal Protection

The device has an internal temperature monitor. If the die temperature exceeds 155°C, the part stops working and restarts when the die temperature drops below 135°C.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see the Typical Application schematic on page 1). The feedback resistor (R_1) must account for both stability and dynamic response and should therefore be chosen carefully. Choose R_1 , and then calculate R_2 with Equation (1):

$$R_2 = \frac{V_{FB}}{V_{OUT} - V_{FB}} \times R_1 \quad (1)$$

Where $V_{FB}=0.504V$.

The feedback circuit is shown in Figure 2.

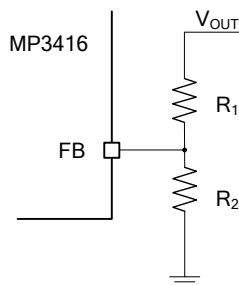


Figure 2: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Values for Common Output Voltages

$V_{OUT}(V)$	$R_1(k\Omega)$	$R_2(k\Omega)$
1.8	1000	383
3	1000	200
3.3	1000	178
5	1000	113

Input Capacitor Selection

Low ESR input capacitors reduce input switching noise and peak current drawn from the battery. Ceramic capacitors are recommended for input decoupling and should be located as close to the device as possible. A ceramic capacitor 10 μ F or larger is recommended to restrain the V_{IN} ripple.

Inductor Selection

The MP3416 can apply small surface-mounted chip inductors due to the 1.1A peak current. Because of the peak current and boundary conduction mode (BCM) control method, the values of the inductance affect the switching frequency. A larger inductance causes lower switching frequency and increases output ripple. A smaller inductance causes higher switching frequency and decreases efficiency.

Considering the efficiency and output ripple, a 1.5 μ H to 3.3 μ H inductor is recommended for most applications.

The inductor should have a low DCR to reduce resistive power loss. The saturated current (I_{SAT}) should be large enough to support the peak current.

Output Capacitor Selection

The output capacitor requires a minimum capacitance value of 22 μ F at the programmed output voltage to ensure stability over the full operating range. A higher capacitance value may be required to lower the output ripple and transient response. Low ESR capacitors such as X5R or X7R type ceramic capacitors are recommended. Supposing that ESR is zero, the minimum output capacitor to support the ripple in the boost mode can be calculated with Equation (2):

$$C_o \geq \frac{I_o \times (V_{OUT(MAX)} - V_{IN(MIN)})}{V_{OUT(MAX)} \times \Delta V \times f_{S(MIN)}} \quad (2)$$

Where $V_{OUT(MAX)}$ is the maximum output voltage, $V_{IN(MIN)}$ is the minimum input voltage, I_o is the output current, $f_{S(MIN)}$ is the minimum switching frequency, and ΔV is the acceptable output ripple.

PCB Layout Considerations

Efficient PCB layout is critical for switching power supplies with a high switching frequency. A poor layout can result in reduced performance, EMI problems, resistive loss, and system instability. For best results, refer to Figure 3 and Figure 4 and follow the guidelines below.

- 1) Place the output capacitor as close to OUT and GND as possible.
- 2) Place the input capacitor and inductor close to the IC.
- 3) Keep the SW trace as short and wide as possible.
- 4) Keep the feedback loop far away from noise sources, such as the SW trace.
- 5) Keep the feedback divider resistor as close to FB and GND as possible.
- 6) Tie the ground return of the input/output capacitor close to GND with a large GND copper area.
- 7) Add GND and vias on the bottom layer if the top layer GND connection between CIN, COUT, and IC-GND is narrow.

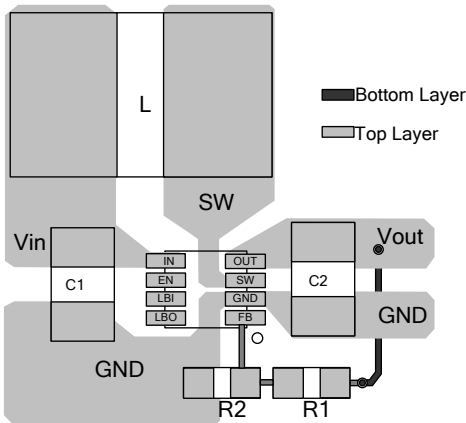


Figure 3: Recommended TSOT23 Layout

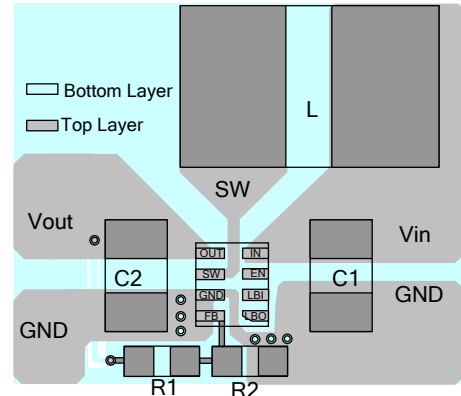


Figure 4: Recommended QFN Layout

Design Example

Table 2 is a design example following the application guidelines for the following specifications.

Table 2: Design Example

V _{IN}	1.25V to 5.5 V
V _{OUT}	3.3V
I _{OUT}	0A-0.1A ⁽⁷⁾

The typical application circuit for V_{OUT} = 3.3V in Figure 5 shows the detailed application schematic and is the basis for the typical performance waveforms. For more detailed device applications, please refer to the related evaluation board datasheets.

NOTE:

7) the load capability is higher when V_{IN} is relatively high, refer to the Maximum Output Current vs. Input Voltage curve on page 8.

TYPICAL APPLICATION CIRCUITS

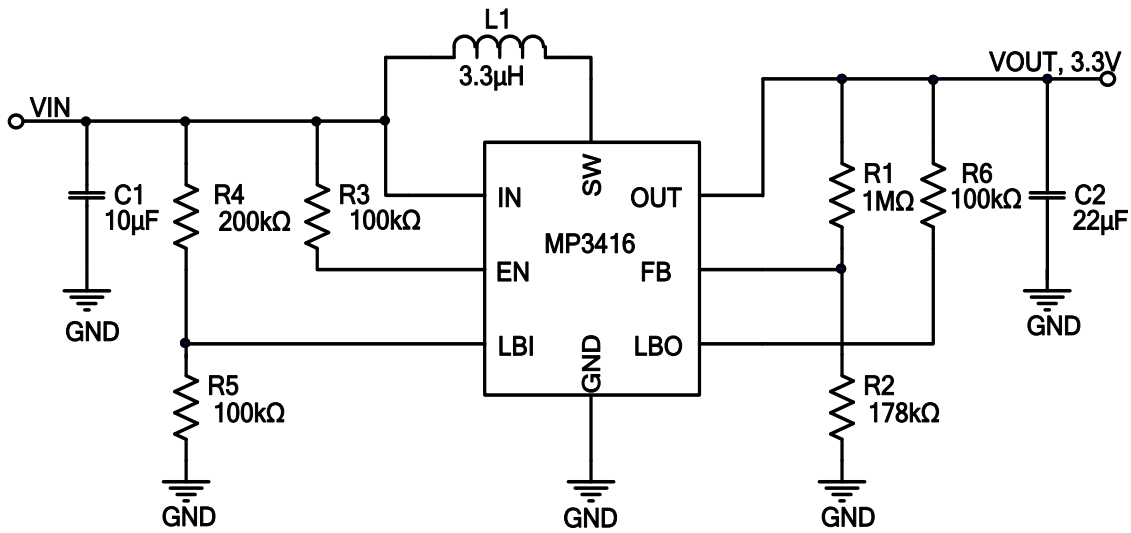


Figure 5: Typical Schematic for 3.3V Output

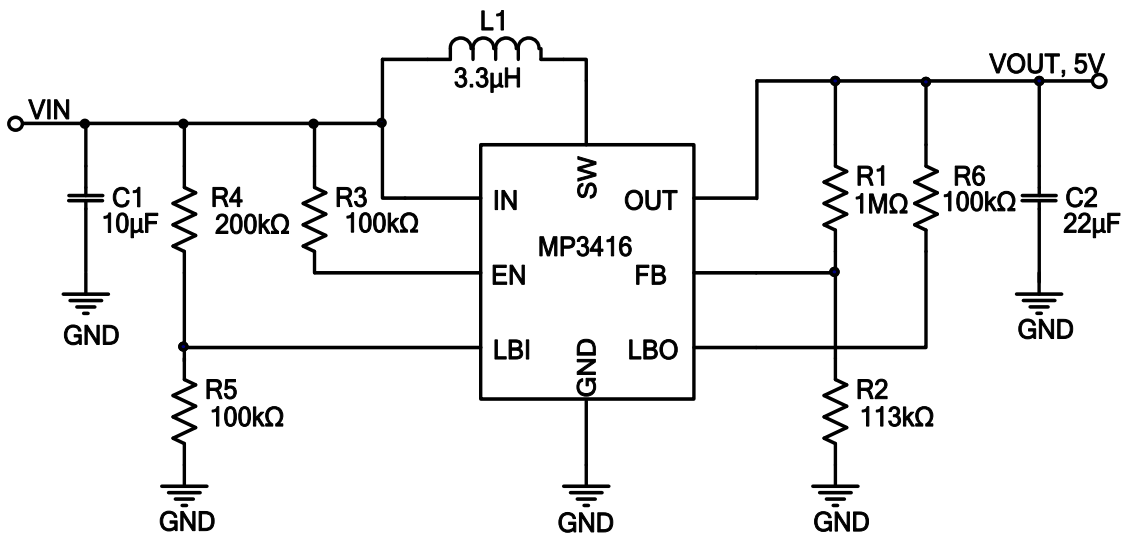
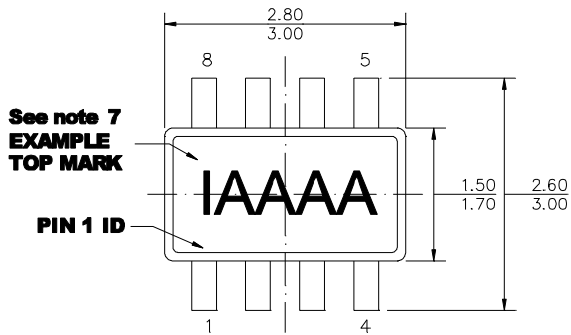
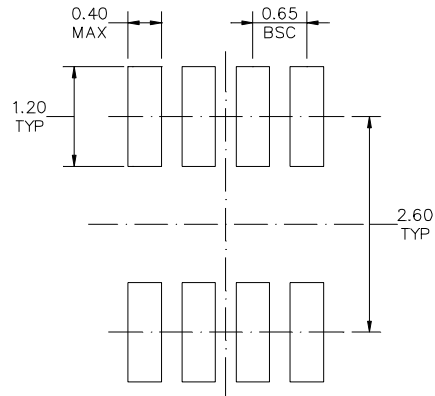
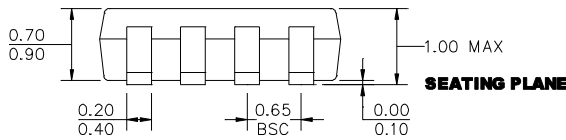
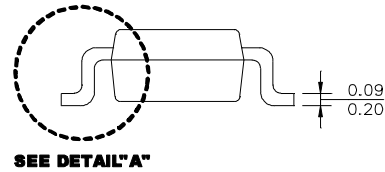
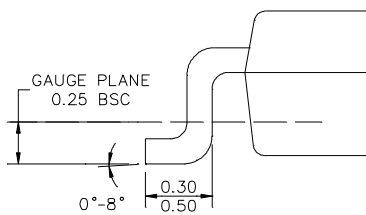
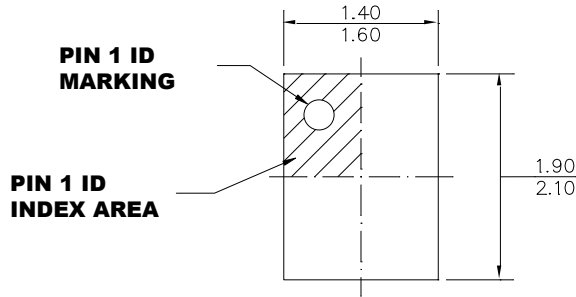
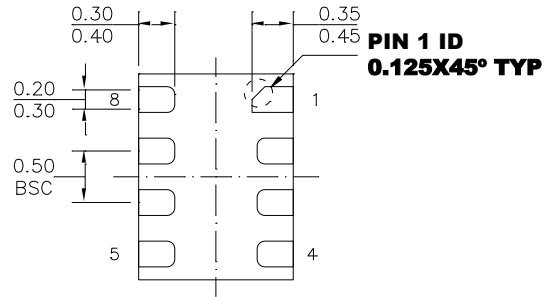
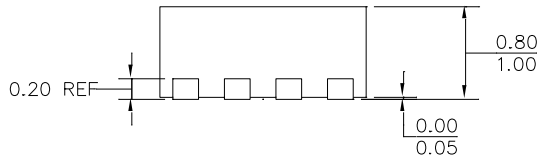
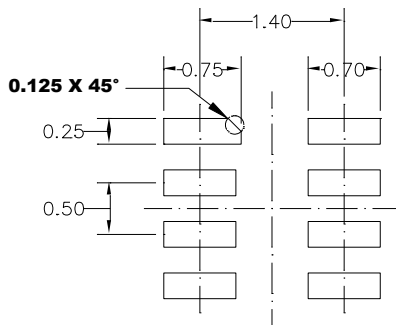


Figure 6: Typical Schematic for 5V Output

PACKAGE INFORMATION
TSOT23-8

TOP VIEW

RECOMMENDED LAND PATTERN

FRONT VIEW

SIDE VIEW

DETAIL "A"
NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) JEDEC REFERENCE IS MO193, VARIATION BA
- 6) DRAWING IS NOT TO SCALE
- 7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT (SEE EXAMPLE TOP MARK)

PACKAGE INFORMATION(continued)

QFN-8 (1.5mmx2.0mm)

TOP VIEW

BOTTOM VIEW

SIDE VIEW

RECOMMENDED LAND PATTERN
NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

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