MP3424

Current Programmable, CC/CV, Synchronous, Step-Up Converter with Output Disconnect

The Future of Analog IC Technology

DESCRIPTION

The MP3424 is a high-efficiency, synchronous, current-mode, step-up converter with output disconnect. The MP3424 targets various load capability boosts from a battery input with an accurate load current limit.

The MP3424 starts up from an input voltage as low as 2V while providing inrush current limiting, output short-circuit protection (SCP), and programmable load current limit. The integrated P-channel synchronous rectifier improves efficiency and eliminates the need for an external Schottky diode. The P-channel MOSFET disconnects the output from the input during shutdown.

The 580kHz switching frequency allows for small external components, while internal compensation and soft-start minimize the external component count. The MP3424 provides flexible current limit programming for up to 5V/3.1A load from a supply voltage down to 2.8V.

The MP3424 is available in a QFN-14 (2mmx2mm) package.

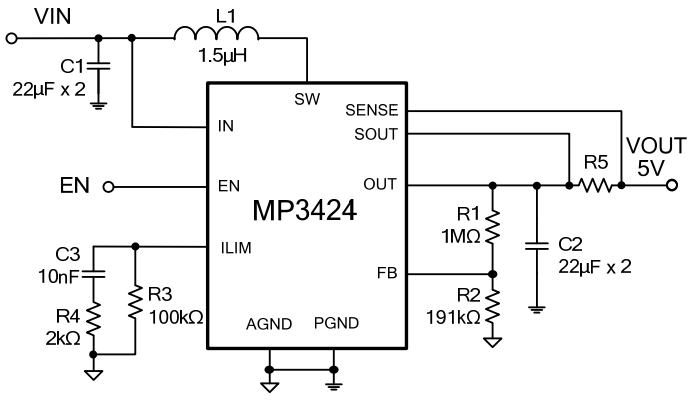
FEATURES

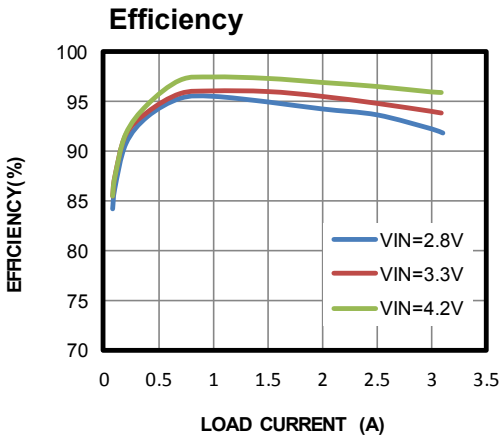
- 2V to 5.5V Input Work Range
- 3V to 5.5V Output Range
- Supports 5V/3.1A Output from 2.8V Input
- Programmable up to 9.5A Switching Current Limit
- Programmable Average Load Current Limit
- 580kHz Fixed Frequency Switching
- Up to 97% Efficiency
- Internal Soft Start and Compensation
- True Output Load Disconnect from Input
- Over-Current Protection (OCP), Short-Circuit Protection (SCP), and Over-Temperature Protection (OTP)
- Available in a QFN-14 (2mmx2mm) Package

APPLICATIONS

- Battery-Powered Products
- Power Bank, Juice Packs, Battery Back-Up Units
- Electronic Cigarettes
- USB Power Supplies
- Consumer Electronic Accessories

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP3424GG	QFN-14 (2mmx2mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP3424GG–Z)

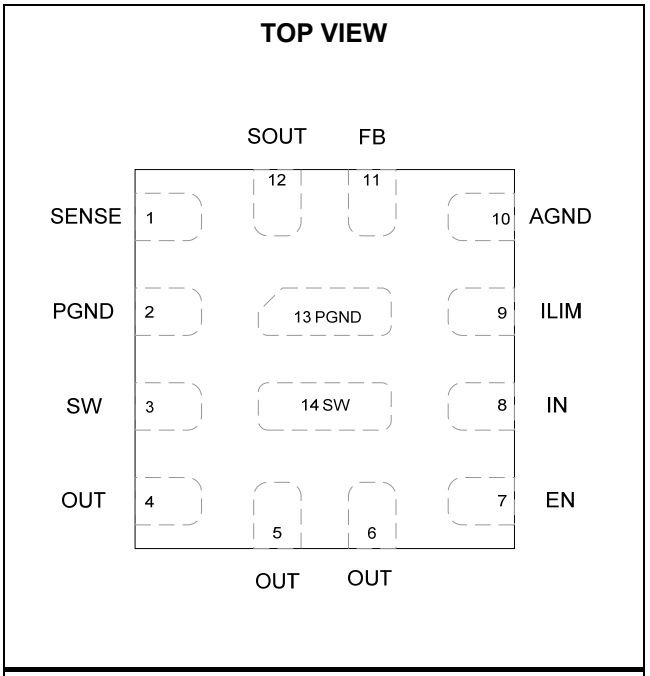
TOP MARKING

DTY

LLL

DT: Product code of MP3424GG
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



QFN-14 (2mmx2mm)

ABSOLUTE MAXIMUM RATINGS (1)

SW pin.....-0.3V to +6.5V (10V for <5ns)
All other pins .....-0.3V to +6.5V
Continuous power dissipation (T_A = +25°C) (2)
..... 2.55W (4)
Junction temperature ..... 150°C
Lead temperature..... 260°C
Storage temperature.....-65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 2V to 5.5V
V_{OUT} ..... 3V to 5.5V
Operating junction temp. (T_J)....-40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}	
QFN-14 (2mmx2mm)			
EV3424-G-00A (4)	49	14	°C/W
JESD51-7 (5)	80	16	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV3424-G-00A, 2-layer 64mmx64mm PCB.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 5V, T_J = -40°C to 125°C [6], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Voltage Range						
Quiescent current	I_Q	V_{EN} = V_{IN} = 3.3V, V_{OUT} = 5V, V_{FB} = 0.85V, no switching, measured on OUT		320		µA
		V_{EN} = V_{IN} = 3.3V, V_{OUT} = 5V, V_{FB} = 0.85V, no switching, measured on IN		13.5		µA
Shutdown current	I_{SD}	V_{EN} = V_{OUT} = 0V, measured on IN, T_J = 25°C		0.1	1	µA
IN UVLO rising threshold	$V_{UVLO-IN-R}$	V_{IN} rising, V_{OUT} = 0V, T_J = 25°C		1.2	1.45	V
IN UVLO falling threshold	$V_{UVLO-IN-F}$	V_{IN} falling, V_{OUT} = 5V		0.61		V
V_{OUT} start switching rising threshold	$V_{UVLO-OUT-R}$			1.7	1.95	V
Step-Up Converter						
Operation frequency	F_{SW}	T_J = 25°C	500	580	660	kHz
		-40°C ≤ T_J ≤ 125°C	460	580	700	
Feedback voltage reference	V_{FB}	T_J = 25°C	794	805	816	mV
		-40°C ≤ T_J ≤ 125°C	790	805	820	mV
Feedback input current	I_{FB}	V_{FB} = 850mV		1	50	nA
N-FET on resistance	R_{NDS-ON}			11		mΩ
N-FET leakage current	I_{N-LK}	V_{SW} = 5V		0.1		µA
P-FET on resistance	R_{PDS-ON}			17		mΩ
P-FET leakage current	I_{P-LK}	V_{SW} = 5V, V_{OUT} = 0V		0.1		µA
Maximum duty cycle	D_{MAX}		90	95		%
Linear charge current limit	$I_{CH-LIMIT}$	V_{IN} = 2V, V_{OUT} = 0V		0.25		A
		V_{IN} = 2V, V_{OUT} = 1.2V		1.15		A
N-FET current limit [7]	$I_{SW-LIMIT}$	R_{ILIM} = 100kΩ, V_{IN} = 3V, V_{OUT} = 5V		9.5		A
OUT average current limit threshold	V_{OCL}		26.5	30	33.5	mV
Logic Interface						
EN high-level voltage	V_{EN-H}	Rising	1.2			V
EN low-level voltage	V_{EN-L}	Falling			0.4	V
EN input current	I_{EN}	Connect to V_{IN}		10		nA
Protection						
Thermal shutdown [7]				150		°C
Thermal shutdown hysteresis [7]				20		°C

NOTES:

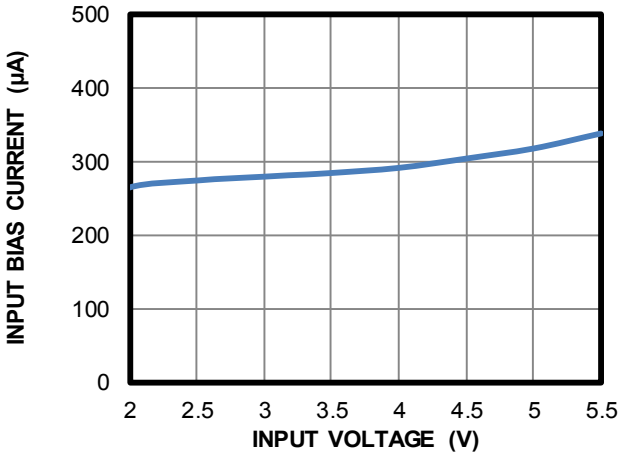
6) Guaranteed by over-temperature correlation, not tested in production.
7) Guaranteed by sample characterization, not tested in production.

TYPICAL CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

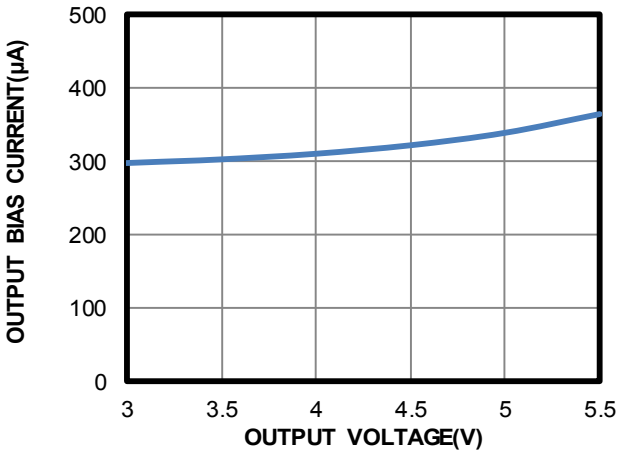
Quiescent Current vs. Input Voltage

$V_{IN} > V_{OUT}$



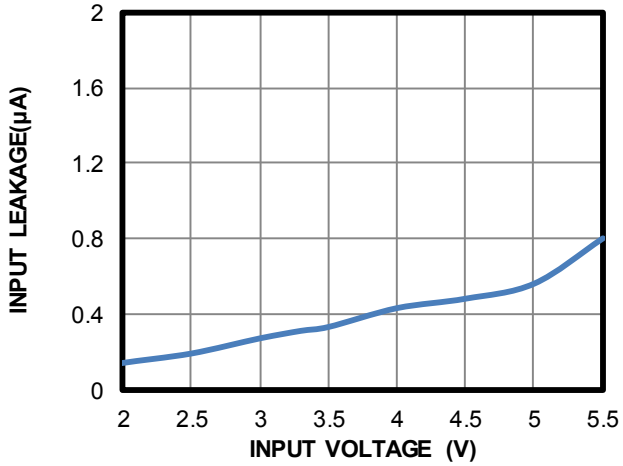
Quiescent Current vs. Input Voltage

$V_{OUT} > V_{IN}$

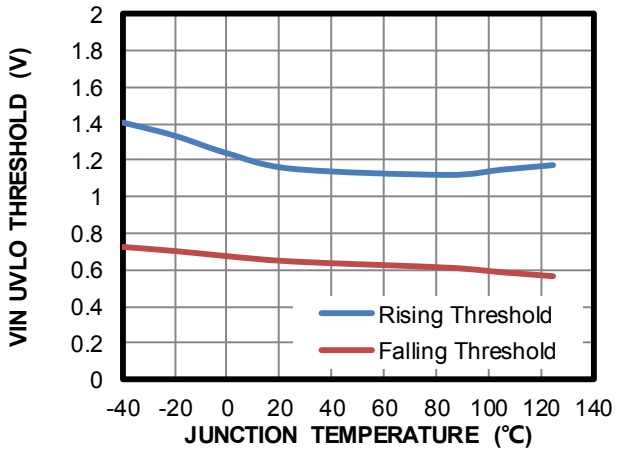


Shutdown Current vs. Input Voltage

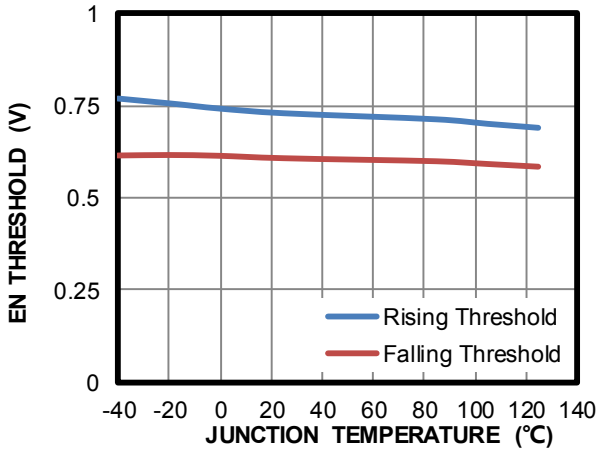
EN = low



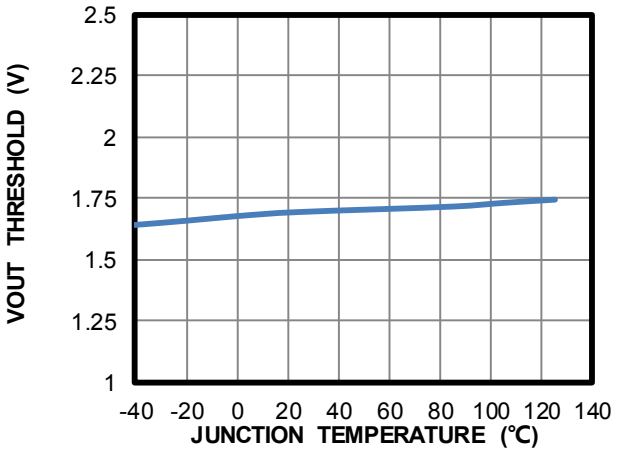
Input UVLO Threshold vs. Temperature



EN Threshold vs. Temperature



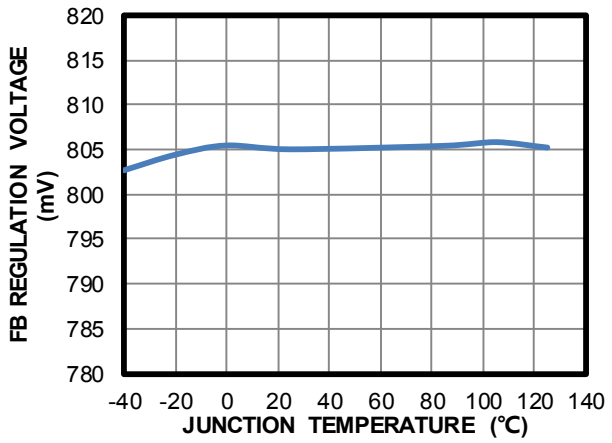
V_{OUT} Rising Threshold for Switching vs. Temperature



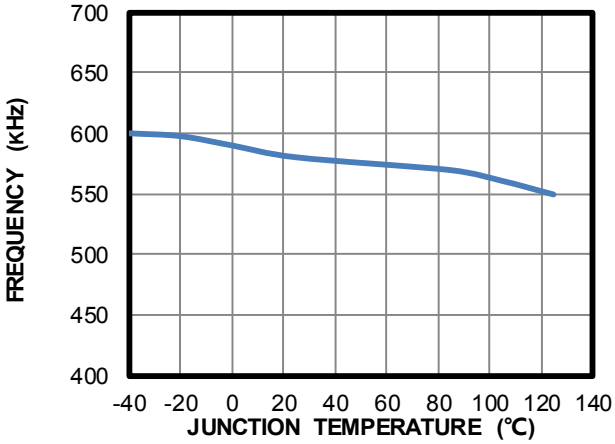
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

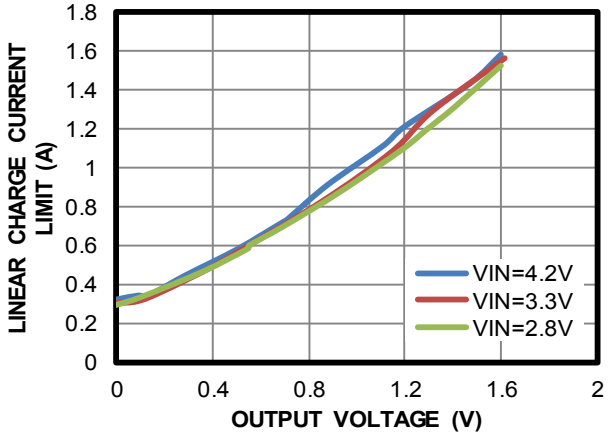
Feedback Voltage vs. Temperature



Frequency vs. Temperature

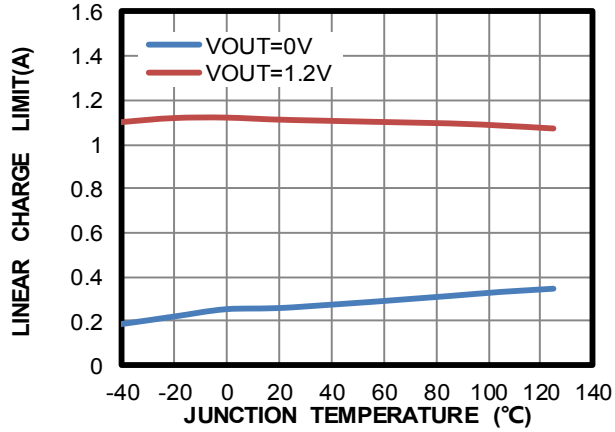


Linear Charging Current Limit vs. Output Voltage



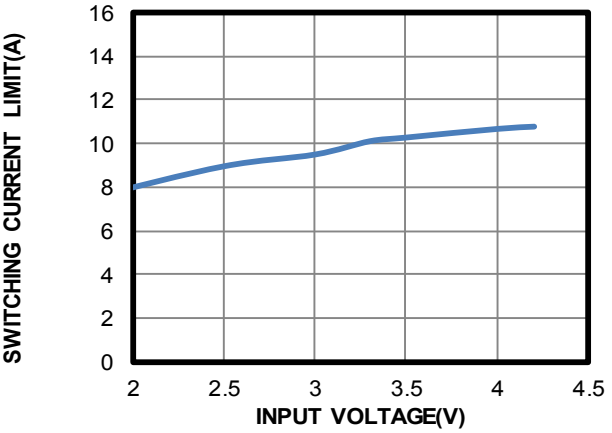
Linear Charging Current Limit vs. Temperature

V_{IN} = 2V

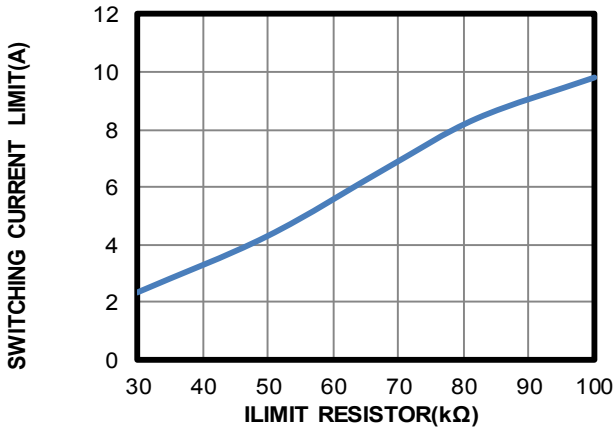


Switching Current Limit vs. Input Voltage

R_{LIMIT} = 100kΩ



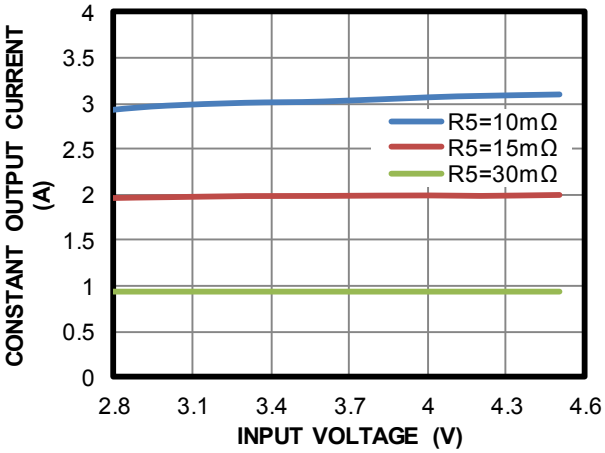
Switching Current Limit vs. I_{LIMIT} Resistor



TYPICAL CHARACTERISTICS *(continued)*

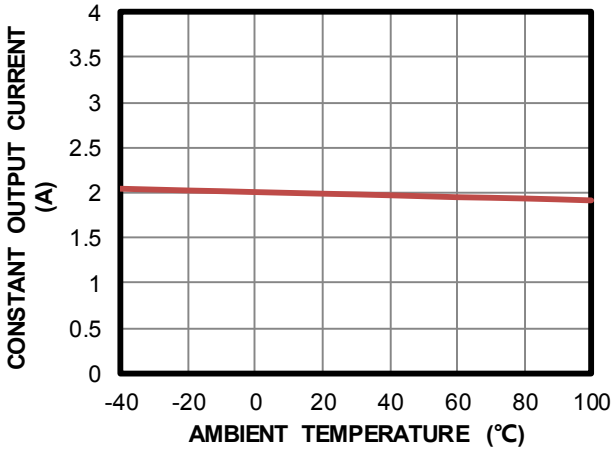
V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

Constant Output Current vs. Input Voltage



Constant Output Current vs. Ambient Temperature

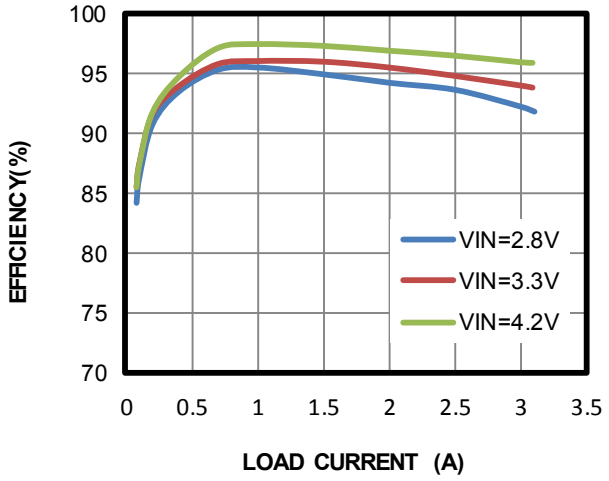
R5 = 15mΩ



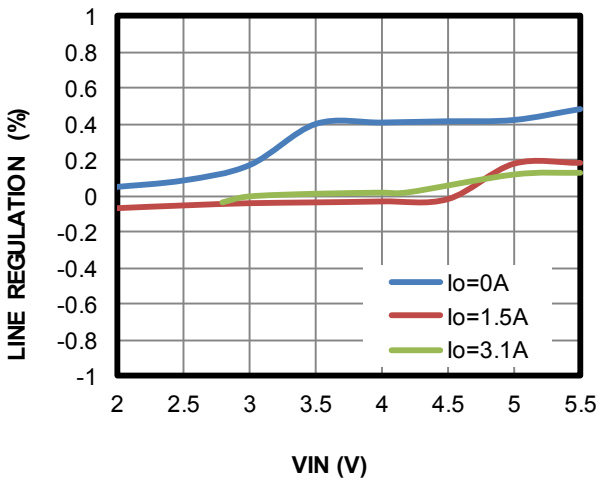
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

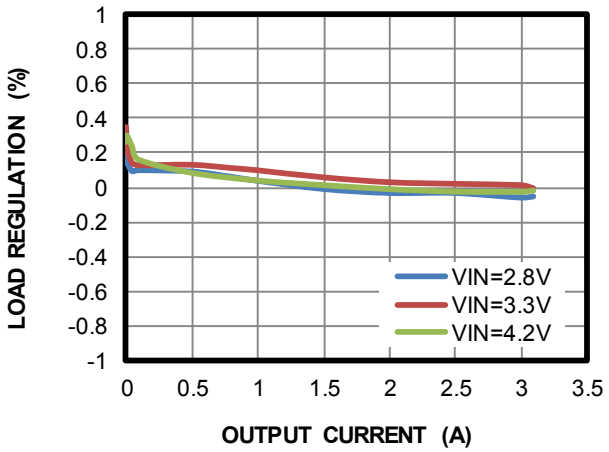
Efficiency vs. Load Current



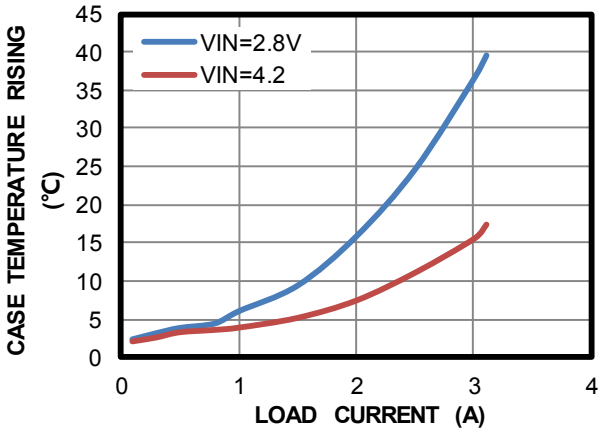
Line Regulation



Load Regulation



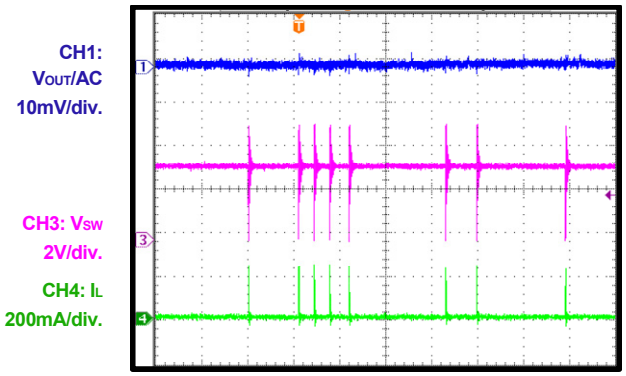
Case Temperature Rising vs. Load Current



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

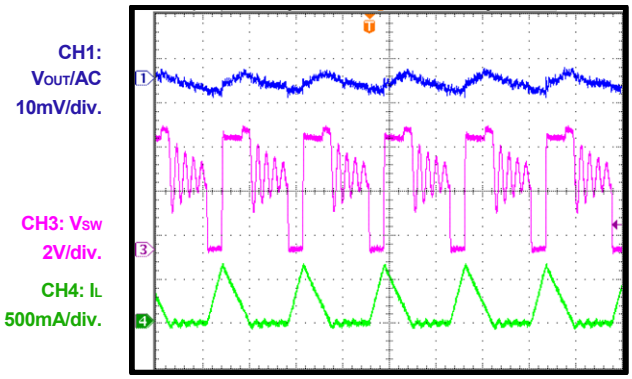
V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

Output Voltage Ripple
Load = 0A



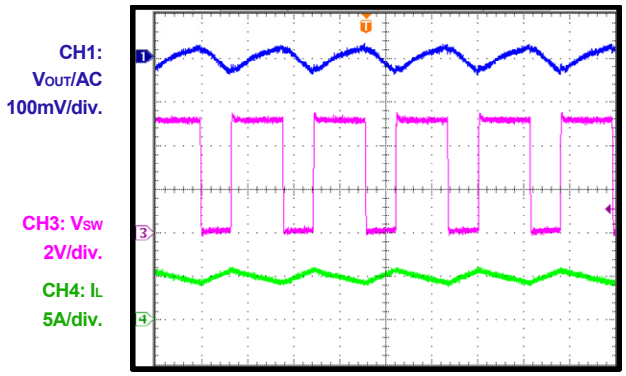
20µs/div.

Output Voltage Ripple
Load = 0.1A



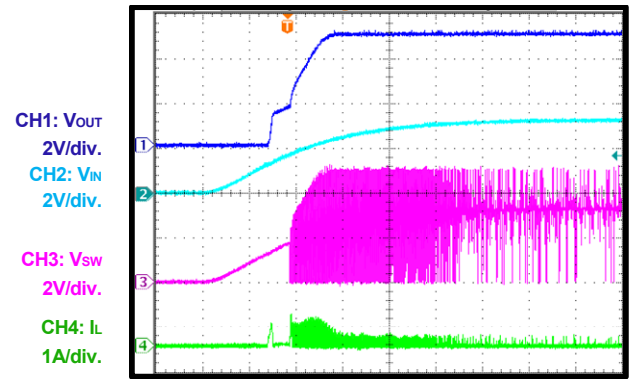
1µs/div.

Output Voltage Ripple
Load = 3.1A



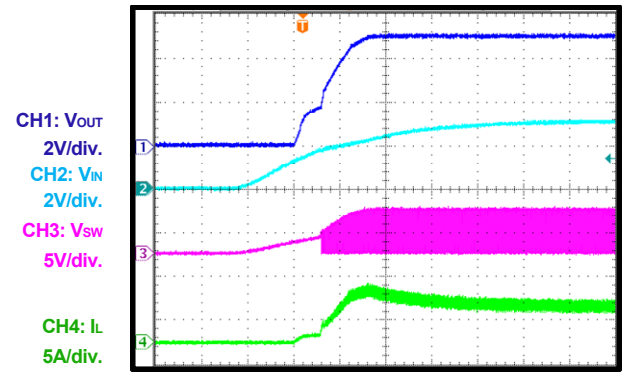
1µs/div.

V_{IN} Start-Up
Load = 0A



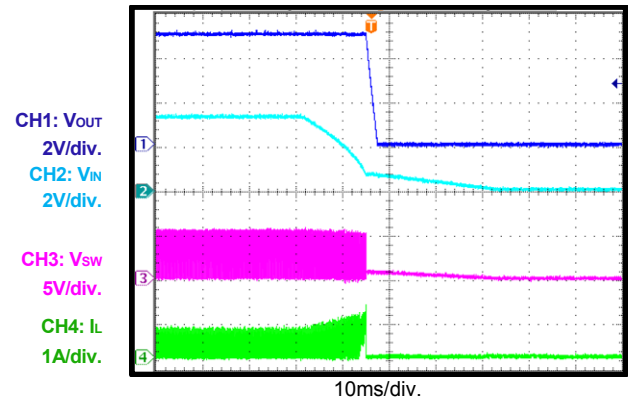
2ms/div.

V_{IN} Start-Up
Load = 2Ω



2ms/div.

V_{IN} Shutdown
Load = 0.1A

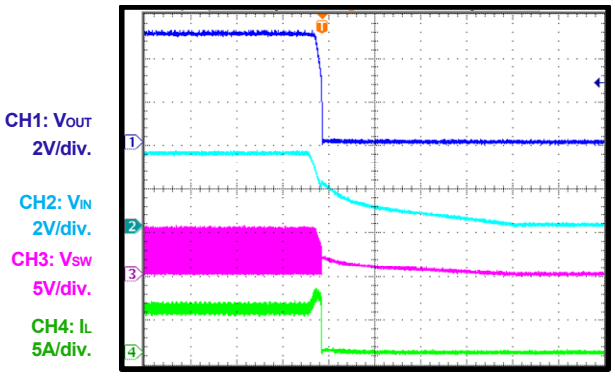


10ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

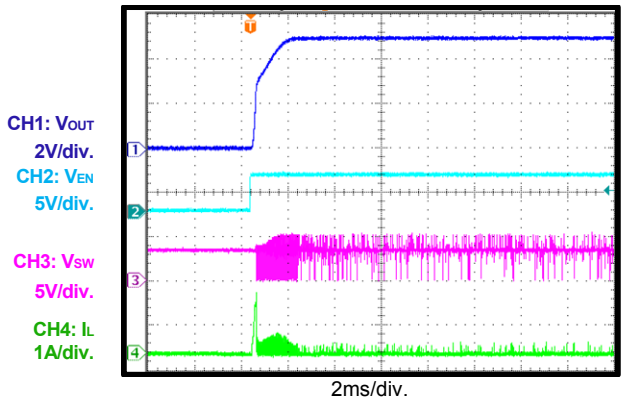
V_{IN} = 3.3V, V_{OUT} = 5V, L=1.5µH, T_A = 25°C, unless otherwise noted.

V_{IN} Shutdown
Load = 3.1A



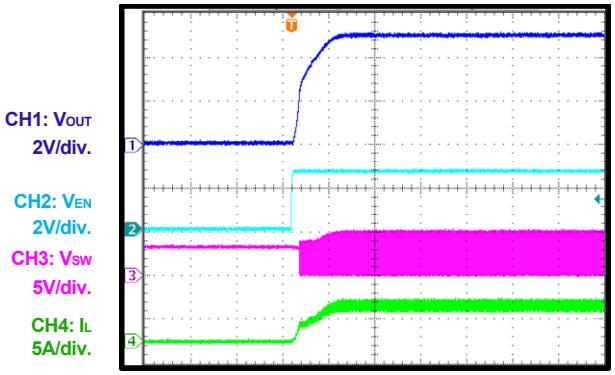
10ms/div.

EN Start-Up
Load = 0A



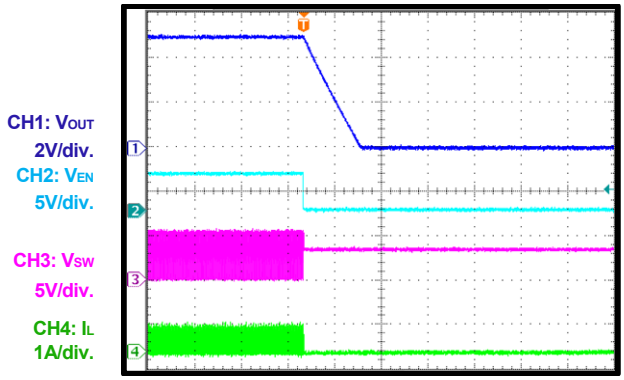
2ms/div.

EN Start-Up
Load = 2Ω



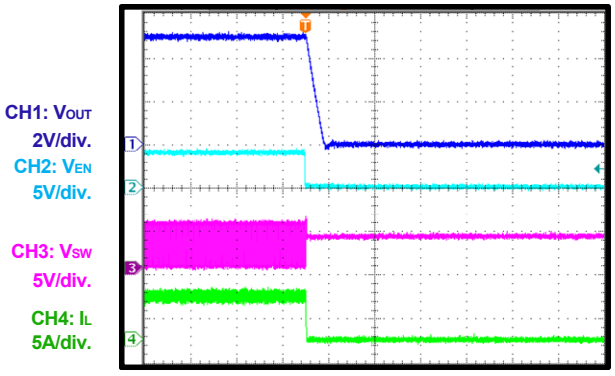
2ms/div.

EN Shutdown
Load = 0.1A



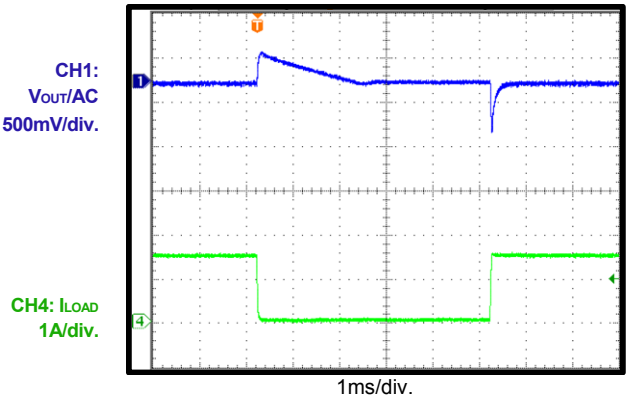
2ms/div.

EN Shutdown
Load = 3.1A



200µs/div.

Load Transient
I_{LOAD} = 0 - 1.5A at 150mA/µs



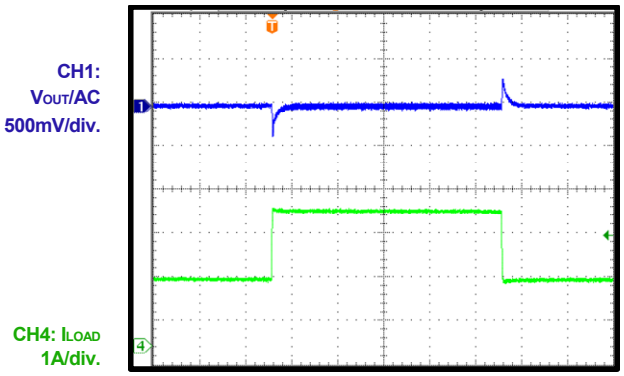
1ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

Load Transient

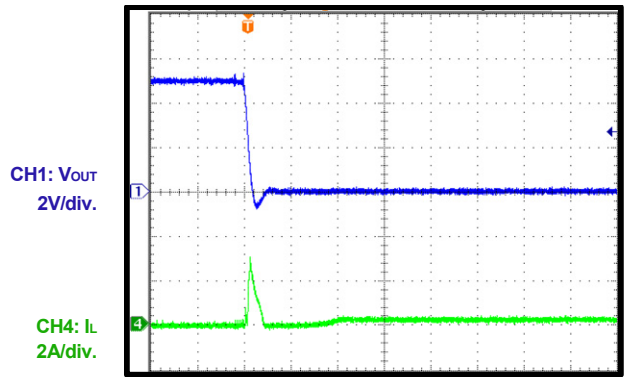
I_{LOAD} = 1.5 - 3.1A at 150mA/µs



1ms/div.

Short-Circuit Entry

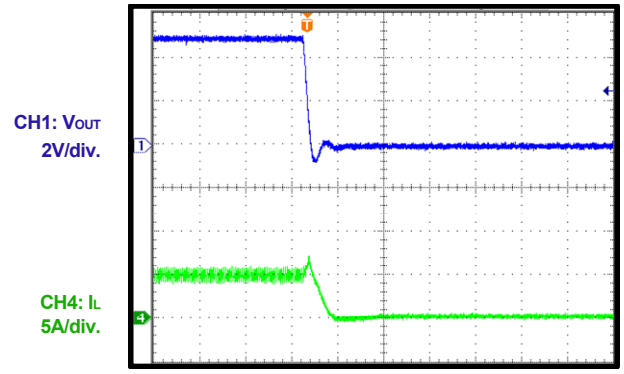
0A load to short



40µs/div.

Short-Circuit Entry

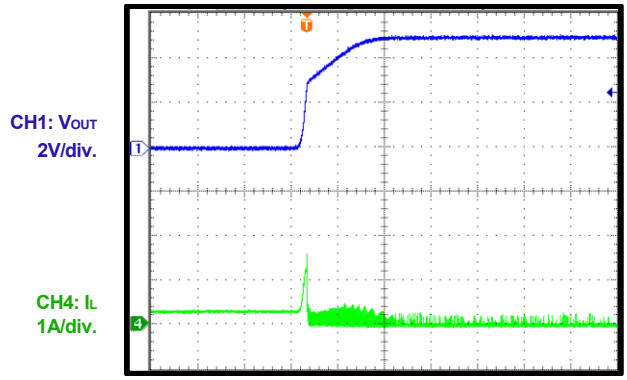
3.1A load to short



40µs/div.

Short-Circuit Recovery

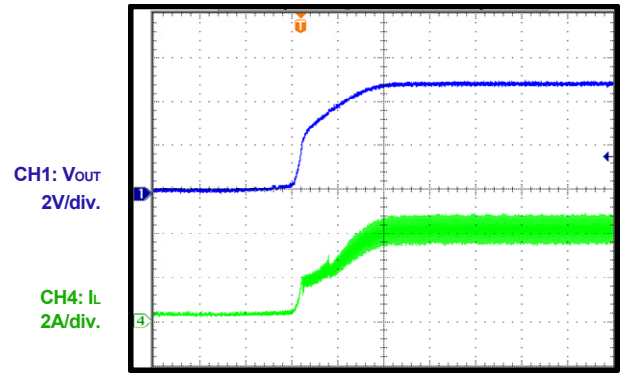
Recover to 0A load



1ms/div.

Short-Circuit Recovery

Recover to 2Ω load



1ms/div.

PIN FUNCTIONS

Pin #	Name	Description
1	SENSE	**Load current sense.** Connect a load sense resistor signal between SENSE and SOUT to determine the maximum load current. If average load current limit isn't needed, connect SENSE and SOUT to VOUT directly.
2, 13	PGND	**Power ground.**
3, 14	SW	**Power switch output.** SW is the connection node of the internal N-channel MOSFET switch and synchronous P-channel MOSFET switch. Connect the power inductor between SW and the input power. Keep the PCB trace lengths as short and wide as possible to reduce EMI and voltage spikes.
4, 5, 6	OUT	**Output.** OUT is the drain of the internal synchronous rectifier MOSFET. Bias is derived from OUT when V_{OUT} is higher than V_{IN}. The PCB trace length from OUT to the output filter capacitor should be as short and wide as possible. OUT is completely disconnected from IN when EN is low due to the output disconnect feature.
7	EN	**Chip enable control input.**
8	IN	**Power supply input.** The start-up bias is derived from IN. IN must be bypassed locally. Once OUT exceeds IN, the bias comes from OUT. Once started, operation is completely independent from IN.
9	ILIM	**Switch current limit set.** A resister from ILIM to AGND programs the low-side MOSFET cycle-by-cycle peak current limit when the output constant load current limit is not triggered. When the output current signal between SOUT and SENSE is higher than the current limit threshold, ILIM is pulled low to regulate the average load current. R-C compensation is needed in this condition. If average load current limit isn't needed, the R-C compensation can be removed, only a resister from ILIM to AGND is ok.
10	AGND	**Analog signal ground.**
11	FB	**Feedback input to error amplifier.** Connect a resistor divider tap to FB. The output voltage can be adjusted from 3V to 5.5V.
12	SOUT	**Load current sense.** Connect a load sense resistor signal between SOUT and SENSE to determine the maximum load current. If average load current limit isn't needed, connect SENSE and SOUT to VOUT directly.

BLOCK DIAGRAM

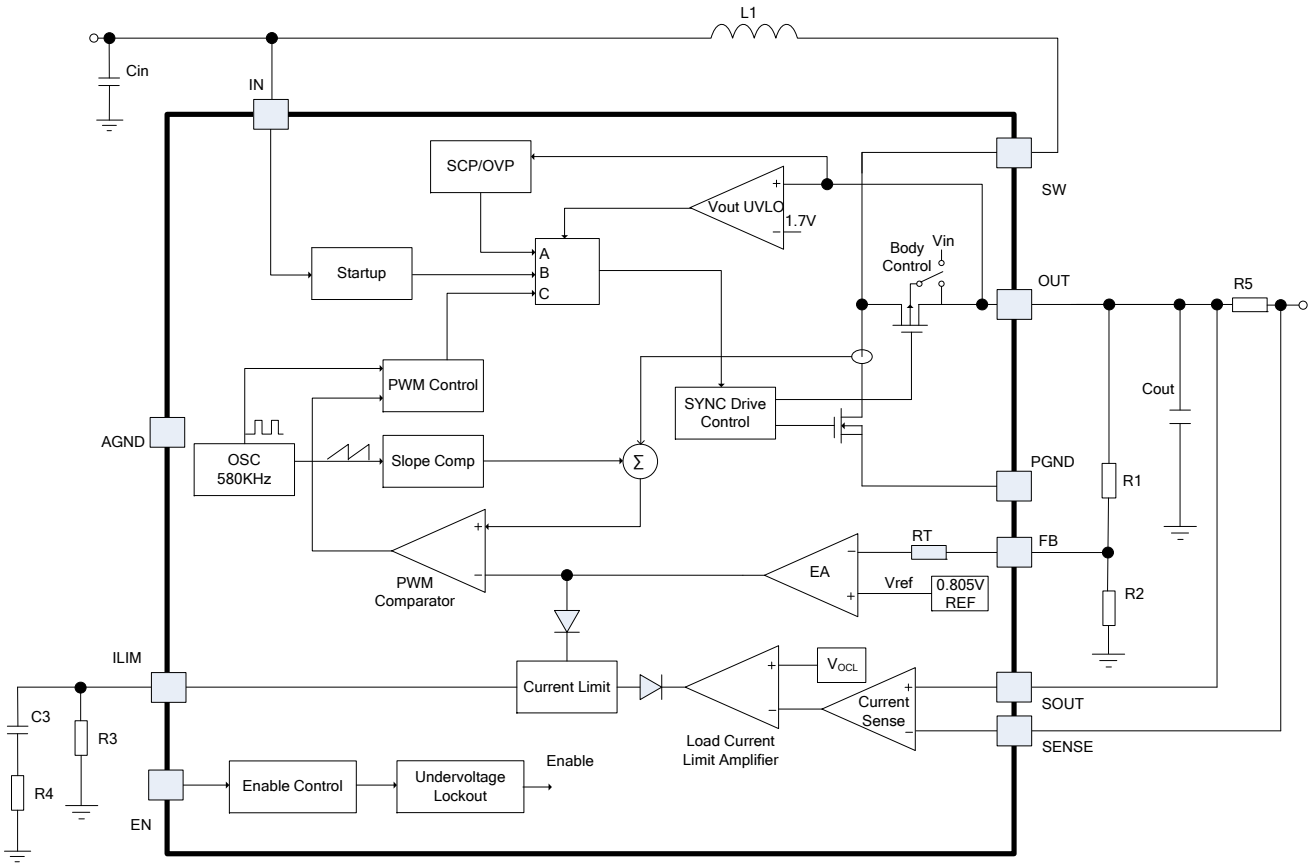


Figure 1: Functional Block Diagram

OPERATION

The MP3424 is a 580kHz, synchronous, step-up converter with true output disconnect packaged in a QFN-14 (2mmx2mm) package. The device features fixed-frequency current mode pulse-width modulation (PWM) control for excellent line and load regulation. Special voltage and current loop provide flexibility for voltage regulation and overload protection. Internal soft start and loop compensation simplify the design process and minimize the external component count. The internal low $R_{DS(ON)}$ MOSFETs enable the device to maintain high efficiency over a wide load current range.

Start-Up

When the IC is enabled and the IN voltage exceeds $V_{UVLO-IN-R}$, the MP3424 starts up in linear charge mode. During this linear charge period, the rectifier P-channel MOSFET (P-FET) turns on until the output capacitor is charged to 1.7V. The P-FET current is limited to 0.25A when V_{OUT} is 0V to avoid inrush current. While V_{OUT} ramps up, the P-FET current limit also increases and ramps up to 1.15A linearly at a 1.2V V_{OUT} condition. This circuit also helps limit the output current under short-circuit conditions.

Once the output is charged to 1.7V, the linear charge period elapses, and the MP3424 starts switching in normal closed-loop operation. In normal operation, if V_{OUT} is lower than V_{IN} + 0.3V, the MP3424 operates in down mode. If V_{OUT} is higher than V_{IN} + 0.3V, the MP3424 operates in boost mode. The switching current limit in both down mode and boost mode are programmed by R_{ILIM} between ILIM and GND. At the same time, R_{ILIM} must always be lower than 100kΩ. Figure 2 and Table 1 show the work mode and current limit during the start-up process.

Table 1: Work Mode during Start-Up

V_{OUT} < 1.7V	Linear charge mode
V_{OUT} ≥ 1.7V, V_{OUT} < V_{IN} + 0.3V	Down mode
V_{OUT} ≥ 1.7V, V_{OUT} ≥ V_{IN} + 0.3V	Boost mode

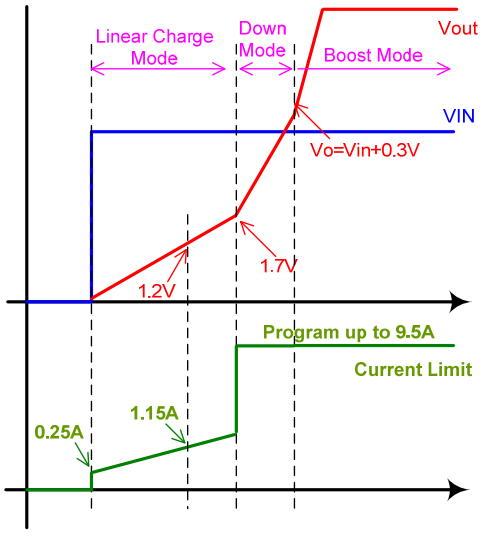


Figure 2: Current Limit and Work Mode during Start-Up

In down mode, the gate of the high-side MOSFET (HS-FET) is pulled to V_{IN} and works with high impedance when the HS-FET is on. The power-loss is high in down mode. Down mode is designed to work during start-up and SCP. It is not recommended to operate the MP3424 in down mode for normal work, unless the system performance will not be affected by the temperature rise.

When the output voltage exceeds the input voltage, the MP3424 powers internal circuits from V_{OUT} instead of V_{IN}.

Soft Start (SS)

The MP3424 provides soft start by charging an internal capacitor with a current source. This soft-start voltage rises, following the FB voltage (V_{FB}) during a linear charge period. Once the linear charge period elapses, the voltage on this capacitor is charged by a fixed internal current, and the reference voltage ramps up slowly. The reference soft-start time is typically 3ms from 0V to 0.805V.

The soft-start capacitor is discharged completely in the event of a commanded shutdown, thermal shutdown, or a short circuit at the output.

Device Enable (EN)

Operation is enabled when EN is switched high. The MP3424 enters shutdown mode when EN is low. In shutdown mode, the regulator stops switching, all internal control circuitry turns off, and the load is isolated from the input.

Error Amplifier (EA)

The error amplifier (EA) is an internally compensated amplifier. The EA compares the internal 0.805V reference voltage (V_{REF}) against V_{FB} to generate an error signal. The output voltage of the MP3424 can be adjusted by an external resistor divider.

Output Disconnect

The MP3424 is designed to allow for true output disconnect by eliminating body diode conduction of the internal P-FET rectifier. This allows V_{OUT} to drop to 0V during shutdown, or V_{IN} to be isolated when maintaining an external bias on V_{OUT}. This limits the inrush current limit at start-up, minimizing surge current seen by the input supply. To obtain the advantage of the output disconnect, there cannot be an external Schottky diode connected between SW and V_{OUT}.

Overload and Short-Circuit Protection (SCP)

When overload occurs, the inductor current is limited cycle-by-cycle, and the output voltage drops. If V_{OUT} drops below V_{IN} + 0.3V, the MP3424 runs back into down mode. When V_{OUT} drops below 1.7V, the MP3424 runs into linear charge mode.

At the same time, if V_{OUT} drops below 50% of the nominal output voltage, the MP3424 treats this as a short-circuit condition and shuts down immediately. The MP3424 restarts after 40μs as a new power-on cycle after short-circuit protection (SCP). If V_{OUT} is higher than 50% of the setting voltage in overload condition, the MP3424 does not treat this as a short-circuit condition. The current is only controlled by cycle-by-cycle switching current limiting or an output current sense resistor. Refer to the Constant Output Current Limit section for details on accurate current limit setting.

Constant Output Current Limit

The MP3424 integrates programmable current limit functions, including cycle-by-cycle current limiting and output load current limiting.

By connecting ILIM to AGND through a resistor, the MP3424 limits the low-side MOSFET (LS-FET) current cycle-by-cycle, and the switching peak current can be programmed by changing R_{ILIM}. The load current capability is affected by the input voltage, output voltage, and inductance.

By inserting a sense resistor between the output capacitor and load terminal, the MP3424 can sense and limit the load current flowing through the current sense resistor. The limited load current is $30mV/R_{SENSE}$ (R5 in the schematic). When the load current limit is triggered, the ILIM voltage is pulled low internally, which controls the inductor current, regulating the average load current. When using an output sense resistor, R-C compensation is necessary on ILIM.

Different load current limits can be achieved by changing R_{ILIM} or the output sense resistor value. Typically, it is recommended to connect a 100kΩ resistor from ILIM to AGND and change the average current sense resistor on the output port to set the average current limit.

If the load current limit isn't needed, connect the SENSE and SOUT to VOUT directly, and the R-C compensation on ILIM can be removed.

The switching current signal is blanked for 70ns internally to enhance noise rejection. The average load current limit does not respond to the load change quickly due to the low-pass filter.

Over-Voltage Protection (OVP)

If V_{OUT} is higher than 6.5V, boost switching stops. This prevents an over-voltage condition from damaging the internal power MOSFET. When the output drops below 6.5V, the device resumes switching automatically.

Thermal Shutdown

The device contains an internal temperature monitor. The switches turn off if the die temperature exceeds 150°C. The device resumes normal operation when the die drops below 130°C.

APPLICATION INFORMATION

Setting the Output Voltage

The output voltage is fed back through a resistor divider. The feedback reference voltage is 0.805V, typically. Calculate the output voltage with Equation (1):

$$V_{OUT} = V_{REF} \times (1 + \frac{R1}{R2}) \quad (1)$$

Where R1 is the top feedback resistor, R2 is the bottom feedback resistor, and V_{REF} is the reference voltage (typically 0.805V).

Set the value of R1 and R2 as high as desired to achieve a low quiescent current. However, setting the resistance too high leads to noise and a low-loop bandwidth. An R1 value between 600kΩ to 1MΩ is recommended for good leakage, stability, and transient balance.

Selecting the Current Limit Resistor

Peak Switching Current Limit

The MP3424 limits the LS-FET cycle-by-cycle current with a current-limit resistor (R_{ILIM}). The switching peak current can be programmed by changing R_{ILIM}.

Load Average Current Limit

The MP3424 can sense and limit the load current flowing through a current sense resistor. R_{SENSE} connected from the output capacitor to the load terminal sets the load current limit (I_{OCL}) and can be estimated with Equation (2):

$$I_{OCL} = V_{OCL} / R_{SENSE} \quad (2)$$

Where V_{OCL} is 30mV (typically), I_{OCL} is the load current limit (in A), and R_{SENSE} is the sense resistor (in Ω) (R5 in the schematic).

Use an R-C compensation net on ILIM to regulate the stable load current limit loop. Typically, a 2kΩ resistor and 10nF capacitor are recommended.

Input Capacitor Selection

Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. Ceramic capacitors are recommended for input decoupling and should be placed as close to the device as possible. A ceramic capacitor larger than 22μF is recommended to restrain V_{IN} ripple.

Output Capacitor Selection

The output capacitor requires a minimum capacitance value of 22μF at the programmed output voltage to ensure stability over the entire operating range. A higher capacitance value may be required to lower the output ripple and transient ripple. Use low ESR capacitors such as X5R or X7R type ceramic capacitors. Supposing that the ESR is zero, the minimum output capacitor to support the ripple in PWM mode can be calculated with Equation (3):

$$C_O \geq \frac{Io \times (V_{OUT(MAX)} - V_{IN(MIN)})}{f_S \times V_{OUT(MAX)} \times \Delta V} \quad (3)$$

Where $V_{OUT(MAX)}$ is the maximum output voltage, $V_{IN(MIN)}$ is the minimum input voltage, I_O is the output current, f_S is the switching frequency, and ΔV is the acceptable output ripple.

A 1μF ceramic capacitor is recommended between OUT and PGND. This reduces spikes on the SW node and improves EMI performance.

Selecting the Inductor

The MP3424 can utilize small surface mount chip inductors due to its 580kHz switching frequency. Inductor values between 1μH and 2.2μH are suitable for most applications. Larger inductance values allow for slightly greater output current capability by reducing the inductor ripple current also increases component size. The minimum inductance value can be calculated with Equation (4):

$$L \geq \frac{V_{IN(MIN)} \times (V_{OUT(MAX)} - V_{IN(MIN)})}{V_{OUT(MAX)} \times \Delta I_L \times f_S} \quad (4)$$

Where ΔI_L is the acceptable inductor current ripple.

The inductor current ripple is set for 30% to 40% of the maximum inductor current, typically. The inductor should have a low DCR to reduce resistive power loss. The saturated current (I_{SAT}) should be large enough to support the peak current.

PCB Layout Guidelines

Efficient PCB layout of the high frequency switching power supplies is critical for stable operation. Poor layout may result in reduced performance, excessive EMI, resistive loss, and system instability. For best results, refer to Figure 3 and follow the guidelines below.

1. Place the output capacitor as close to OUT as possible with minimal distance to PGND.
2. Place a small decoupling capacitor in parallel with the bulk output capacitor and as close to OUT as possible.
   This is very important for reducing the spikes on SW and improving EMI performance.
3. Place the input capacitor and inductor as close to IN and SW as possible.
4. Keep the trace between the inductor and SW as wide and short as possible.
5. Keep the FB feedback loop far away from all noise sources, such as SW.
6. Place the feedback resistor dividers as close to FB and AGND as possible.
7. Connect the current sensing traces (SOUT and SENSE) from the pad of sense resistor routed in parallel closely with a small closed area far away from noise sources such as the SW trace.
8. Place the ILIM set and compensation net close to ILIM and AGND.
9. Tie the ground return of the input/output capacitors as close to PGND as possible with a large copper GND area.
10. Place vias around GND to lower the die temperature.

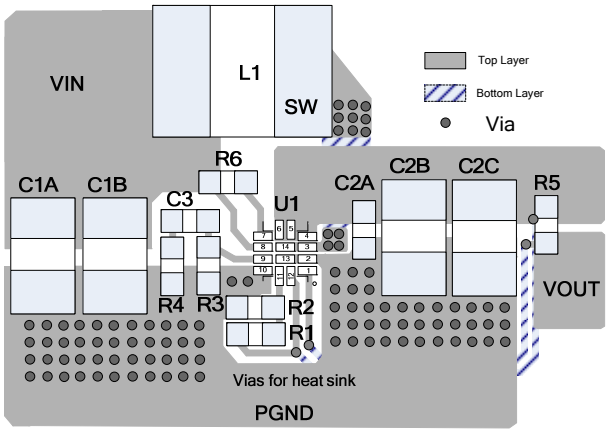


Figure 3: Recommended Layout

Design Example

Table 2 is a design example following the application guidelines for the following specifications.

Table 2: Design Example

V_{IN}	2.8V to 4.2V
V_{OUT}	5V
I_{OUT}	3.1A

TYPICAL APPLICATION CIRCUIT

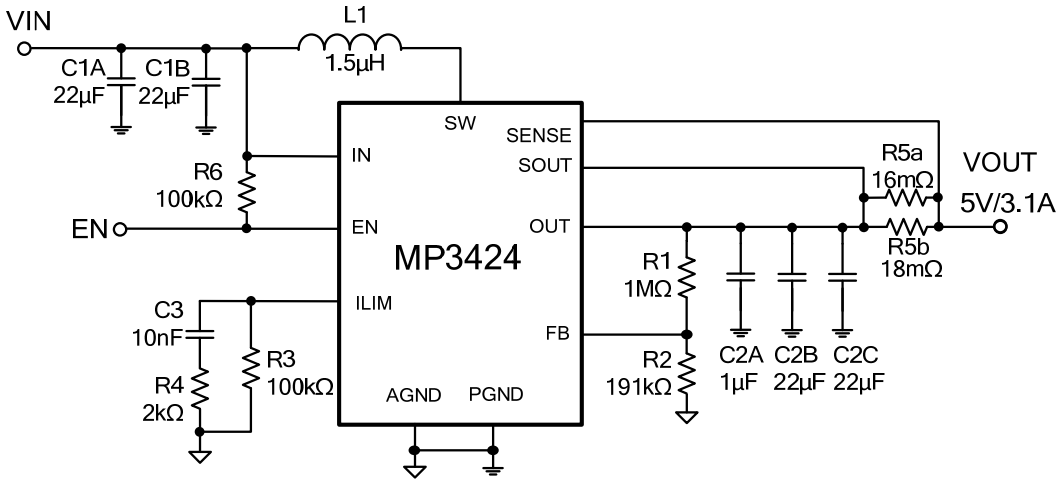


Figure 4: Typical Boost Application Circuit with Average Load Current Limit, V_{IN} = 2.8V to 4.2V, V_{OUT} = 5V

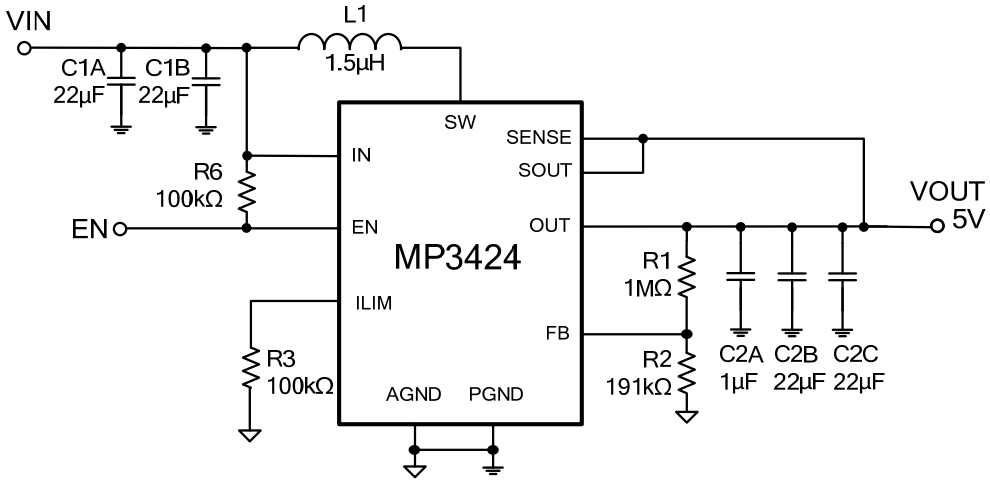
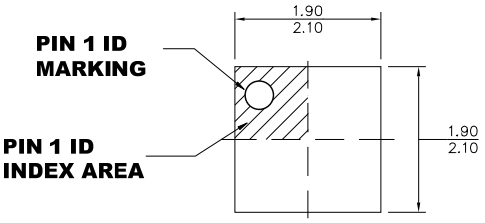


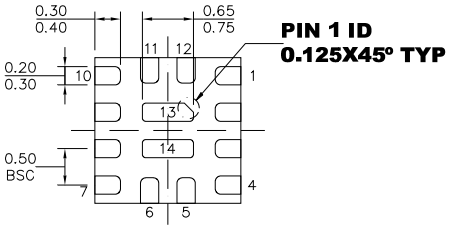
Figure 5: Typical Boost Application Circuit without Average Load Current Limit, V_{IN} = 2.8V to 4.2V, V_{OUT} = 5V

PACKAGE INFORMATION

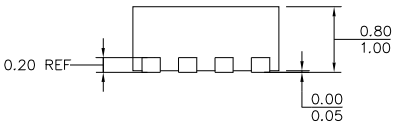
QFN-14 (2mmx2mm)



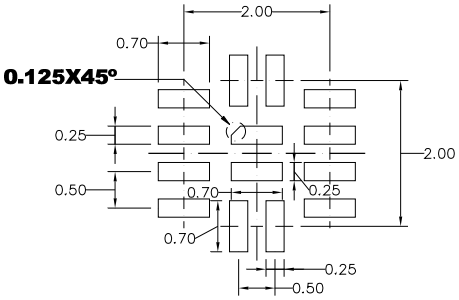
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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