MP6960

Fast Turn-Off Intelligent Controller With CC/CV Controller

The Future of Analog IC Technology

DESCRIPTION

The MP6960 is a synchronous rectified controller for a high-efficiency flyback converter circuit. The controller has integrated voltage and current regulators for the secondary side of the converter, making it suitable for battery charging and as a secondary controller for switching regulator systems.

The MP6960 regulates the forward drop of an external switch to about 70mV and switches it off as soon as the voltage goes negative. It also has a light-load sleep mode to reduce the quiescent current to <300μA.

The MP6960 also compares the DC voltage and the current level at the output of a switching power supply to the voltage reference and current limitation, respectively. It provides feedback through an opto-coupler to the PWM controller IC at the primary side.

The MP6960 is available in an SOIC8 package.

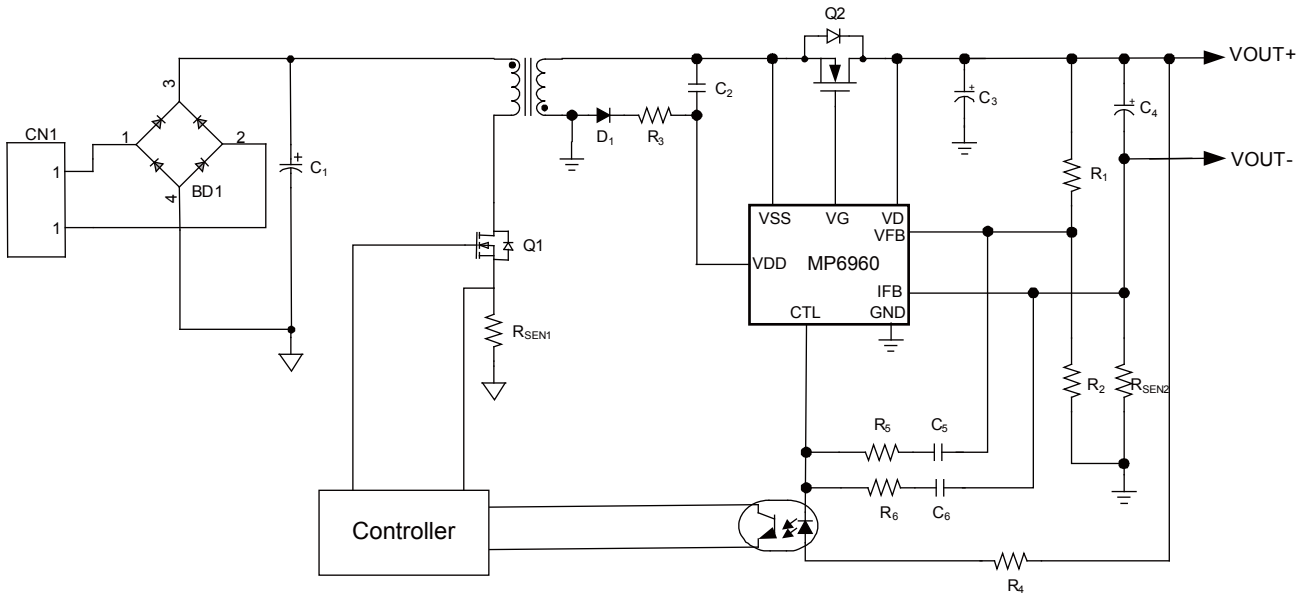
FEATURES

- Works with 12V Standard and 5V Logic-Level FETS
- Compatible with Energy Star 1W Standby Requirements
- V_{DD} to V_{SS} Range from 8V to 24V
- V_D to GND Range from 4.5V to 36V
- Fast Turn-Off Total Delay of 20ns
- Max. 400kHz Switching Frequency
- <400μA Quiescent Current in Light-Load Mode
- Supports CCM, DCM and Quasi-Resonant Topologies
- Supports High-Side and Low-Side Rectification
- Power Savings of up to 1.5W in a Typical Notebook Adapter
- 2.5V Built-In Voltage Reference with ±0.5% Accuracy
- 25mV Built-In Current Reference with ±5% Accuracy
- Constant Voltage and Constant Current Control
- Two Operational Amplifier with ORED Output and 1MHz Bandwidth
- 8-Pin SOIC8 Package

APPLICATIONS

- Industrial Power Systems
- Distributed Power Systems
- Battery Powered Systems
- Flyback Converters

TYPICAL APPLICATION

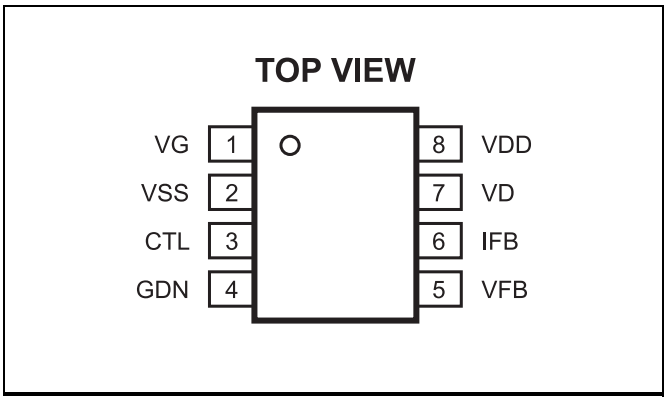


ORDERING INFORMATION

Part Number	Package	Top Marking
MP6960GS*	SOIC8	MP6960
MP6960CGS**	SOIC8	MP6960

* For Tape & Reel, add suffix –Z (e.g. MP6960GS–Z);
** For Tape & Reel, add suffix –Z (e.g. MP6960CGS–Z);

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{DD} to V_{SS} ..... -0.3V to +27V
GND to V_{SS} ..... -0.3V to +180V
V_G to V_{SS} ..... -0.3V to +27V
V_D to V_{SS} ..... -0.7V to +180V
V_D to GND ..... -0.7V to +40V
CTL to GND ..... -0.3V to +40V
VFB, IFB to GND ..... -0.3V to +6.5V
Maximum Operating Frequency ..... 400 kHz
Continuous Power Dissipation (T_A=+25°C) (2) 1.4W
Junction Temperature ..... 125°C
Lead Temperature (Solder) ..... 260°C
Storage Temperature ..... -55°C to +150°C

Recommended Operating Conditions (3)

V_{DD} to V_{SS} ..... 8V to 24V
V_D to GND ..... 4.5V to 36V
Maximum Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
SOIC8	90	45 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS (5)

V_{DD} = 12V, T_A= +25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SYNCHRONOUS RECTIFIER CONTROLLER						
V_{DD} Voltage Range		V_{DD}- V_{SS}	8		24	V
V_{DD} UVLO Rising			4.5	5.6	7	V
V_{DD} UVLO Hysteresis			0.8	1	1.2	V
Operating Current	I_{CC}	C_{LOAD}=5nF, f_{SW}=100kHz		8	10	mA
Quiescent Current	I_q	V_{SS}-V_D=0.5V		2	3	mA
Shutdown Current of Synchronous Rectifier Controller	I_{shut_SR}	V_{DD} =4V,V_D=GND		170	220	µA
Light-Load Mode Current				260	360	µA
Thermal Shutdown				150		°C
Thermal Shutdown Hysteresis				30		°C
Turn-On Threshold (V_{SS}-V_D)	V_{fwd}		55	70	85	mV
Turn-on Delay	t_{Don}	C_{LOAD} = 5nF		150		ns
	t_{Don}	C_{LOAD} = 10nF		250		ns
Input Bias Current on V_D Pin		V_D = 180V			1	µA
Minimum On-Time (5)	t_{MIN}	C_{LOAD} = 5nF		1.6		µs
Light-Load–Enter Delay	$t_{LL\text{-}Delay}$	(R_{LL}=100kΩ,integrated)		100		µs
Light-Load–Enter Pulse Width	t_{LL}		1.3	2	2.6	µs
Light-Load–Enter Pulse Width Hysteresis	$t_{LL\text{-}H}$			0.2		µs
Light-Load Mode Exit Pulse Width Threshold (V_{DS})	$V_{LL\text{-}DS}$		-400	-250	-150	mV
Light-Load Mode Enter Pulse Width Threshold (V_{GS}) (5)	$V_{LL\text{-}GS}$			1.0		V
GATE DRIVER SECTION						
V_G (Low)		I_{LOAD}=1mA		0.05	0.1	V
V_G (High)		V_{DD} >17V	13	14	15	V
		V_{DD} <17V	V_{DD}-2.2			
Turn-off Threshold (V_{SS}-V_D)			20	30	40	mV
Turn-off Propagation Delay		V_D=V_{SS}		15		ns
Turn-Off Total Delay	t_{Doff}	V_D =V_{SS}, C_{LOAD}=5nF, R_{GATE}=0Ω		35		ns
	t_{Doff}	V_D =V_{SS}, C_{LOAD}=10nF, R_{GATE}=0Ω		45		ns
Pull-Down Impedance				1	2	Ω
Pull-Down Current (5)		3V <V_G<10V		2		A
CC/CV CONTROLLER						
Supply Current of CC/CV Controller	I_D	V_D-GND = 15V, no load		90		µA
OPERATIONAL AMPLIFIER of CC/CV CONTROLLER						
Input Bias Current (5)	I_B	T_A = 25°C	-50	-10	0	nA
Output Sink Current	I_{CTL_SINK}	T_A = 25°C, V_{CTL}=0.5V		15		mA
		-20°C =T_A =+85°C	8			
Large Signal Voltage Gain (5)	A_{VO}	R_L =2kΩ		15		V/mV

ELECTRICAL CHARACTERISTICS (5) *(continued)*

V_{DD} = 12V, T_A= +25°C, unless otherwise noted.

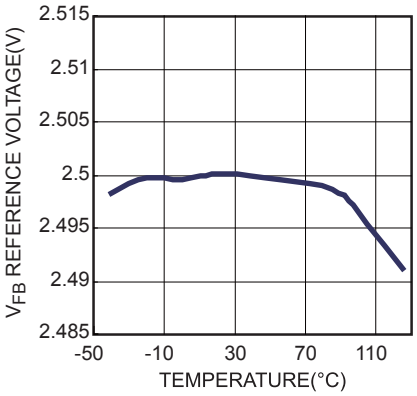
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage Rejection Ratio	SVR	Supply Voltage change of 1.0V	65	90		dB
Common Mode Rejection Ratio (5)	CMRR			80		dB
Gain Bandwidth Product (5)	GBW	V_D-GND=15V, $V_{FB}(I_{FB})$-$V_{REF}(I_{REF})$= 10mV, R_L =2kΩ, C_L =100pF		1		MHz
Output Leakage Current	$I_{CTL\_LEAKAGE}$	T_A = 25°C			2	μA
VOLTAGE REFERENCE (MP6960)						
Reference Voltage	V_{REF}	I_{OUT} = 1mA, T_A = 25°C	2.475	2.5	2.525	V
		0°C . T_A . 85°C(5)	2.47	2.5	2.53	V
VOLTAGE REFERENCE (MP6960C)						
Reference Voltage	V_{REF}	I_{OUT} = 1mA, T_A = 25°C	2.488	2.5	2.512	V
		0°C . T_A . 85°C(5)	2.48	2.5	2.52	V
CURRENT REFERENCE						
Reference Current	V_{IREF}	I_{OUT}=1mA, T_A=25°C	24	25	26	mV
		T_A=0°C to 85°C(5)	23.75	25	26.25	mV

Notes:

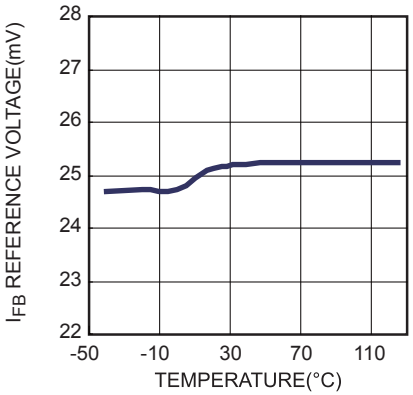
5) Guaranteed by Design and Characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{FB} Reference Voltage vs. Temperature

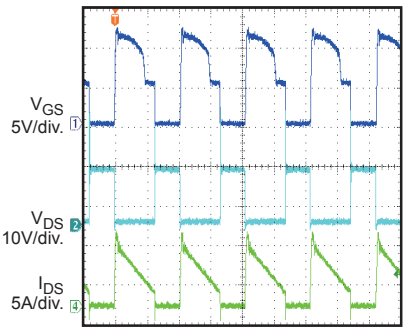


I_{FB} Reference Voltage vs. Temperature



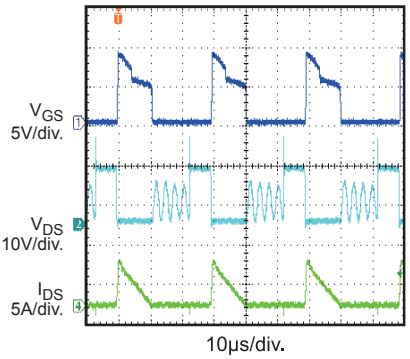
Synchronous Rectification in 15W Flyback

V_{IN}=85VAC, I_{OUT}=3A



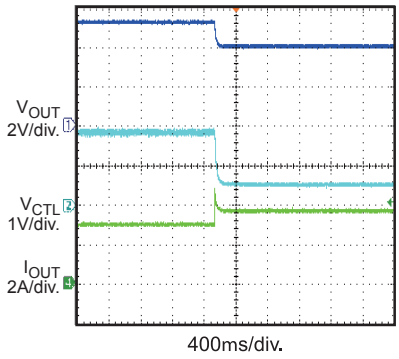
Synchronous Rectification in 15W Flyback

V_{IN}=85VAC, I_{OUT}=1A



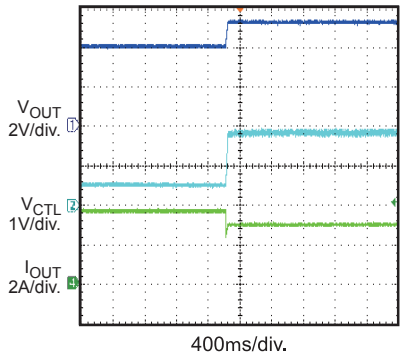
CV Mode to CC Mode

5V CV, 3.7A CC, V_{IN}=220VAC



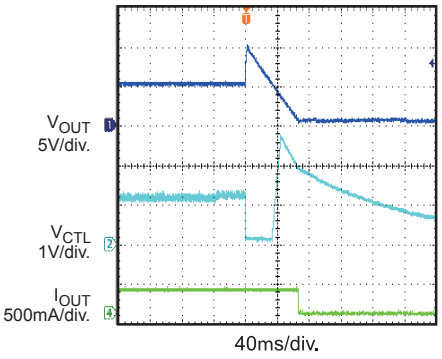
CC Mode to CV Mode

(5V CV, 3.7A CC, V_{IN}=220VAC



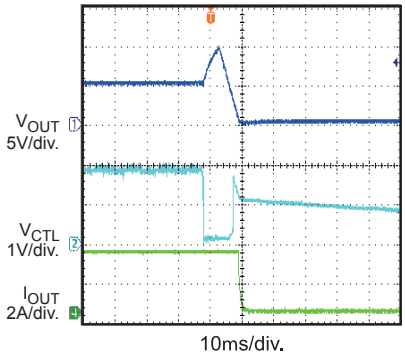
OVP Function in 15W Flyback

V_{IN}=220VAC, I_{OUT}=0.3A



OVP Function in 15W Flyback

V_{IN}=220VAC, I_{OUT}=3A



PIN FUNCTIONS

Pin #	Name	Description
1	VG	Gate Drive Output
2	VSS	Reference for VD. Connect to MOSFET source pin.
3	CTL	Output Common. Reference for voltage regulation and current limitation loops. Drives the primary side of an opto-coupler.
4	GND	CC/CV controller ground.
5	VFB	Voltage Feedback. An external resistor divider from the output to GND tapped to the FB pin sets the output voltage.
6	IFB	Current Feedback. Connected to the sense resistor.
7	VD	MOSFET Drain Voltage Sense. Also the supply voltage of the CC/CV controller
8	VDD	Supply Voltage of the Synchronous Rectifier Controller

BLOCK DIAGRAM

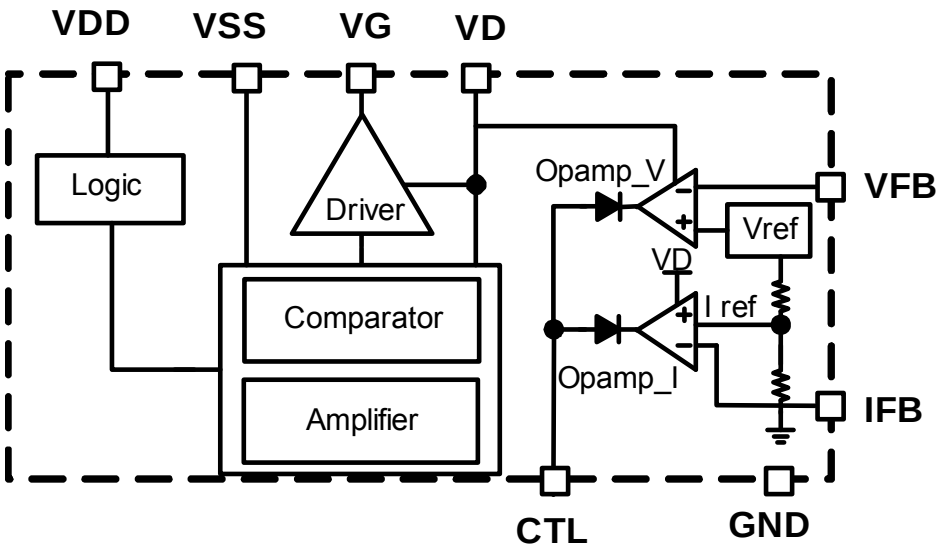


Figure 1: Functional Block Diagram

OPERATION

The MP6960 is a synchronous rectified controller for use in constant-current mode (CCM), discontinuous-current mode (DCM), and quasi-resonant topologies. MP6960 integrates a high-precision bandgap voltage reference, and two opamps to regulate and control the output voltage and current of the power supply.

Blanking

The control circuitry contains a blanking function that ensures that when the MOSFET turns on or off, it remains in that state for a minimal time period. The turn on blanking time is ~1.6μs, which determines the minimum on-time. During the turn-on blanking period, the turn-off threshold changes to approximately +50mV (instead of -30mV) to ensure that the part can always turn off even during the turn on blanking period (albeit slower, so do not set the synchronous period to less than 1.6μs in CCM for a flyback converter, or risk shoot through).

Under-Voltage Lockout (UVLO)

When the VDD drops below the UVLO threshold, the part enters sleep mode and the VG pin is pulled low by a 10kΩ resistor.

Turn-On Phase

When the synchronous MOSFET is ON, the current flowing through its body diode generates a negative V_{DS}. Because this body diode voltage drop (<-500mV) is much smaller than the turn-on threshold of the control circuitry (-70mV), then MP6960 will then pull the gate driver voltage high to turn on the synchronous MOSFET after a 150ns turn-on delay (Defined in Figure 2).

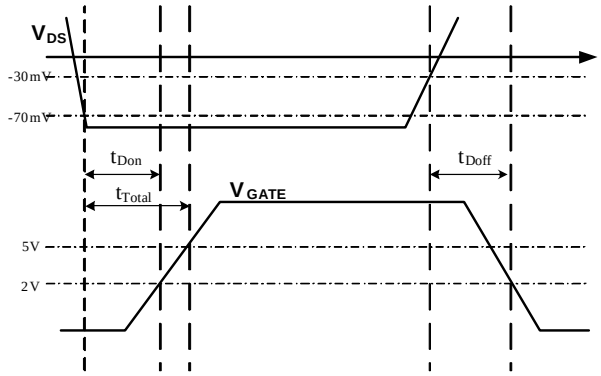


Figure 2: Turn-On and Turn-Off Delay

Conducting Phase

When the synchronous MOSFET turns ON, V_{DS} rises according to its ON resistance. As soon as V_{DS} rises above the turn-on threshold (-70mV), the control circuitry stops pulling up the gate driver, so the internal pull-down resistor (10kΩ) pulls down the gate voltage to increase the ON resistance of the synchronous MOSFET to slow the V_{DS} rise. This adjusts V_{DS} to around -70mV even when the current through the MOSFET is fairly small, and drop the driver voltage to fairly low levels when the synchronous MOSFET turns off to speed up turn-off (this driver-self-regulating function is still active during the turn-on blanking time so that the gate driver can turn off even with a very small duty).

Turn-Off Phase

When V_{DS} rises to trigger the turn-off threshold (-30mV), the control circuitry causes the gate voltage to go low after a 20ns turn-off delay (as shown in Figure 2) by the control circuitry. A 200ns blanking time—similar to the turn-on phase—after the synchronous MOSFET turns off avoids erroneous triggering.

Figure 3 shows synchronous rectification at heavy loads. The gate driver initially saturates due to the high current. After V_{DS} rises above -70mV, gate driver voltage decreases to adjust V_{DS} to -70mV.

Figure 4 shows synchronous rectification under light loads. Due to the low current, the gate driver voltage never saturates but decreases as soon as the synchronous MOSFET turns on and adjusts V_{DS}.

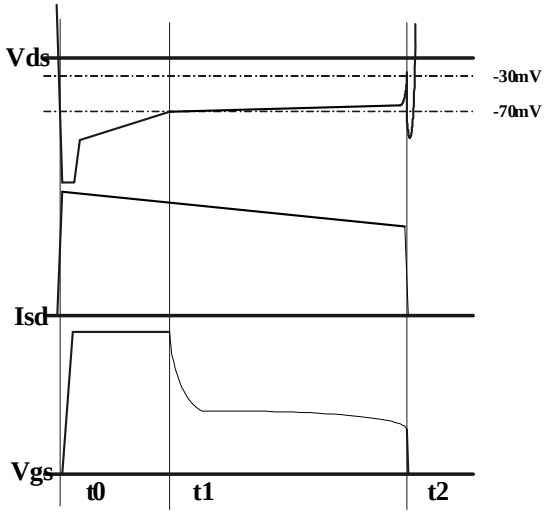


Figure 3: Synchronous Rectification Operation at Heavy-Load

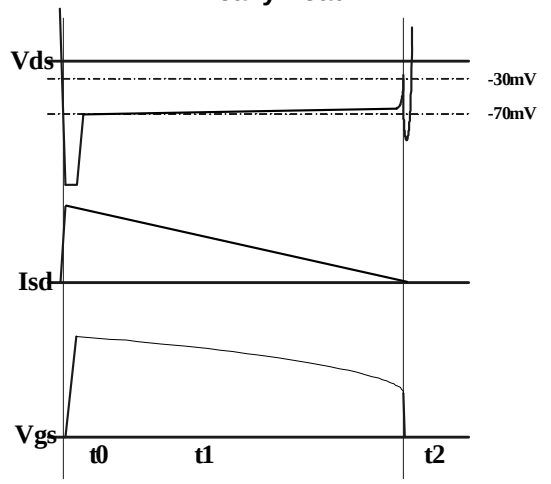


Figure 4: Synchronous Rectification Operation at Light-Load

Light-Load Latch-Off Function

The gate driver of the MP6960 latches to limit driver loss at light loads to improve efficiency. An internal resistor sets the light-load–enter pulse width, t_{LL}. When the synchronous MOSFET conducting period is less than t_{LL} for a longer than the light-load–enter delay ($t_{LL\text{-}Delay}$), the MP6960 enters light-load mode and latches off the gate driver. The synchronous MOSFET conducting period now starts when the gate driver turns on to when V_{GS} drops to the light-load–enter pulse width threshold ($V_{LL\text{-}GS}$).

During light-load mode, the MP6960 monitors the synchronous MOSFET body diode conducting period by sensing V_{DS}. When V_{DS} exceeds the light-load–exit pulse width threshold—$V_{LL\text{-}DS}$—the synchronous MOSFET body diode conducting period has ended. If the conducting period is longer than $t_{LL}+t_{LL\text{-}H}$ ($t_{LL\text{-}H}$, light-load-enter pulse width hysteresis), the light-load mode has ended and the gate driver is unlatched to restart the synchronous rectification.

SR MOSFET Selection and Driver Ability

Selecting a power MOSFET requires trading off between R_{ON} and Q_G. For higher efficiency, chose a MOSFET with a smaller R_{ON}, though is typically Q_G is usually larger and slows turn-on/off speed and increases power loss. Because V_{DS} is regulated at -70mV during the driving period, avoid MOSFET with very small R_{ON} because a low gate driver level when the MOSFET current is still fairly high counters any efficiency gains from using a MOSFET with a low R_{ON}.

Figure 5 shows the typical waveform of QR flyback. Assume a 50% duty cycle and the output current is I_{OUT}.

To make use of the MOSFET's low R_{ON}, the MOSFET be fully on for at least 50% of the SR conduction period:

$$V_{ds} = -I_c \times R_{on} = -2 \cdot I_{OUT} \times R_{on} \leq -V_{fwd}$$

Where V_{DS} is the MOSFET drain-source voltage and V_{fwd} is the forward voltage threshold of the MP6960, which is ~70mV.

Based on these requirements, select a MOSFET with an R_{ON} no less than $35/I_{OUT}$ (mΩ). For example, for a 5A application, select R_{ON} no less than 7mΩ. Figure 6 shows the corresponding total delay during the turn-on period with different Q_G values. Driving a 120nC Q_G MOSFET, the MP6960 can pull up the MOSFET gate driver voltage to 5V in 300ns as soon as the body diode can conduct, which reduces turn-on power loss.

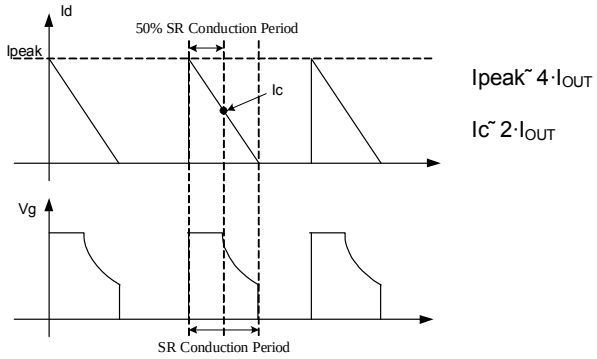


Figure 5: Synchronous Rectification of Typical Waveforms in QR Flyback

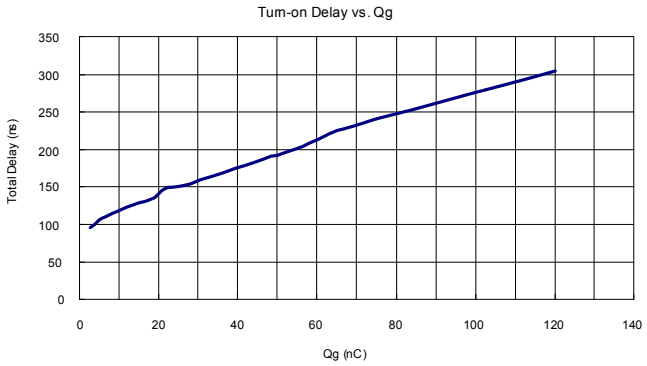


Figure 6: Total Turn-on Delay vs. QG

Voltage Regulation Loop

The voltage regulation is done by comparing the feedback output voltage (resistor divider R1 and R2) to the voltage reference (2.5V). If the feedback voltage exceeds 2.5V, the output of the voltage loop operational amplifier decreases. The opto-coupler current increases and reduces the output voltage by the way of the PWM controller.

Current-Limit Loop

Current limitation uses the voltage drop across the sense resistor, R_{SEN}, to measure the output current and compare it against the 25mV current reference. When the voltage across R_{SEN} exceeds 25mV, the output of the current loop operational amplifier decreases. The opto-coupler current increases and reduces the output voltage by the way of the PWM controller.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

Select the resistive voltage divider ratio to set the output voltage. The voltage divider drops the output voltage to 2.5V—the internal voltage reference. For most applications, use a 10kΩ low-side resistor for the voltage divider. Determine the high-side resistor using the equation:

$$R1 = R2 \times (\frac{V_{OUT}}{2.5V} - 1)$$

Where R1 is the high-side resistor, R2 is the low-side resistor and V_{OUT} is the output voltage.

Setting the Output Current

R_{SEN} is the sense resistor used for current measurement.

The current regulation is most effective when the voltage drop across R_{SEN} equals the voltage of the current reference, 25mV.

R_{SEN} can be realized with standard low cost 0.5W resistors in parallel.

$$I_{OUT} = \frac{V_{REF}}{R_{SEN}}$$

Where I_{OUT} is the output current, and V_{REF}=25mV.

In case the voltage drop across R_{SEN} always exceeds the voltage of the current reference (25mV),CTL will send a signal to the PWM controller to shutdown the PWM driver so that V_{IFB} remains around V_{IREF}. Figure 7 shows typical application in this case.

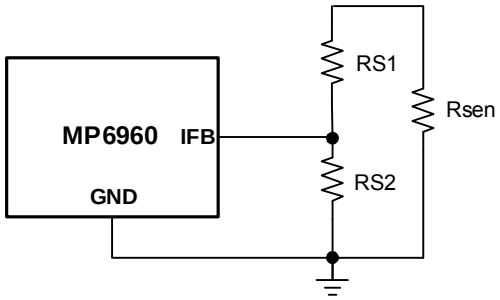


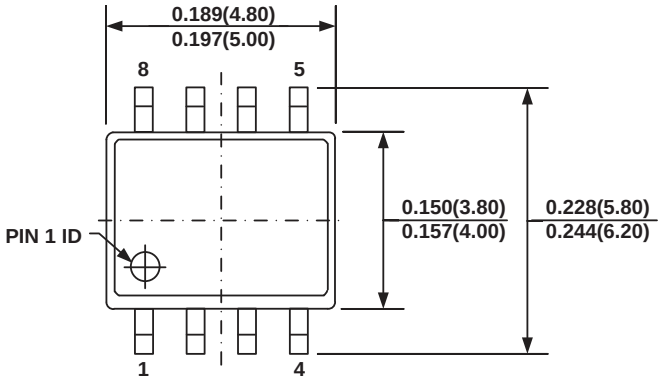
Figure 7: Typical IFB Application

$$I_{OUT} = \frac{V_{REF}}{R_{SEN}} \times \frac{Rs1 + Rs2}{Rs2}$$

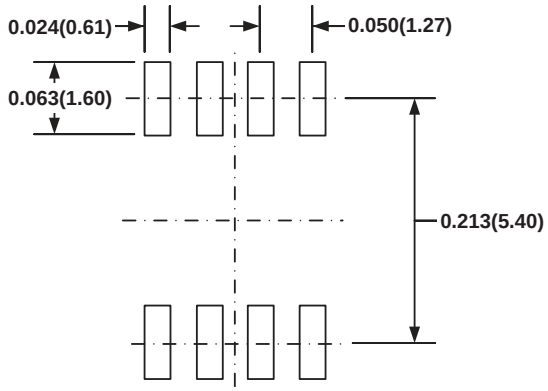
Where RS1 is the high-side resistor, RS2 is the low-side resistor and I_{OUT} is the output current, V_{REF}=25mV.

PACKAGE INFORMATION

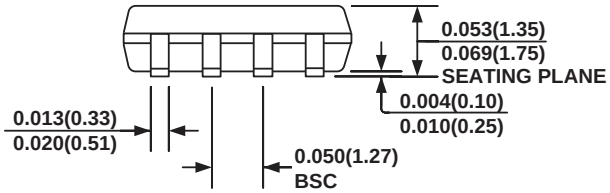
SOIC8



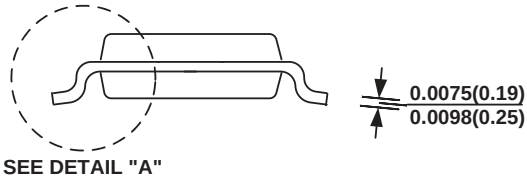
TOP VIEW



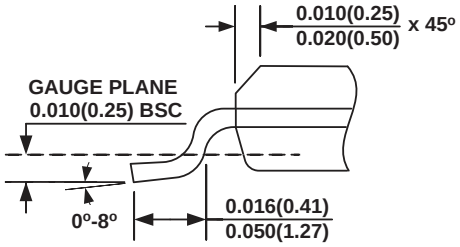
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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