MP4541

80V, 0.8A, High-Efficiency,
Synchronous**, Step-Down Converter**
with Integrated Power MOSFETS

DESCRIPTION

The MP4541 is a high-efficiency, synchronous step-down converter with integrated power MOSFETs. The device provides 0.8A of output current (I_{OUT}) in a buck topology from an input power supply of up to 80V.

The MP4541 features constant-on-time (COT) control, which provides fast transient response and facilitates loop stabilization. The configurable operation frequency can be set between 100kHz and 1MHz via an external resistor.

The device supports high-efficiency pulse-skip mode (PSM) while operating under light-load conditions. The valley current limit circuits protect against overload and short-circuit conditions.

The MP4541 is available in an SOIC-8EP package.

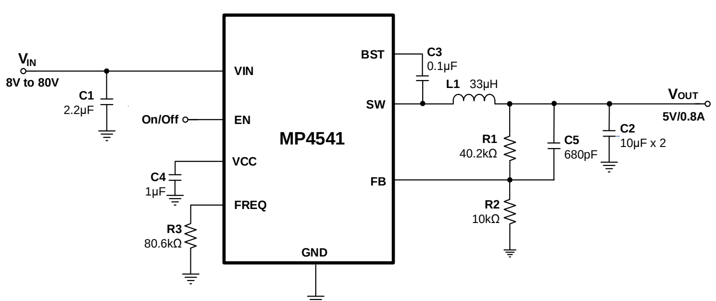
FEATURES

- 8V to 80V Input Voltage Range
- 1V to 30V Output Voltage Range
- 90% Maximum Operation Duty Cycle
- 625mΩ/265mΩ Internal Power MOSFETs
- Constant-On-Time (COT) Control
- 100kHz to 1MHz Configurable Frequency
- Internal Soft Start and Loop Compensation
- Over-Current Protection (OCP)
- Short-Circuit Protection (SCP) with Hiccup Mode
- High-Efficiency Pulse-Skip Mode (PSM) under Light-Load Conditions
- Available in an SOIC-8EP Package

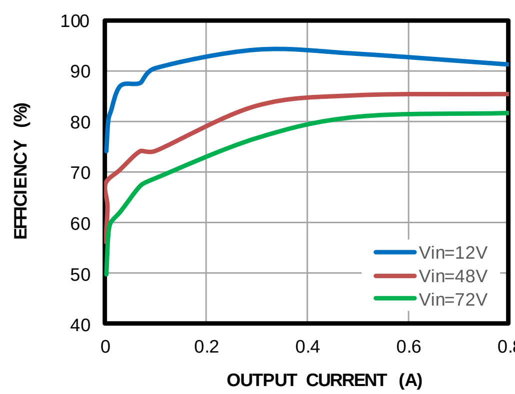
APPLICATIONS

- High-Voltage Battery Packs
- Industrial Power Supplies
- Printer Power Boards

TYPICAL APPLICATION



Efficiency
V_{OUT} = 5V



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP4541GN	SOIC-8EP	*See Below*	*2a*

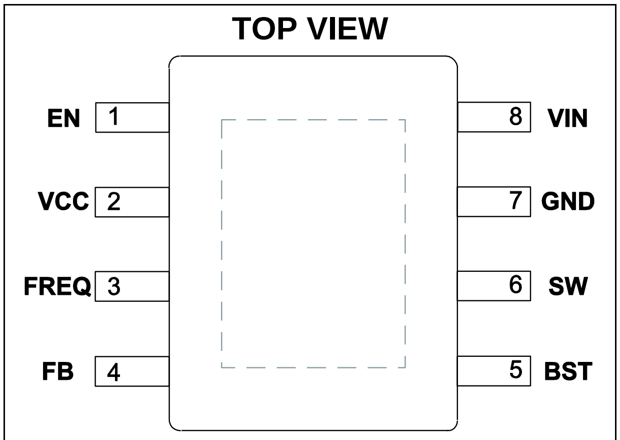
* For Tape & Reel, add suffix -Z (e.g. MP4541GN-Z).

TOP MARKING

MP4541
LLLLLLLL
MPSYWW

MP4541: Part number
MPS: MPS prefix
Y: Year code
WW: Week code
LLLLLLLL: Lot number

PACKAGE REFERENCE



SOIC-8EP

PIN FUNCTIONS

Pin #	Name	Description
1	EN	**Power enable.** Pull the EN pin high to turn on the MP4541. Pull EN low to turn off the MP4541. Do not float the EN pin.
2	VCC	**Internal LDO output.** VCC supplies power to the internal control circuit. Decouple VCC with a ≥1µF ceramic capacitor.
3	FREQ	**Switching frequency (f_{SW}) setting.** Connect an external resistor from the FREQ pin to the GND pin to set the buck f_{SW}.
4	FB	**Output voltage (V_{OUT}) feedback.** Connect a resistor divider from the output to the FB pin.
5	BST	**Bootstrap power for the high-side MOSFET (HS-FET) gate driver.** Connect a 0.1µF capacitor between the BST and SW pins.
6	SW	**Switch node of the converter.** Connect the SW pin to the source of the HS-FET and the drain of the low-side MOSFET (LS-FET).
7	GND	**Power ground.**
8	VIN	**Power supply input.**

ABSOLUTE MAXIMUM RATINGS (1)

VIN, EN .... -0.3V to +85V
SW .... -0.5V to +85V
SW (<20ns) .... -5V to +88V
BST to SW .... -0.3V to +6V
All other pins .... -0.3V to +6V
Continuous power dissipation (T_A = 25°C)
.... 3.2W (2) (4)
Junction temperature .... 150°C
Lead temperature .... 260°C
Storage temperature.............. -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .... 8V to 80V
Output voltage (V_{OUT})...................... 1V to 30V
Operating junction temp (T_J)... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

SOIC-8EP
EV4541-N-00A (4) .... 38......... 7.5.....°C/W
JESD51-7 (5) .... 48......... 10......°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the converter may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EV4541-N-00A, a 63.5mmx63.5mm, 1oz, 2-layer PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages, and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 48V, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
VCC under-voltage lockout (UVLO) threshold rising	VCC_{UVLO-R}	VCC rising	3.15	3.35	3.55	V
VCC UVLO threshold hysteresis	VCC_{HYS}			150		mV
VCC regulation voltage		I_{VCC} = 2mA	4.5	4.85	5.2	V
Shutdown current	I_{SD}	V_{EN} = 0V, measured on VIN			2	μA
Quiescent current	I_Q	V_{IN} = 12V, V_{FB} = 1.05V, no switching, measured on VIN, T_J = 25°C		15		μA
Enable (EN) Control						
Micro-power EN start-up threshold					0.9	V
Micro-power EN off threshold			0.4			V
EN input high threshold	V_{EN_ON}	V_{EN} rising	1.15	1.25	1.35	V
EN hysteresis	V_{EN_H}	V_{EN} rising/falling		120		mV
Minimum off time	t_{MIN_OFF}	V_{FB} = 0V		150		ns
Minimum on time (7)	t_{MIN_ON}			45		ns
Reference Voltage						
FB reference voltage	V_{REF}	8V to 100V, T_J = 25°C	0.99	1	1.01	V
		8V to 100V, T_J = -40°C to +125°C	0.985	1	1.015	V
FB input current	I_{FB}	V_{FB} = 1.05V			50	nA
Soft-start (SS) time	t_{SS}	10% to 90% of V_{REF}		4.35		ms
FB under-voltage threshold	V_{UVP}			60%		V_{REF}
Power Switch						
LS-FET on resistance	R_{ON_L}			265		mΩ
Synchronous HS-FET on resistance	R_{ON_H}			625		mΩ
Current Limit						
LS-FET valley current limit	I_{VL_LIMT}	Over full duty cycle, T_J = 25°C	0.72	0.8	0.88	A
		Over full duty cycle, T_J = -40°C to +125°C	0.68	0.8	0.92	A
Inductor current zero-current detection (ZCD) threshold			-60	0	+60	mA
Thermal Protection						
Thermal shutdown (7)	T_{SD}			150		°C
Thermal shutdown hysteresis (7)	T_{SD_HYS}			25		°C

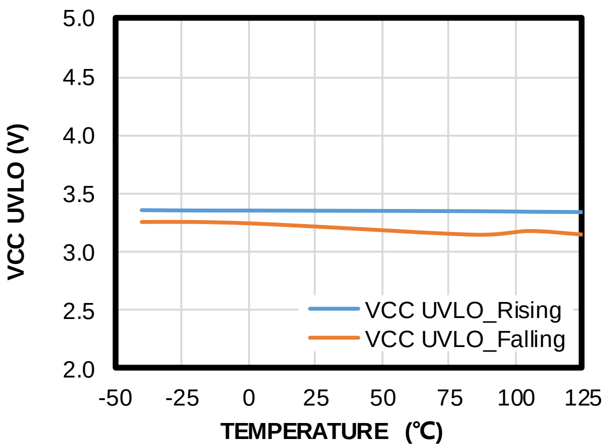
Notes:

6) Not tested in production. Guaranteed by over-temperature correlation.
7) Guaranteed by engineering sample characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

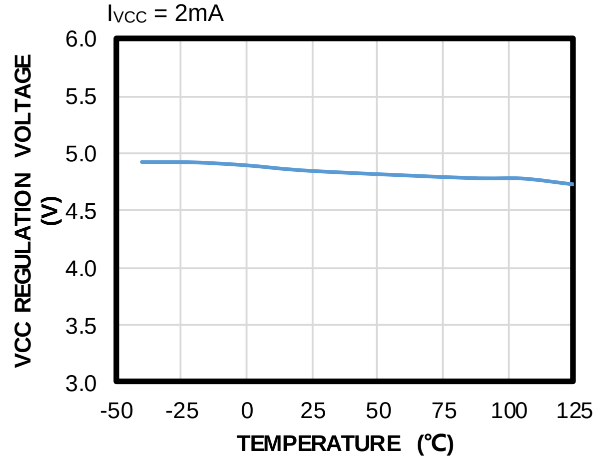
V_{IN} = 48V, T_J = -40°C to +125°C, unless otherwise noted.

VCC UVLO vs. Temperature

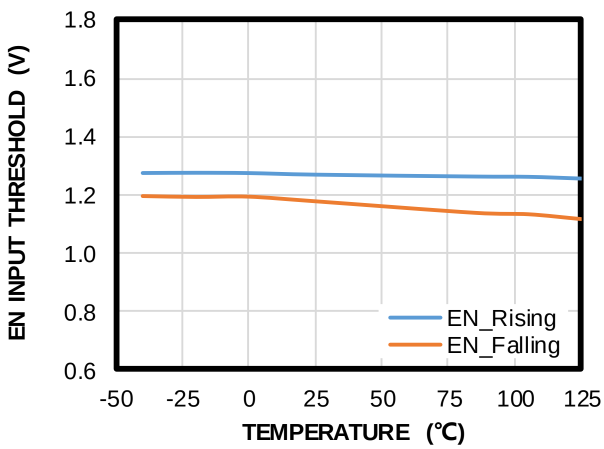


VCC Regulation Voltage vs. Temperature

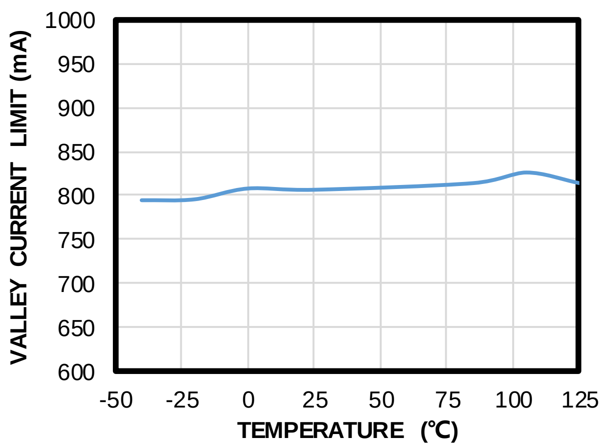
I_{VCC} = 2mA



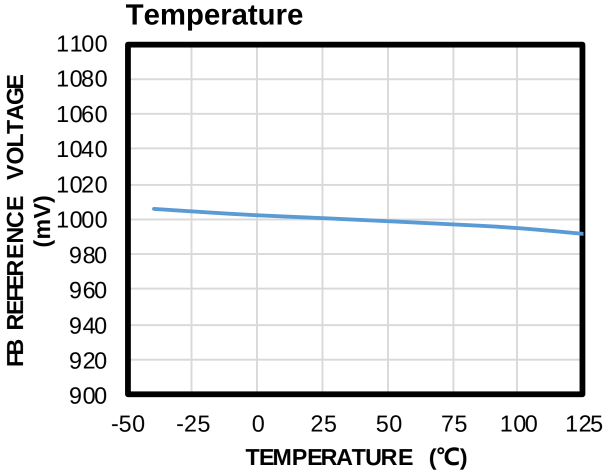
EN Input Threshold vs. Temperature



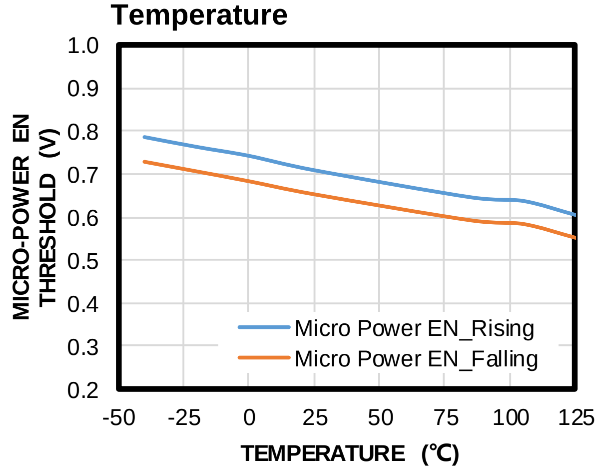
Valley Current Limit vs. Temperature



FB Reference Voltage vs. Temperature



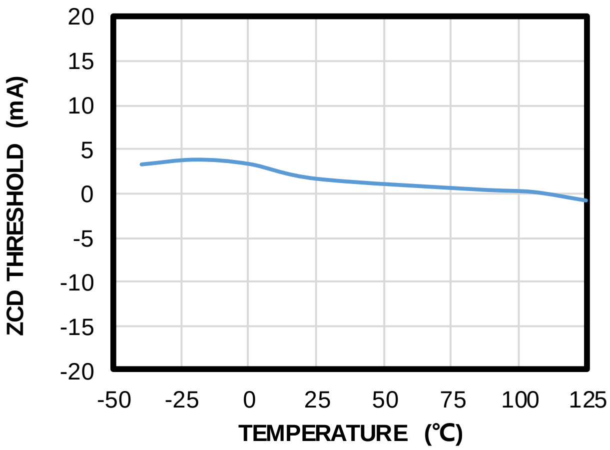
Micro-Power EN Threshold vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

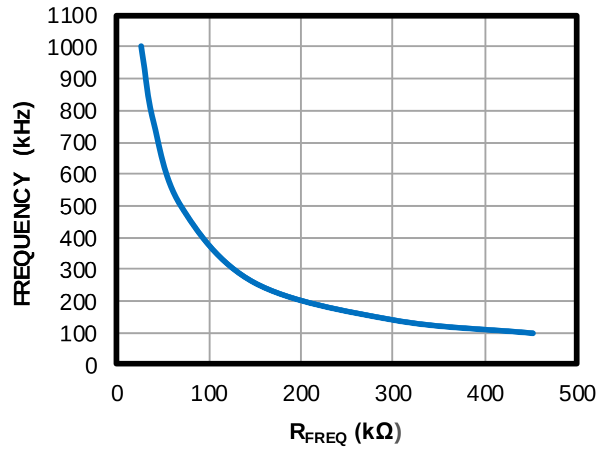
V_{IN} = 48V, T_J = -40°C to +125°C, unless otherwise noted.

Inductor Current ZCD Threshold vs. Temperature



Frequency vs. R_{FREQ}

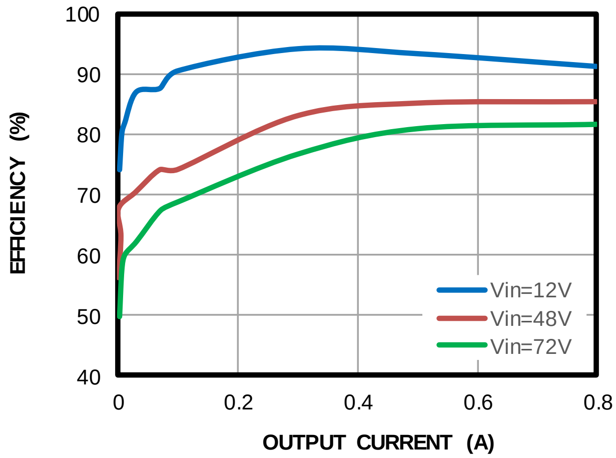
T_A = 25°C



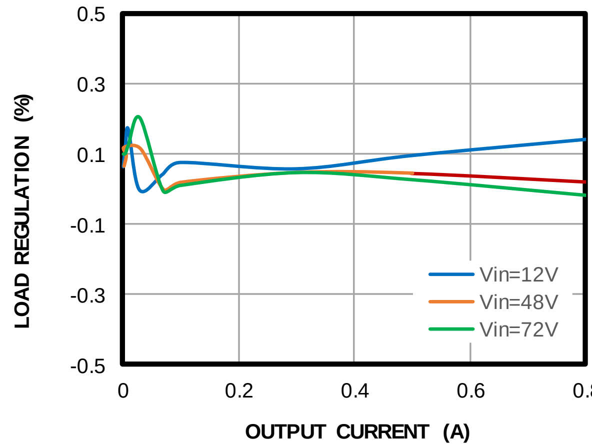
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{OUT} = 5V, L = 33µH, T_A = 25°C, unless otherwise noted.

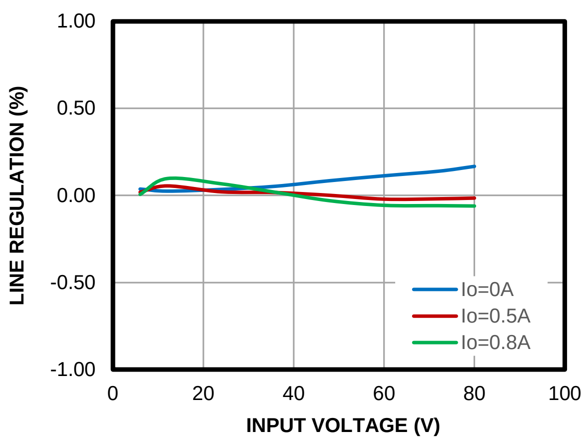
Efficiency



Load Regulation

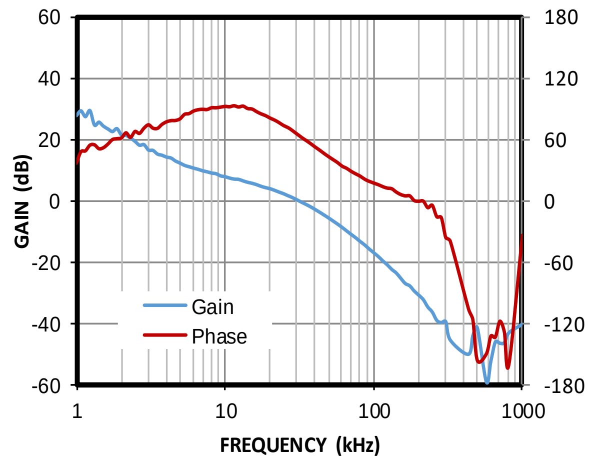


Line Regulation

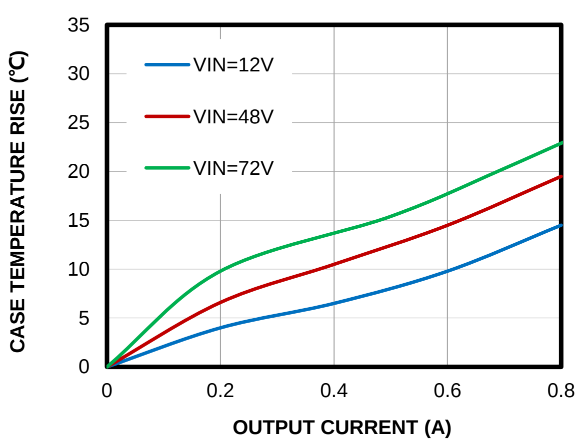


Bode Plot

I_{OUT} = 0.8A



Case Temperature Rise vs. Output Current

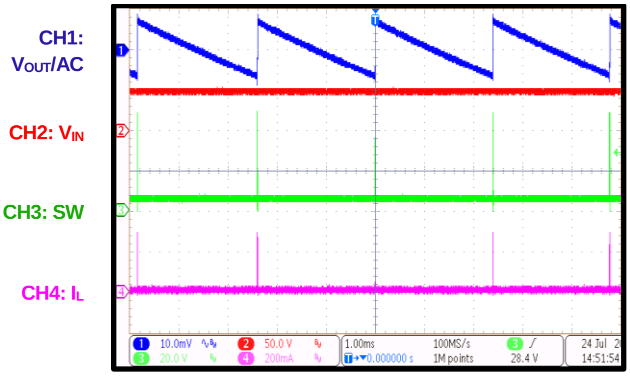


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{OUT} = 5V, L = 33µH, T_A = 25°C, unless otherwise noted.

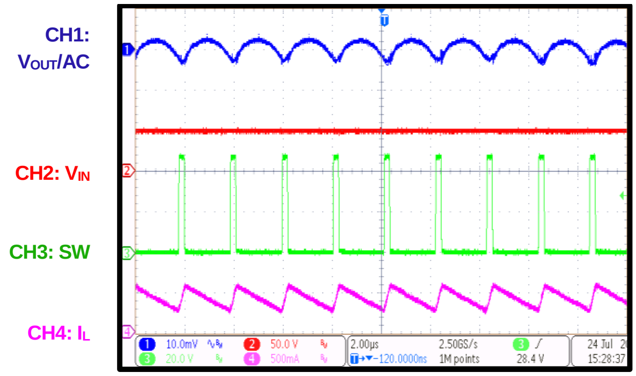
Steady State

I_{OUT} = 0A



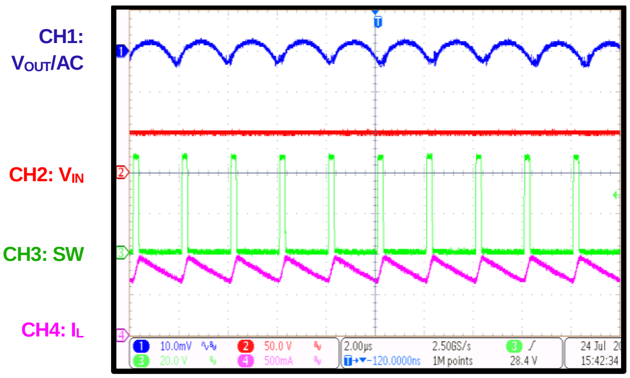
Steady State

I_{OUT} = 0.4A



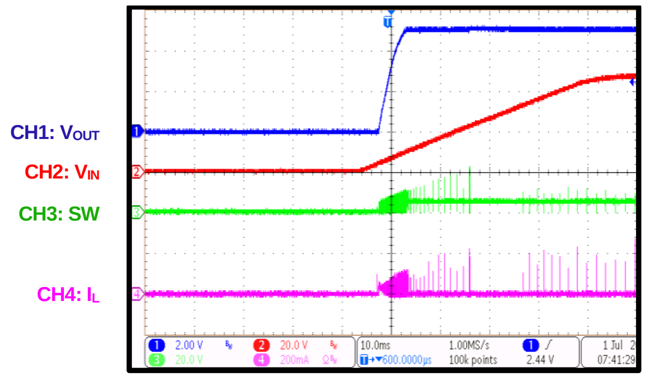
Steady State

I_{OUT} = 0.8A



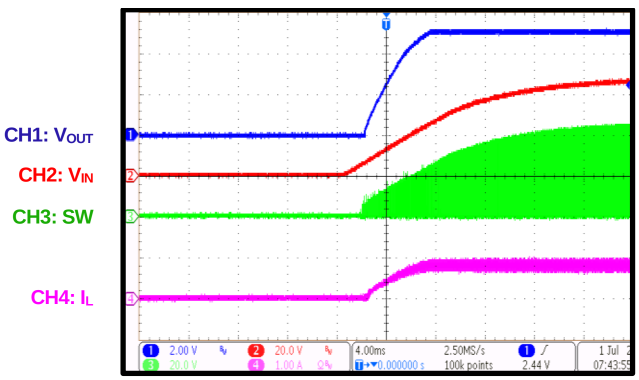
Start-Up through VIN

I_{OUT} = 0A



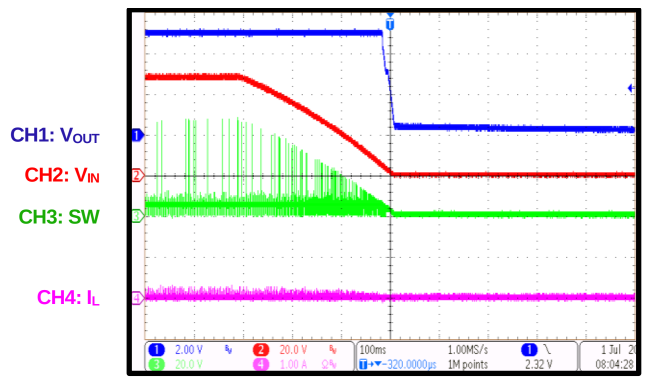
Start-Up through VIN

I_{OUT} = 0.8A



Shutdown through VIN

I_{OUT} = 0A

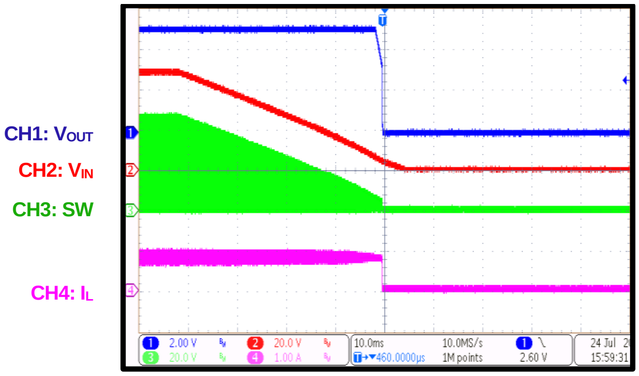


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{OUT} = 5V, L = 33µH, T_A = 25°C, unless otherwise noted.

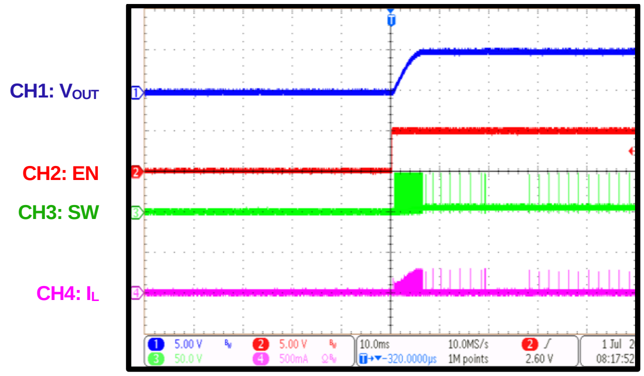
Shutdown through VIN

I_{OUT} = 0.8A



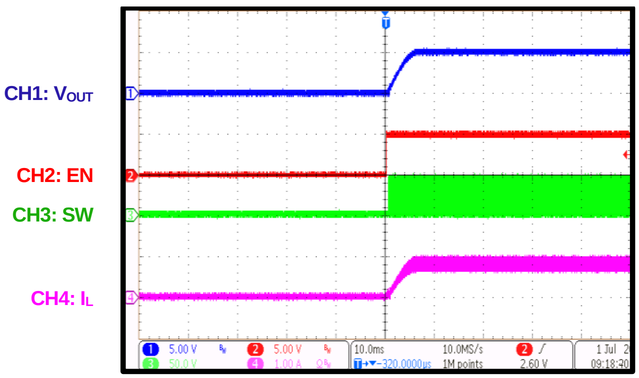
EN On

I_{OUT} = 0A



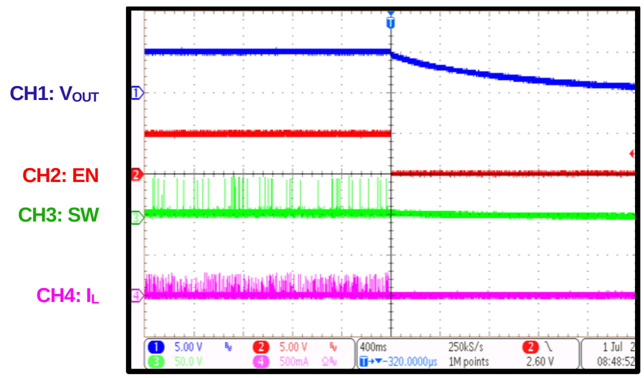
EN On

I_{OUT} = 0.8A



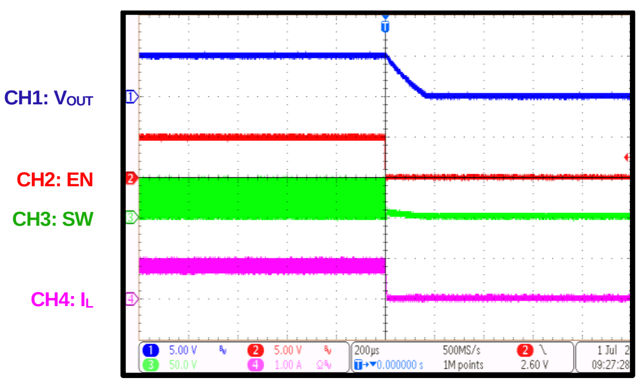
EN Off

I_{OUT} = 0A



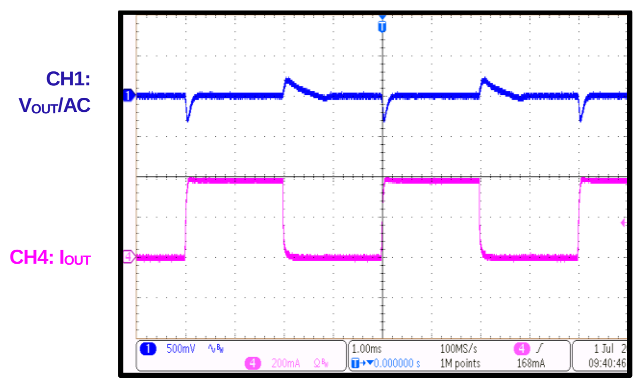
EN Off

I_{OUT} = 0.8A



Load Transient

I_{OUT} = 0A to 0.4A

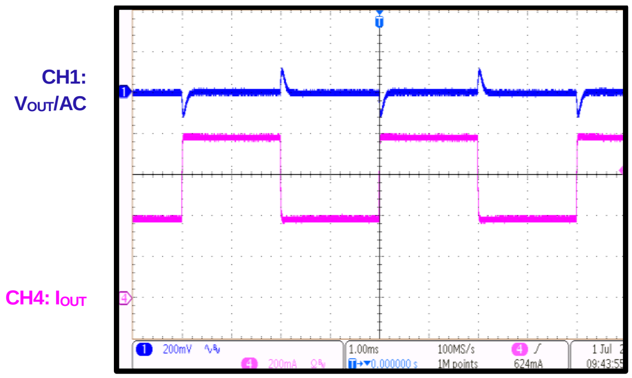


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

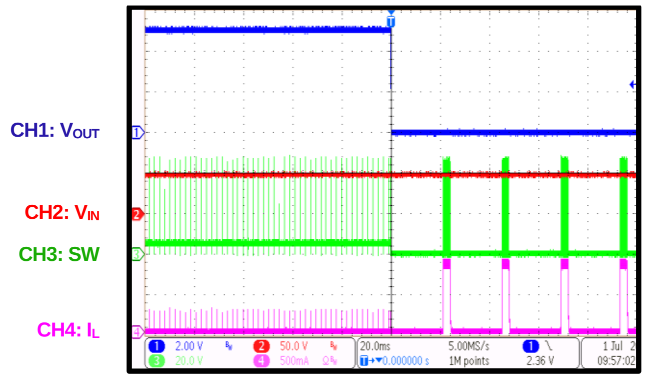
V_{IN} = 48V, V_{OUT} = 5V, L = 33µH, T_A = 25°C, unless otherwise noted.

Load Transient

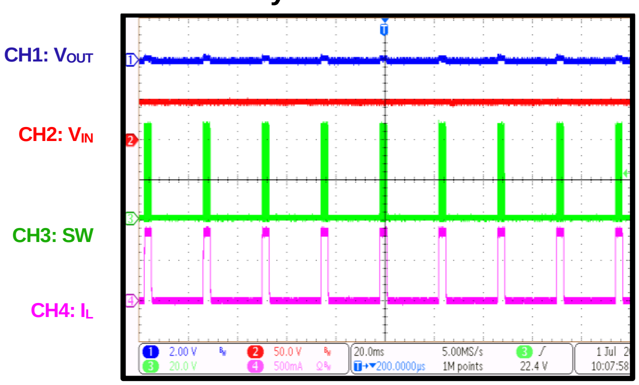
I_{OUT} = 0.4A to 0.8A



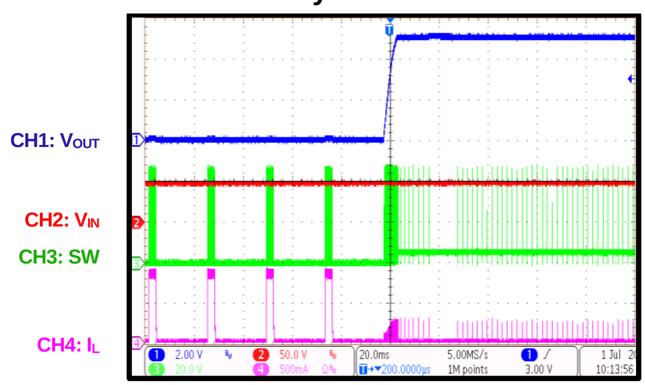
SCP Entry



SCP Steady State



SCP Recovery



FUNCTIONAL BLOCK DIAGRAM

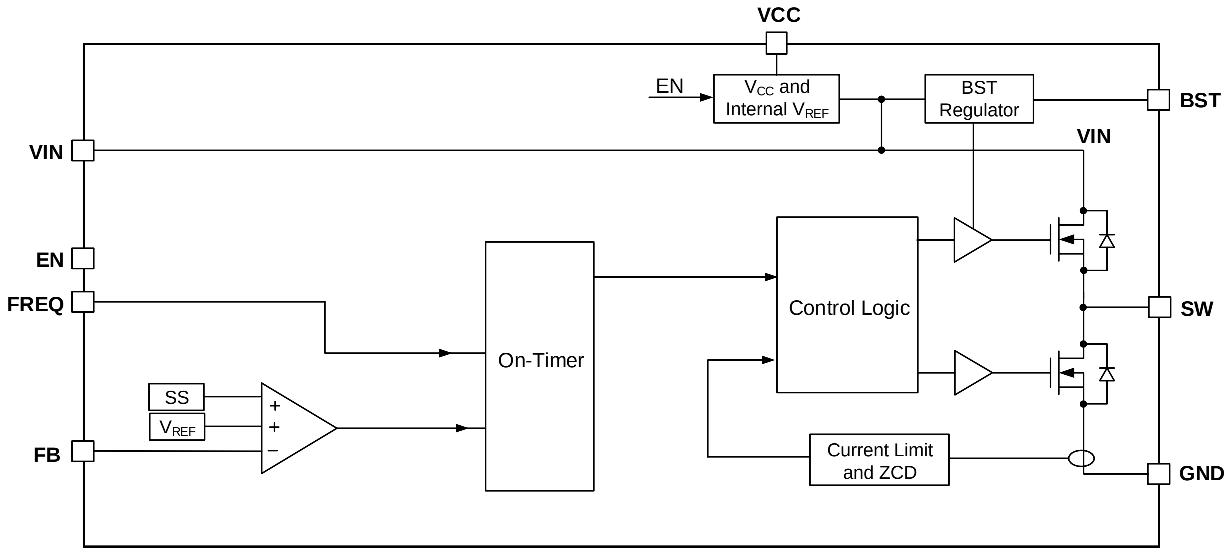


Figure 1: Functional Block Diagram

OPERATION

The MP4541 is a synchronous step-down switching converter with integrated power MOSFETs. It provides high efficiency and constant-on-time (COT) control for fast loop response and easy loop stabilization. The MP4541 features a wide 8V to 80V input voltage range, internal soft-start (SS) control, and precise current limiting. Its ultra-low quiescent current (I_Q) enables high efficiency under light-load conditions.

Constant-On-Time (COT) Control

The MP4541 includes constant-on-time (COT) control mode. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on for a fixed amount of time when the FB pin's voltage (V_{FB}) drops below the reference voltage (V_{REF}). This fixed on time is determined by a one-shot on-timer. The on time is determined by both the output voltage (V_{OUT}) and input voltage (V_{IN}) to maintain a constant switching frequency (f_{SW}) across the entire input voltage range.

Once the on period is complete, the HS-FET turns off until the next period. By repeating this operation, the converter can regulate V_{OUT}.

The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is off to minimize conduction loss. A dead short occurs between the VIN pin and GND pin if the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time is generated internally between the HS-FET and LS-FET on and off periods. The dead time occurs between the HS-FET off time and the LS-FET on time, or vice versa.

Heavy-Load Operation

The MP4541 operates in continuous conduction mode (CCM) when the output current (I_{OUT}) is high and the inductor current is above 0A. In CCM, the HS-FET turns on, then turns off once the on period is complete. Once the HS-FET turns off, the LS-FET turns on to conduct the inductor current.

Pulse-width modulation (PWM) operation occurs when f_{SW} remains constant while the part is in CCM.

Light-Load Operation

The MP4541 can work in pulse-skip mode (PSM) under light-load conditions. In PSM, the LS-FET goes into tri-state (Hi-Z) when the inductor current drops close to 0A, and the output capacitors discharge slowly to GND through the FB pin's feedback resistor. If V_{OUT} drops and the internal EA output voltage rises, the MP4541 starts the next switching cycle by turning on the HS-FET. The MP4541 automatically reduces f_{SW} and I_Q when the device is not switching. This improves the device's efficiency when I_{OUT} is low.

When the MP4541 is in PSM under light-load conditions, the HS-FET does not turn on as frequently as it does under heavy-load conditions. The frequency at which the HS-FET turns on is a function of I_{OUT}. As I_{OUT} increases, the HS-FET turns on more frequently. In turn, f_{SW} also increases. I_{OUT} exceeds the upper boundary threshold when the valley inductor current reaches 0A. I_{OUT} can be calculated with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \qquad (1)$$

Where f_{SW} is the switching frequency.

The MP4541 returns to CCM once I_{OUT} exceeds the upper boundary threshold. After this point, f_{SW} remains constant across the entire I_{OUT} range.

Switching Frequency (f_{SW})

Selecting a switching frequency (f_{SW}) is a tradeoff between efficiency and component size. Low-frequency operation increases efficiency by reducing MOSFET switching loss, but requires a larger inductance and capacitance to maintain the low output voltage ripple.

The MP4541 offers configurable COT control. When the FREQ pin is connected to the GND pin via a resistor (R_{FREQ}), V_{IN} is internally fed-forward to the one-shot on-timer. When the MP4541 is in steady state operation in CCM, the duty ratio is set to V_{OUT} / V_{IN}. Therefore, f_{SW} remains constant across the entire input voltage range. f_{SW} can be estimated with Equation (2):

$$f_{SW} = \left[\frac{10^6}{34.5 \times R_{FREQ}(k\Omega)} + 57\right](kHz) \qquad (2)$$

The switching frequency is typically set between 100kHz and 1MHz.

Power Supply

The MP4541's control circuit is powered by VCC, which is regulated by V_{IN}.

There is a V_{CC} under-voltage lockout (UVLO) circuit that protects the MP4541 from operating at an insufficient V_{IN}. The MP4541's UVLO comparator monitors V_{CC} and starts operating when V_{CC} exceeds the V_{CC} UVLO rising threshold.

Start-Up

When the EN pin is high and V_{CC} exceeds its UVLO threshold, the MP4541 starts up via an internal soft-start (SS) signal. Once the MP4541 starts switching, the SS signal ramps up from 0V and is compared to V_{REF}. The lower voltage is used by the error amplifier (EA) to control V_{OUT}. After the SS signal exceeds V_{REF}, soft start completes, and the internal reference block regulates the feedback loop.

The MP4541 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the voltage on the SS capacitor is charged. If the SS capacitor voltage exceeds the sensed output voltage at FB, the device starts normal operation.

Enable (EN) and Configurable Under-Voltage Lockout (UVLO)

The EN pin turns the MP4541 on and off. If voltage above 0.9V is applied, the MP4541 starts the internal bandgap (BG) circuit. Once the EN voltage (V_{EN}) exceeds EN's high threshold (typically 1.25V), the MP4541 turns on all functions and starts switching operation. Switching operation stops once V_{EN} drops below the low threshold (typically 1.13V). EN is compatible with voltages up to 80V.

There is no internal resistor on EN. For automatic start-up, connect EN to VIN through a resistor.

Overload Protection (OLP) and Short-Circuit Protection (SCP)

The MP4541 features valley current limit control. The inductor current is monitored during the LS-FET's on state. When the inductor current exceeds the valley current limit threshold, the LS-FET current limit comparator output switches. The HS-FET remains off until the inductor current drops below the valley current limit. Then the HS-FET turns on again. Meanwhile, the FB output voltage (V_{FB}) may drop below its UVLO threshold (typically 60% of V_{REF}). Once UVLO is triggered, the MP4541 enters hiccup mode and periodically restarts the part. Hiccup mode is disabled during soft start.

If over-current protection (OCP) triggers hiccup mode, the MP4541 turns off the output power stage and discharges the SS capacitor. Then the IC automatically initiates another soft start. If the over-current (OC) condition remains after soft start ends, the device repeats this hiccup operation until the OC condition is removed. Once the OC condition has been removed, V_{OUT} returns to the regulation level.

Bootstrap (BST) Power Supply

An external bootstrap (BST) capacitor powers the floating MOSFET driver. The external BST capacitor is charged by VCC. The V_{BST} - V_{SW} voltage supplies power to the HS-FET driver.

The MP4541 turns on once both VCC and EN exceed their respective thresholds. The reference block turns on first, and generates a stable V_{REF} and reference currents. Then the internal regulator turns on. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN being pulled low, VCC being pulled low, and thermal shutdown. The shutdown procedure starts by blocking the signaling path to avoid any fault triggering. Then the COMP voltage (V_{COMP}) and the internal supply rail are pulled low. The BST floating driver is not subject to this shutdown command.

Thermal Shutdown Protection

The MP4541 has one circuit to monitor the temperature. If the junction temperature exceeds 150°C, the MP4541 shuts down. Once the temperature drops below 125°C, the device resumes normal operation.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider sets the output voltage (V_{OUT}). First, choose a value for the resistor (R2). If R2 is too low, there can be considerable I_Q loss, while a higher-value R2 can make FB noise sensitive. It is recommended to choose an R2 value between 10kΩ and 100kΩ. R1 can be calculated with Equation (3):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (3)$$

Where V_{REF} is the reference voltage (typically 1V).

Figure 2 shows the typical feedback circuit.

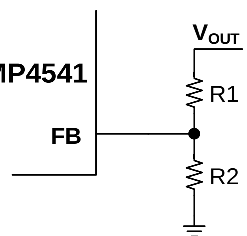


Figure 2: Feedback Network

Selecting the Inductor

A larger-value inductor provides less ripple current, which results in a lower output voltage ripple. However, a larger-value inductor has a larger physical footprint, higher series resistance, and lower saturation current. The recommended inductance value is to design the peak-to peak ripple current in the inductor to be in the range of 0.3A to 0.4A. The inductance can be calculated with Equation (4):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum peak inductor current (I_{LP}). I_{LP} can be calculated with Equation (5):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while also maintaining the DC input voltage. For the best results, it is recommended to use ceramic capacitors placed as close to VIN as possible. Ceramic capacitors with X5R and X7R dielectrics are recommended due to their stability amid temperature fluctuations.

The capacitors must have a ripple current rating that exceeds the converter's maximum input ripple current (I_{CIN}). I_{CIN} can be estimated with Equation (6):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (6)$$

The worst-case scenario occurs at $V_{IN} = 2 \times V_{OUT}$, calculated with Equation (7):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half the maximum load current.

The input capacitance determines the converter's input voltage ripple. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the relevant specifications.

The input voltage ripple can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

The worst-case scenario occurs at $V_{IN} = 2 \times V_{OUT}$, calculated with Equation (9):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (9)$$

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. It is recommended to use ceramic or POSCAP capacitors.

The output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (10)$$

With ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f^2_{SW} \times C_{OUT} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

With POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (12)$$

Selecting a larger-value output capacitor provides faster load transient response. However, the maximum output capacitor limit should be considered when designing for application. If the output capacitor value is too high, the output voltage cannot reach the required value during the SS time, and the capacitor may fail to regulate. The maximum output capacitor value (C_{O_MAX}) can be estimated with Equation (13):

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (13)$$

Where I_{LIM_AVG} is the average start-up current during soft start, and t_{SS} is the SS time.

Design Example

Table 1 shows a design example following the application guidelines for the provided specifications.

Table 1: Design Example

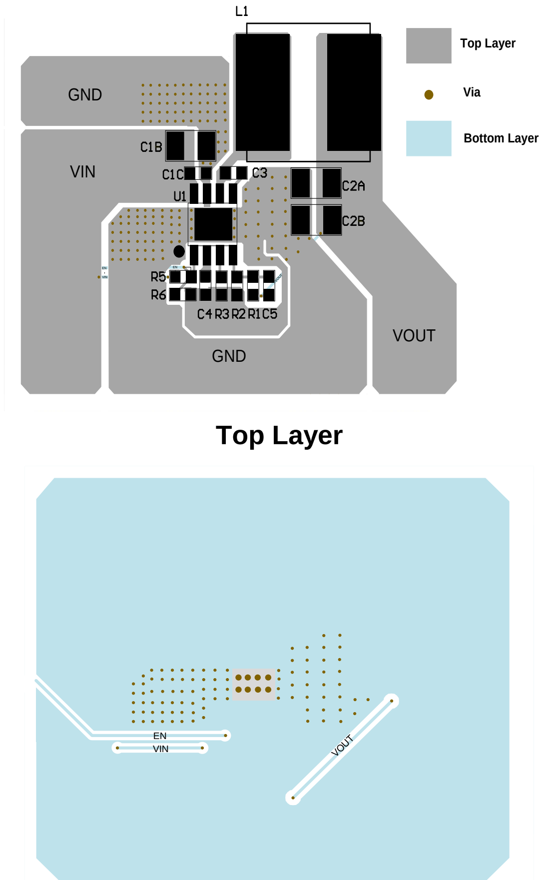
V_{IN}	8V to 80V
V_{OUT}	5V/0.8A
f_{SW}	420kHz

Figure 4 on page 17 shows the detailed application schematics. For the typical performance and circuit waveforms, see the Typical Performance Characteristics section. For more device applications, refer to the related evaluation board datasheet.

PCB Layout Guidelines

Efficient layout is critical for stable operation. For the best results, refer to Figure 3 and follow the guidelines below:

1. Place the high-current paths (GND, VIN, and SW) as close to the device as possible using short, direct, and wide traces.
2. Place the input capacitor as close to the VIN and GND pins as possible.
3. Place the external feedback resistors next to the FB pin.
4. Keep the switching node (SW) short, and route it as far away from the feedback network as possible.



Top Layer

Bottom Layer

Figure 3: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

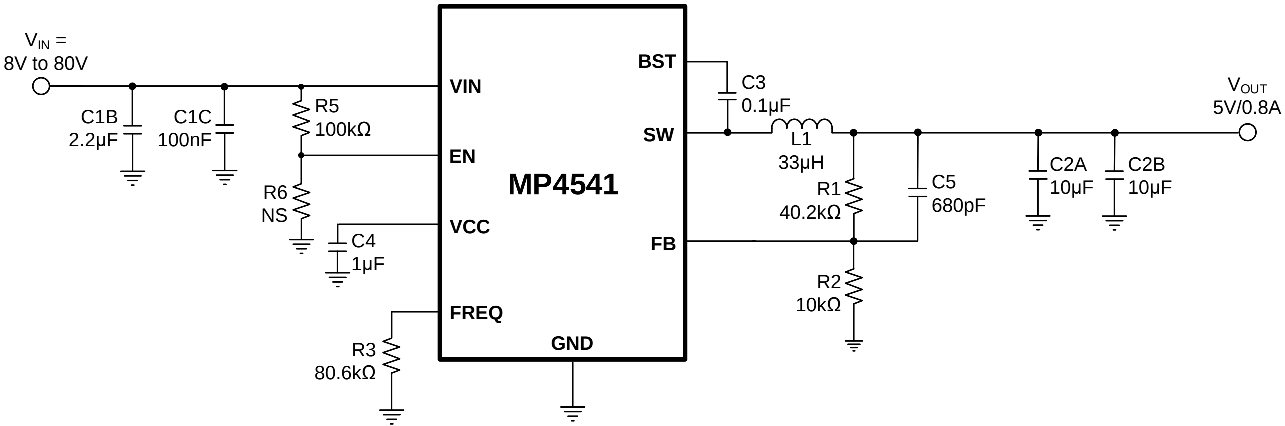
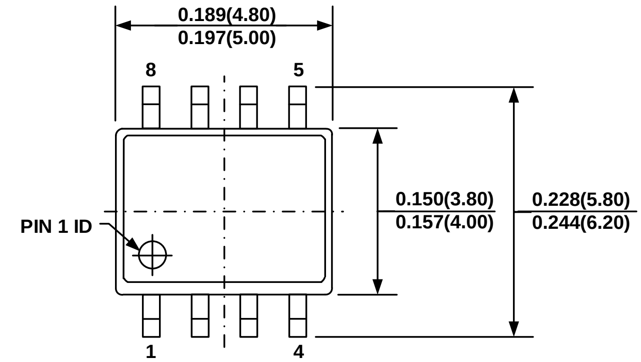


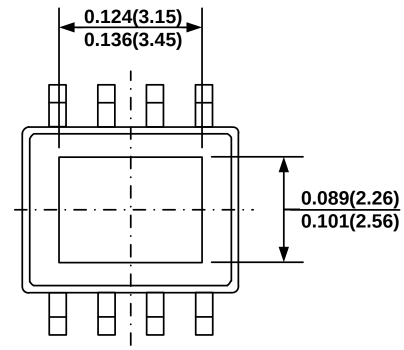
Figure 4: Typical Application Circuit

PACKAGE INFORMATION

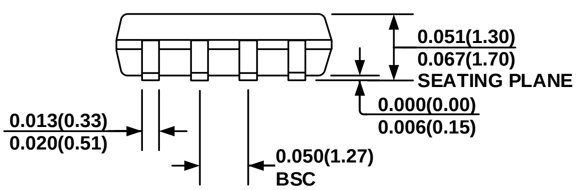
SOIC-8EP



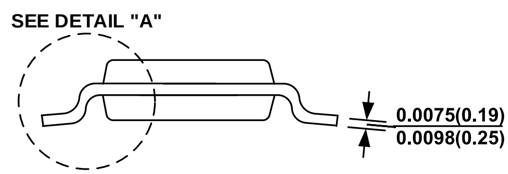
TOP VIEW



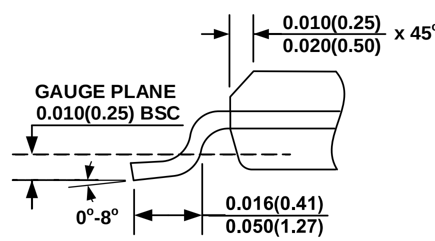
BOTTOM VIEW



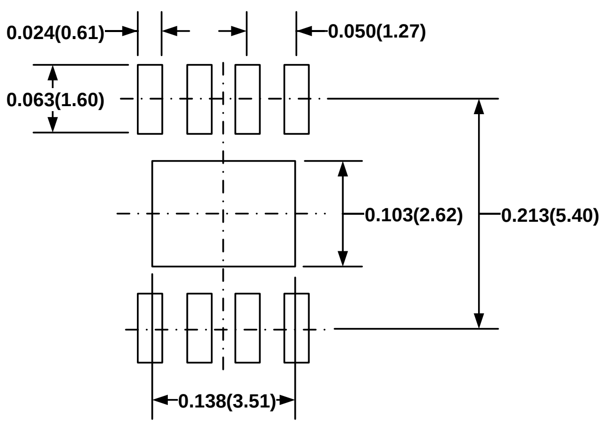
FRONT VIEW



SIDE VIEW



DETAIL "A"

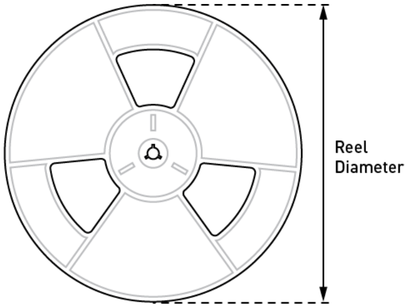


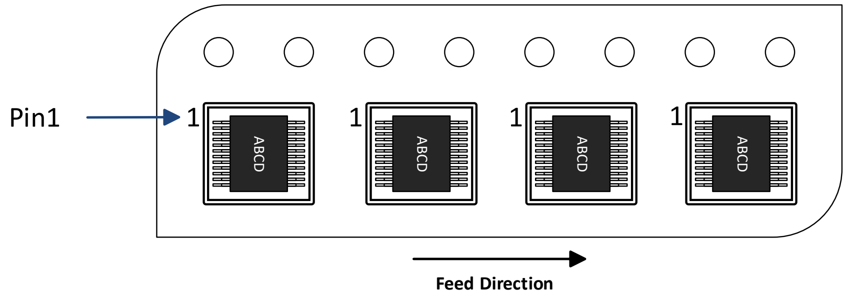
RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004 INCHES MAXIMUM.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4541GN-Z	SOIC-8EP	2500	100	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/28/2021	Initial Release	-