MP6005

High-Efficiency Flyback/Forward Controller with Primary and Secondary-Side Regulation

DESCRIPTION

The MP6005 is a high-power, high-efficiency flyback and forward controller. It is specifically designed as a low-cost, small, isolated solution with primary-side regulation (PSR) for flyback application, and high-efficiency secondary-side regulation (SSR) for active-clamped forward application. The MP6005 can also be used in SSR for flyback topology.

In PSR mode, the MP6005 senses the third winding waveform on the primary side to regulate the output and save the optocoupler and TL431 feedback circuit from SSR application. Continuous conduction mode (CCM) provides high efficiency under heavy load conditions, while the output diode compensation function supports good output regulation even during primary-side regulation. In SSR mode, the SYNC driver provides high efficiency for active-clamped forward topology.

The MP6005 includes a 2A gate driver, frequency dithering, overload protection (OLP), and over-voltage protection (OVP).

The MP6005 is available in an MSOP10 package.

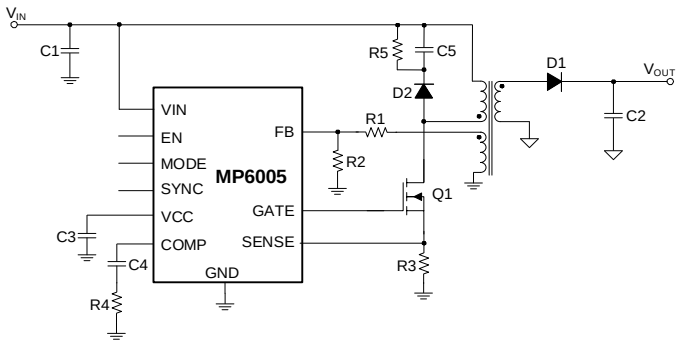
FEATURES

- Primary-Side Regulated Flyback without Optocoupler Feedback
- Synchronous Gate Driver (SYNC) Provides High Efficiency for Active-Clamped Forward Topology
- Wide 8V to 80V Input Voltage Range
- Internal Circuit Supply Compatible with 16V External Power
- 2A GATE and 0.8A SYNC Drivers
- 160mV Switching Current-Sense (CS) Limit
- Output Diode Compensation in Primary-Side Regulation (PSR) Mode
- 250kHz Fixed Switching Frequency
- Hiccup Protection, Overload Protection (OLP), Short-Circuit Protection (SCP), Over-Voltage Protection (OVP), and Thermal Shutdown
- Frequency Dithering to Reduce Electromagnetic Interference (EMI)
- Available in an MSOP10 Package

APPLICATIONS

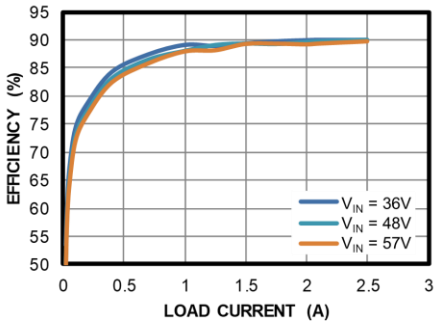
- Security Cameras
- Video Telephones
- Wireless Access Points (WAPs)
- Point-of-Sale (POS) Systems
- Power over Ethernet (PoE) Systems
- Industrial Isolated Power Supplies

TYPICAL APPLICATION



Efficiency

PSR flyback, V_{OUT} = 12V



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6005GK	MSOP10	*See Below*	1

* For Tape & Reel, add suffix –Z (e.g. MP6005GK–Z).

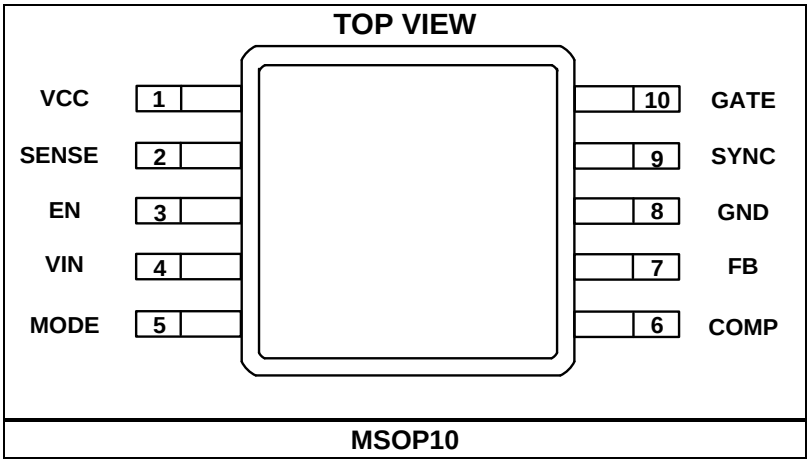
TOP MARKING

YWLLL

M6005

Y: Year code
W: Week code
LLL: Lot number
M6005: First five digits of the part number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Pin Function
1	VCC	**Internal circuit supply pin.** The VCC pin is powered by the internal LDO regulator (LDO) from the VIN pin. To bypass the internal regulator, connect a capacitor from the VCC pin to GND. The VCC capacitor has a 1μF minimum for flyback application, and a 4.7μF minimum for forward application. The VCC pin can also be powered by an external power source to reduce internal low-dropout loss.
2	SENSE	**Current-sense PSR, output voltage (V_{OUT}) compensation, and frequency dithering setting pin.** For function details, see the Output Voltage Compensation section and the Frequency Dithering section on page 17.
3	EN	**On/off control pin.** The EN pin is internally connected to GND through a 2.5MΩ resistor.
4	VIN	**Input power supply pin.** Connect a bypass capacitor from the VIN pin to GND.
5	MODE	**PSR/SSR mode and dead time setting pin.** For function details, see the Work Mode Detection section on page 15.
6	COMP	**Loop compensation pin**. In PSR mode, the COMP pin is the error amplifier (EA) output. In SSR mode, the COMP pin is pulled up to 5V through an internal 10kΩ resistor.
7	FB	**Output voltage feedback and OVP monitoring pin.** To regulate the output voltage in PSR mode, connect the FB pin to a resistor divider from the SENSE pin. The internal EA is disabled in SSR mode. The FB pin detects the OVP signal in both PSR and SSR mode. If OVP is not used in SSR mode, connect the FB pin to GND.
8	GND	**Ground.** Power return for the controller.
9	SYNC	**Synchronous MOSFET gate driver pin.**
10	GATE	**Main MOSFET gate driver pin.**

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to +100V
V_{CC}, V_{GATE}, V_{SYNC} ..... -0.3V to +18V
V_{EN} ..... -0.3V to +6.5V (2)
V_{FB} ..... -0.5V to +5.5V (3)
All other pins ..... -0.3V to +5.5V
EN sinking current 0.5mA (2)
FB sinking current ..... ±2mA (3)
Continuous power dissipation (T_A = +25°C) (4) (6)
MSOP10 ..... 1.62W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (5)

Supply voltage (V_{IN}) ..... 8V to 80V
Maximum VCC, GATE, SYNC voltage 16V
Maximum EN sink current 0.4mA (2)
Maximum FB sink current ..... ±1mA (3)
Operating junction temp (T_J) ... -40 °C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

MSOP10		
EV6005-K-00A (6)	77	17… °C/W
JESD51-7 (7)	150	65… °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) When V_{EN} is pulled high, a current limited by the external pull-up resistor flows into the EN pin. See the Enable (EN) Control section on page 15 for the EN pin's voltage rating description.
3) FB is clamped by the internal circuit. The sink and source currents should be limited. See the Setting the Output Voltage section on page 20 for details.
4) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on EV6005-K-00A, 2-layer 90mmx35mm PCB.
7) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 48V, V_{EN} = 5V, T_J = -40°C to +125°C [8], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply and Under-Voltage Lockout (UVLO)						
UVLO rising threshold	V_{IN-R}	V_{IN} rising, start charge V_{CC}	4.5	5.5	6.5	V
VIN UVLO falling threshold	V_{IN-F}	V_{IN} falling	3.8	4.8	5.8	V
VCC regulation voltage	V_{CC}	Load = 0mA to 20mA		8.5		V
VCC dropout voltage	$V_{CC-DROP}$	V_{IN} = 8V, I_{VCC} = 10mA		1.5		V
VCC UVLO rising threshold	V_{CC-R}	V_{IN} > V_{IN-R}, V_{CC} rising	5.4	5.7	6.0	V
VCC UVLO falling threshold	V_{CC-F}	V_{IN} > V_{IN-R}, V_{CC} falling	5.0	5.3	5.6	V
Quiescent supply current	I_Q	MODE pin float, V_{FB} = -0.1V, V_{SENSE} = 100mV, V_{COMP} = 0V, I_Q = I_{IN} - I_{COMP}, GATE and SYNC floating		800		µA
		V_{MODE} = 0V, V_{COMP} = 0V, I_Q = I_{IN} - I_{COMP}, GATE and SYNC floating		450		µA
Shutdown supply current	I_{SD}	V_{EN} = 0V			1	µA
Enable (EN) Control						
EN turn-on threshold	V_{EN-R}	Start switching	1.93	2	2.07	V
EN hysteresis	V_{EN-HYS}	Stop switching		0.2		V
EN high micro-power threshold	V_{EN-H}	Start internal logic			1.0	V
EN low micro-power threshold	V_{EN-L}	Stop internal logic	0.4			V
EN input current	I_{EN}	V_{EN} = 5V		2		µA
EN turn-on delay		EN on to GATE output		500		µs
Voltage Feedback						
FB reference voltage	V_{REF}	T_J = 25°C	1.98	2	2.02	V
		T_J = -40°C to +125°C	1.97	2	2.03	V
FB leakage current	I_{FB}	V_{FB} = 2V		10	50	nA
FB over-voltage protection (OVP) threshold	V_{FBOVP}		120%	125%	130%	V_{REF}
OVP hiccup off time				340		ms
Minimum diode conduction time for FB sample	t_{SAMPLE}			0.5	0.6 [9]	µs
Regulation compensation current into FB		V_{SENSE} = 50mV, $R_{SENSE-GND}$ = 3.3kΩ [10]		2.7		µA
		V_{SENSE} = 50mV, $R_{SENSE-GND}$ = 6.8kΩ [10]		5.4		µA
		V_{SENSE} = 50mV, $R_{SENSE-GND}$ = 12.7kΩ [10]		10.8		µA
Error Amplifier (EA)						
EA transconductance	G_{EA}	MODE floating, V_{FB} is ±50mV from V_{REF}, V_{COMP} = 1.5V		0.59		mA/V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{EN} = 5V, T_J = -40°C to +125°C (8), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
EA max source current	I_{EA}	MODE floating, V_{COMP} = 1.5V, V_{FB} = 1.9V		-110		μA
EA max sink current	I_{EA}	MODE floating, V_{COMP} = 1.5V, V_{FB} = 2.1V		110		μA
COMP high voltage	V_{COMP}	MODE floating, V_{FB} = 1.9V		4		V
		V_{MODE} = 0V, float COMP		5		
COMP internal pull-up resistor		SSR mode		10		kΩ
Soft Start (SS)						
Internal soft-start time	t_{SS}	When MODE is floating, test FB from 0V to 2V; when V_{MODE} = 0V, test COMP from 1.5V to 3.5V		4.7		ms
Current Sense (CS)						
Max CS	$I_{LIMIT-MAX}$		140	160	180	mV
Low current threshold	$I_{LIMIT-MIN}$	In PSR mode	33	36	39	mV
Short-circuit protection (SCP)			240	300	360	mV
Current leading-edge blanking time	t_{LED}			250		ns
CS amplifier gain	G_{CS}			11		V
SENSE input bias current		V_{SENSE} = 160mV		10	50	nA
Pulse-Width Modulation (PWM)						
Switching frequency	f_{SW}		225	250	275	kHz
Minimum foldback frequency in pulse-frequency modulation (PFM) mode		In PSR mode, V_{COMP} = 0V		30		kHz
Mode, Dead Time, Dither, V_{OUT} Compensation Setting (MODE and SENSE Pin)						
MODE detection current	I_{MODE}		35	40	45	μA
SENSE detection current	I_{SENSE}		90	100	110	μA
MODE/SENSE detection period	t_{MODE}/ t_{SENSE}			200		μs
MODE/SENSE detection threshold (11)	V_{MODE}/ V_{SENSE}	Voltage level 1 range			0.15	V
		Voltage level 2 range	0.25		0.4	V
		Voltage level 3 range	0.55		0.85	V
		Voltage level 4 range	1.1		1.5	V
		Voltage level 5 range	2.2			V
GATE Signal						
GATE sourcing impedance	I_{GATE}	I_{GATE} = -20mA		2		Ω
GATE sinking impedance	I_{GATE}	I_{GATE} = 20mA		1.7		Ω
GATE source current (12)		V_{CC} = 8.5V, GATE = 10nF, test gate rising speed		2		A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{EN} = 5V, T_J = -40°C to +125°C (8), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
GATE sink current (12)		V_{CC} = 8.5V, GATE = 10nF, test gate falling speed		1.7		A
GATE high voltage output	V_{GATE}		V_{CC} - 0.05			V
GATE low voltage output	V_{GATE}				0.05	V
GATE minimum on time	t_{ON-MIN}			250		ns
GATE max duty cycle	D_{MAX}			70		%
SYNC Signal						
SYNC sourcing impedance	I_{SYNC}	I_{GATE} = -20mA		5		Ω
SYNC sinking impedance	I_{SYNC}	I_{GATE} = 20mA		2		Ω
SYNC source current (12)		V_{CC} = 8.5V, SYNC = 10nF, test SYNC rising speed		0.8		A
SYNC sink current (12)		V_{CC} = 8.5V, SYNC = 10nF, test SYNC falling speed		1.2		A
SYNC high voltage output	V_{SYNC}		V_{CC} - 0.05			V
SYNC low voltage output	V_{SYNC}				0.05	V
Protections						
Overload protection (OLP) hiccup on time (12)				4.8		ms
OLP hiccup off time (12)				340		ms
Thermal shutdown temperature (12)	T_{SD}			150		°C
Thermal shutdown hysteresis (12)	T_{HYS}			20		°C

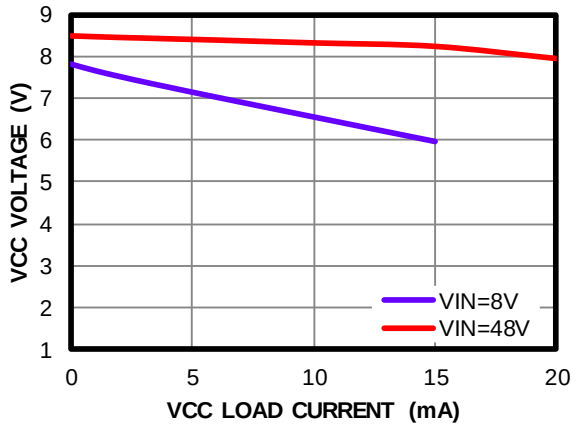
Notes:

8) Guaranteed by over-temperature correlation, not tested in production.
9) A minimum output diode conduction time greater than 0.7μs is recommended.
10) $R_{SENSE-GND}$ is the resistance from the SENSE pin to GND, which includes the CS resistor from the MOSFET source to GND and the resistor from the MOSFET source to the SENSE pin.
11) See Table 1 on page 15 and Table 2 on page 17 for voltage-level program options.
12) Guaranteed by sample characterization, not tested in production.

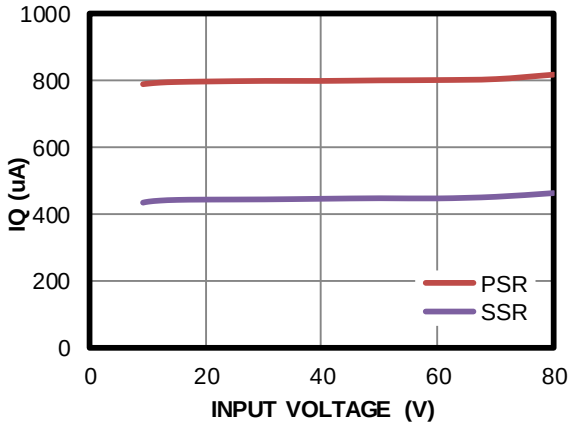
TYPICAL CHARACTERISTICS

V_{IN} = 48V, V_{EN} = 5V, T_A = 25°C, unless otherwise noted.

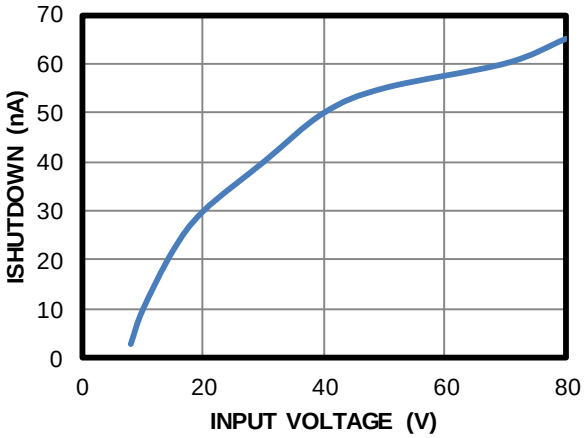
V_{CC} Load Regulation



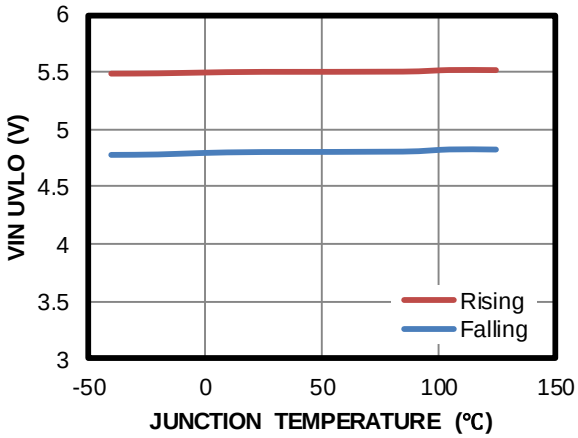
Quiescent Current vs. V_{IN}



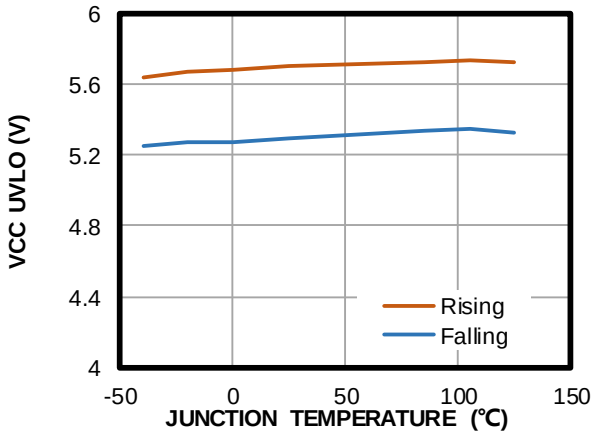
Shutdown Current vs. V_{IN}



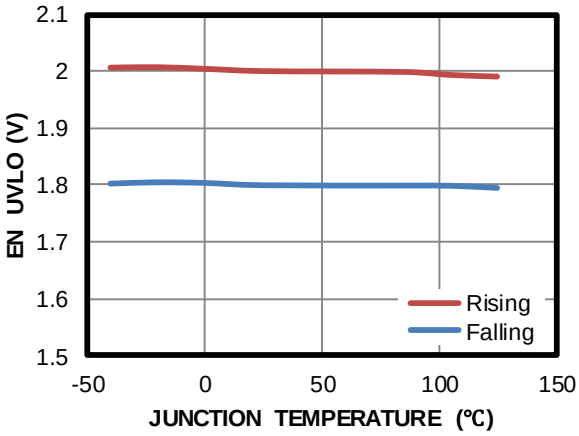
VIN UVLO vs. Junction Temp



VCC UVLO vs. Junction Temp



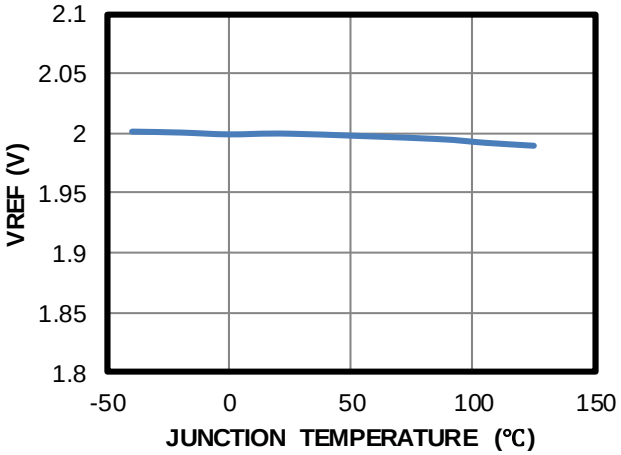
EN UVLO vs. Junction Temp



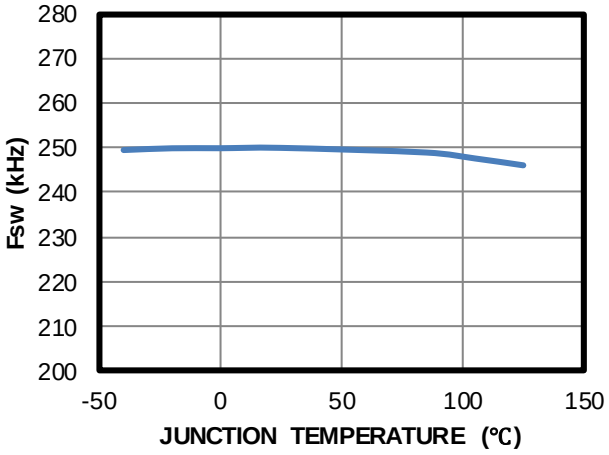
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{EN} = 5V, T_A = 25°C, unless otherwise noted.

V_{REF} vs. Junction Temp

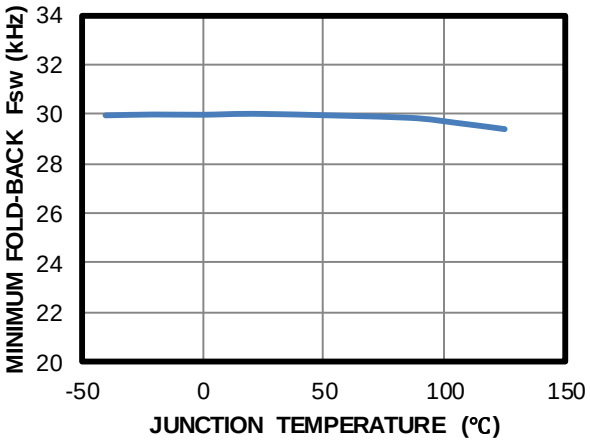


Switching Frequency vs. Junction Temp

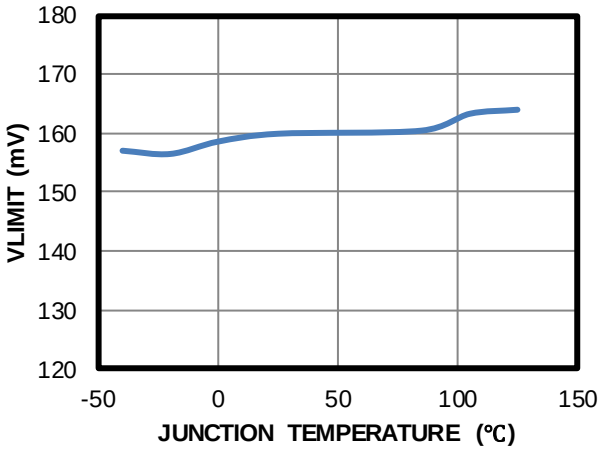


Minimum Foldback Frequency vs. Junction Temp

PSR mode

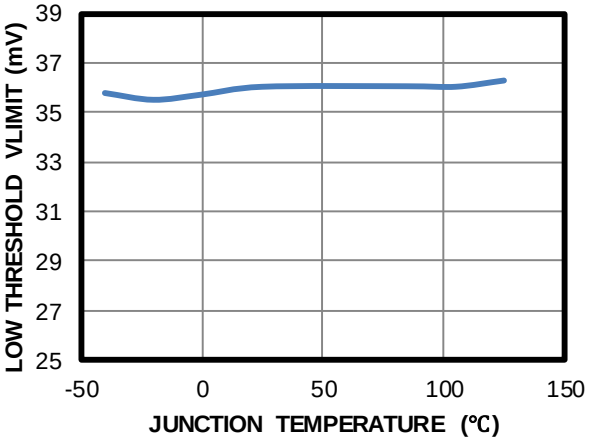


Current Limit Sense Voltage vs. Junction Temp

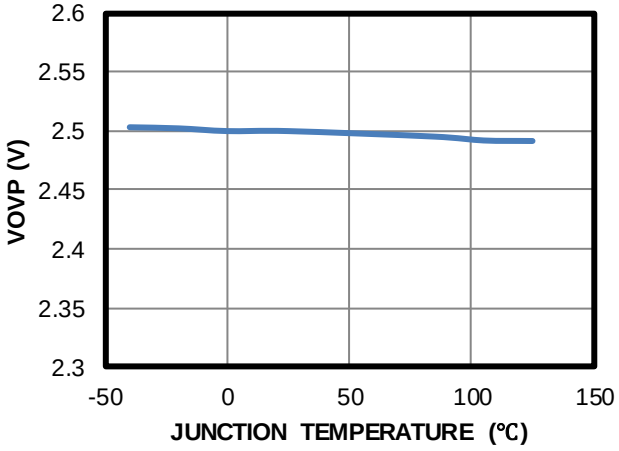


Low Threshold Current Limit Sense Voltage vs. Junction Temp

PSR mode



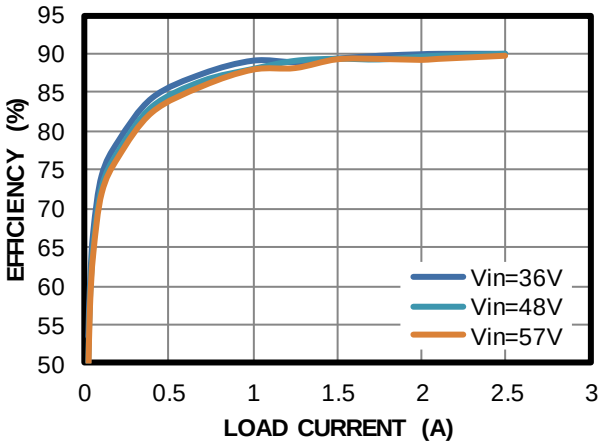
OVP Threshold vs. Junction Temp



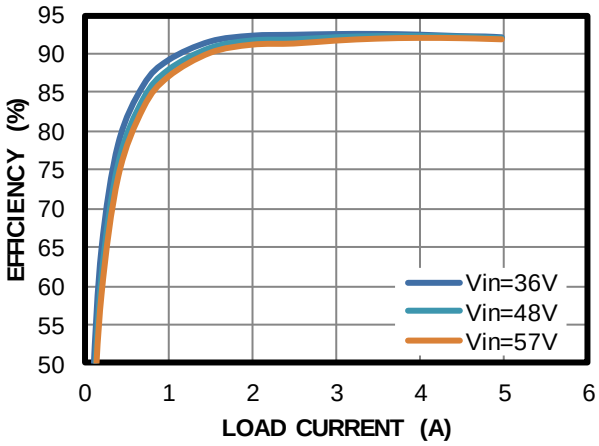
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{EN} = 5V, V_{OUT} = 12V, I_{OUT} = 2.5A, T_A = 25°C, unless otherwise noted.

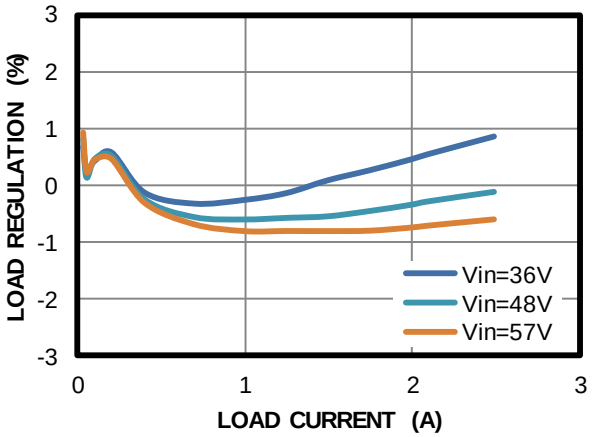
Efficiency
PSR flyback, V_{OUT} = 12V



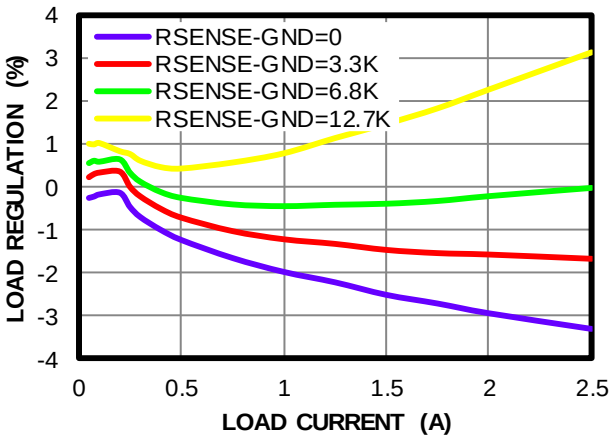
Efficiency
SSR forward, V_{OUT} = 5V



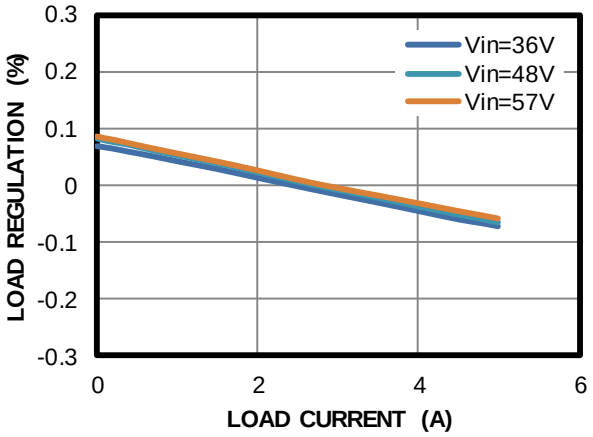
Load Regulation
PSR flyback, V_{OUT} = 12V, R_{FBH} = 100kΩ, $R_{SENSE-GND}$ = 6.8kΩ



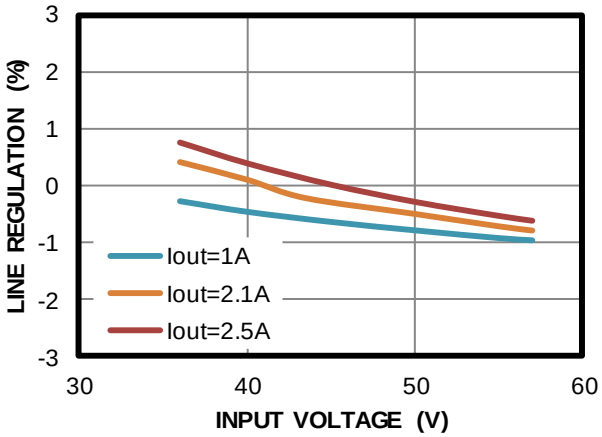
Load Regulation
PSR flyback, V_{IN} = 48V, V_{OUT} = 12V, R_{FBH} = 100kΩ



Load Regulation
SSR forward, V_{OUT} = 5V



Line Regulation
PSR flyback, V_{OUT} = 12V, R_{FBH} = 100kΩ, $R_{SENSE-GND}$ = 6.8kΩ

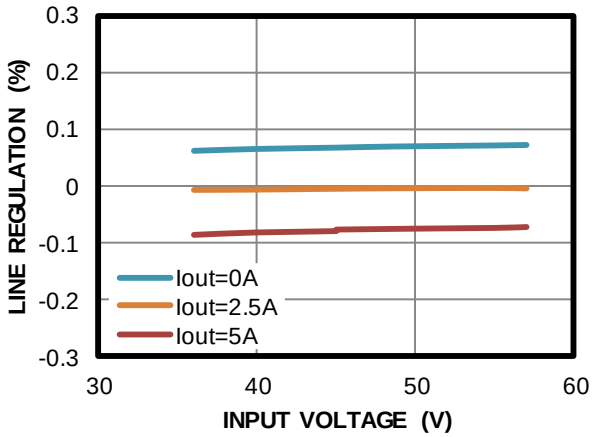


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{EN} = 5V, V_{OUT} = 12V, I_{OUT} = 2.5A, T_A = 25°C, unless otherwise noted.

Line Regulation

SSR forward, V_{OUT} = 5V

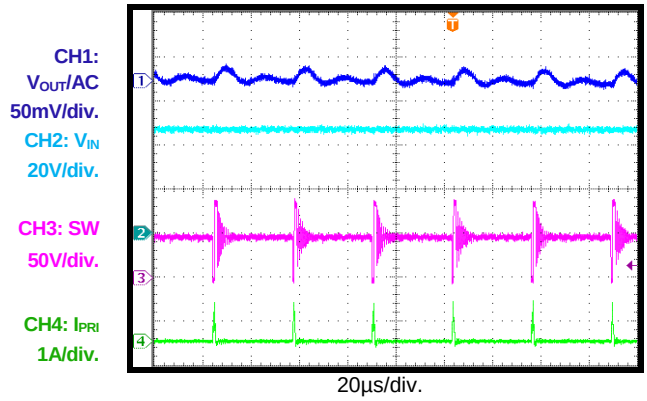


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{EN} = 5V, V_{OUT} = 12V, I_{OUT} = 2.5A, T_A = 25°C, unless otherwise noted.

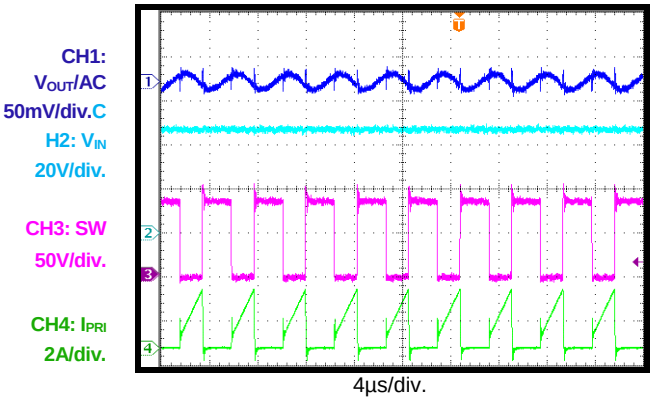
Steady State

I_{OUT} = 30mA



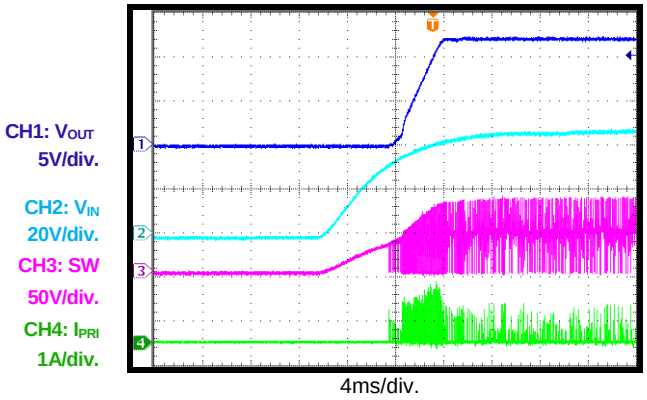
Steady State

I_{OUT} = 2.5A



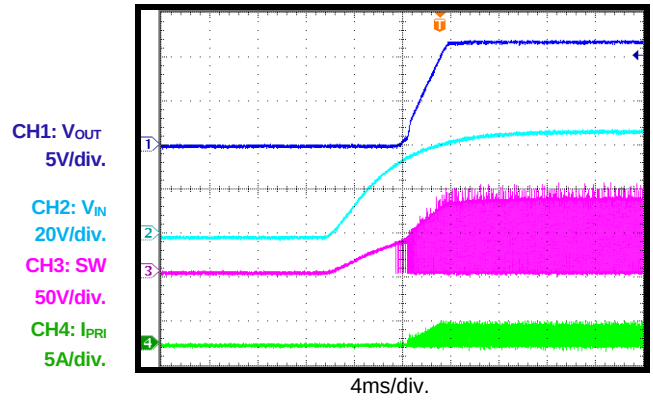
Start-Up through VIN

I_{OUT} = 30mA



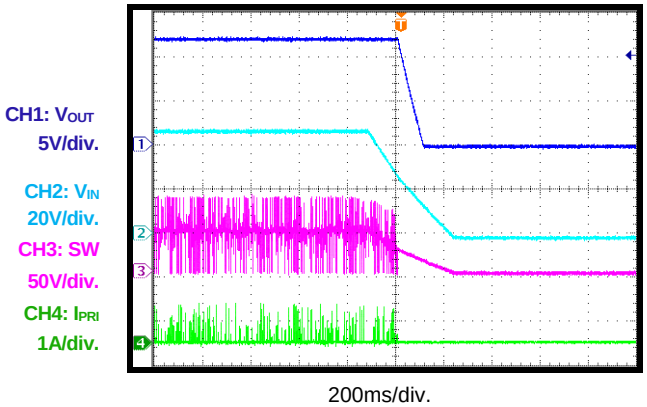
Start-Up through VIN

I_{OUT} = 2.5A



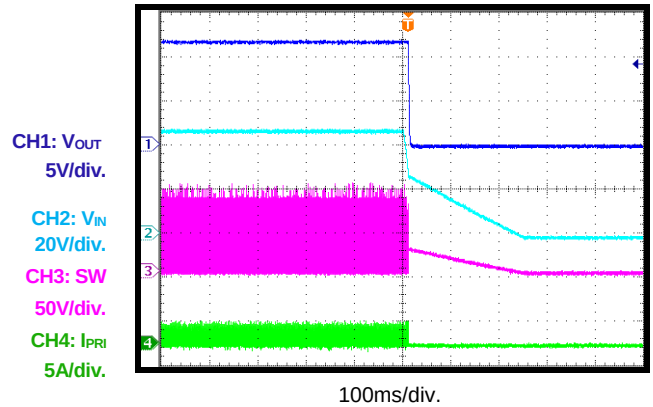
Shutdown through VIN

I_{OUT} = 30mA



Shutdown through VIN

I_{OUT} = 2.5A

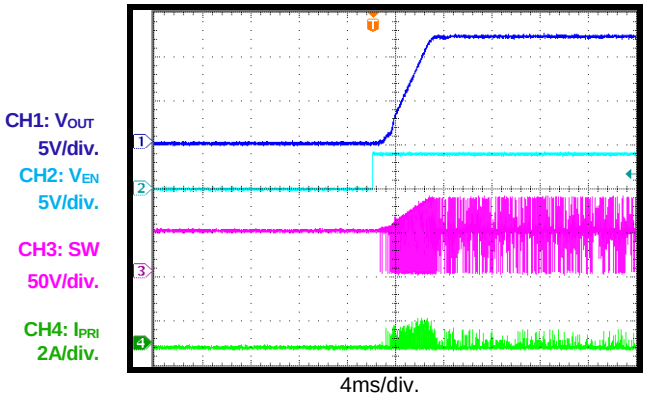


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{EN} = 5V, V_{OUT} = 12V, I_{OUT} = 2.5A, T_A = 25°C, unless otherwise noted.

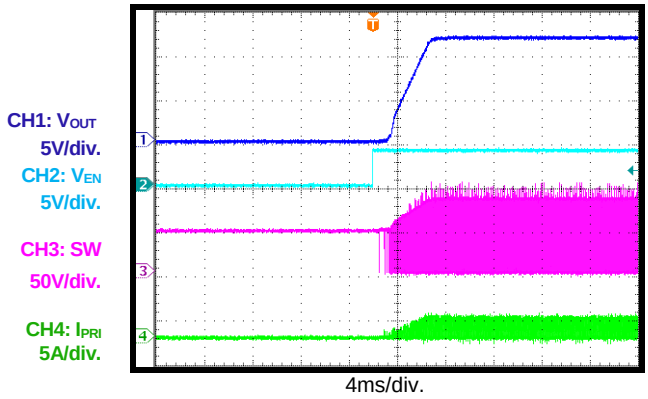
Start-Up through EN

I_{OUT} = 30mA



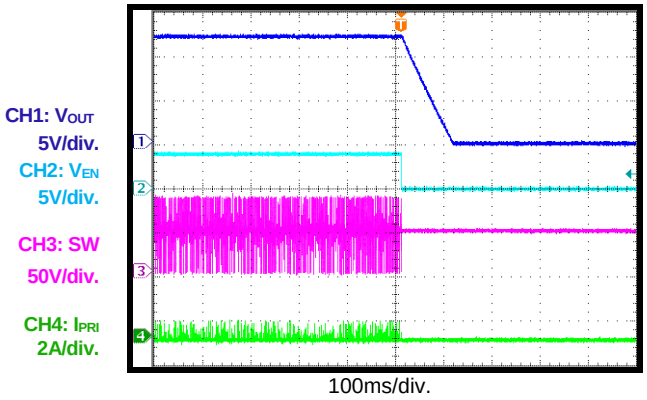
Start-Up through EN

I_{OUT} = 2.5A



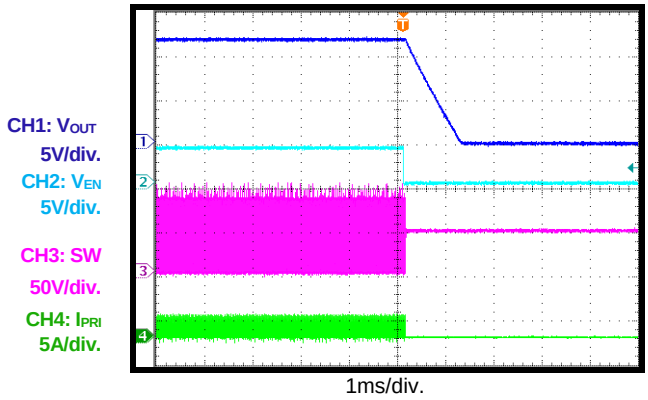
Shutdown through EN

I_{OUT} = 30mA



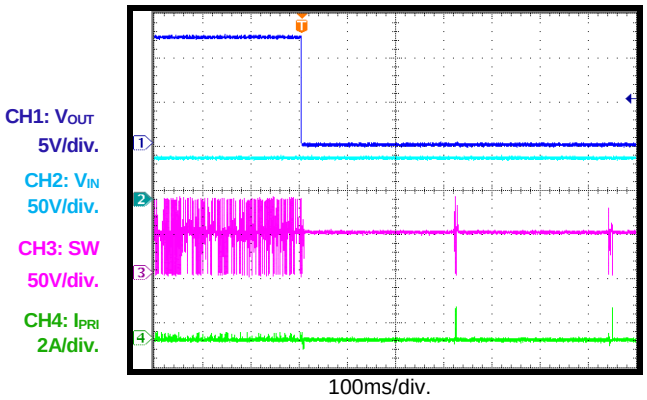
Shutdown through EN

I_{OUT} = 2.5A



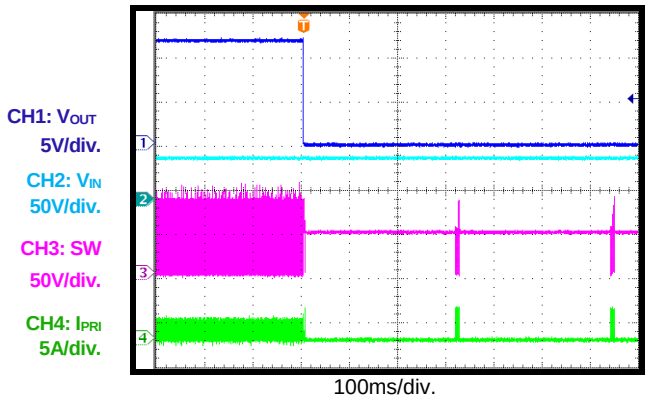
SCP Entry

I_{OUT} = 30mA to short



SCP Entry

I_{OUT} = 2.5A to short

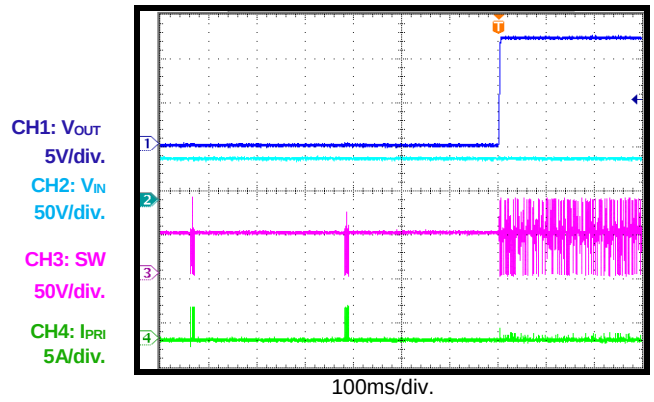


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{EN} = 5V, V_{OUT} = 12V, I_{OUT} = 2.5A, T_A = 25°C, unless otherwise noted.

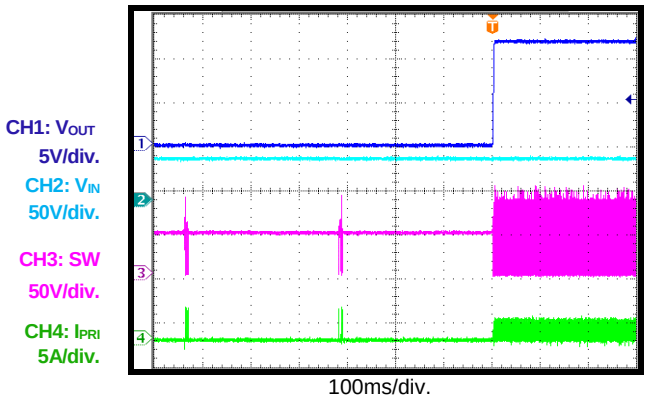
SCP Recovery

I_{OUT} = short to 30mA



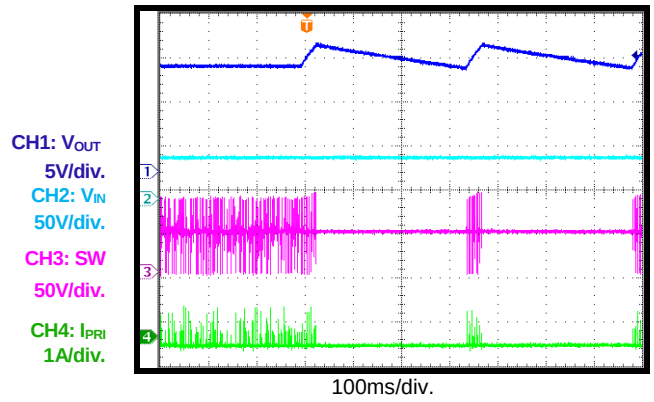
SCP Recovery

I_{OUT} = short to 2.5A



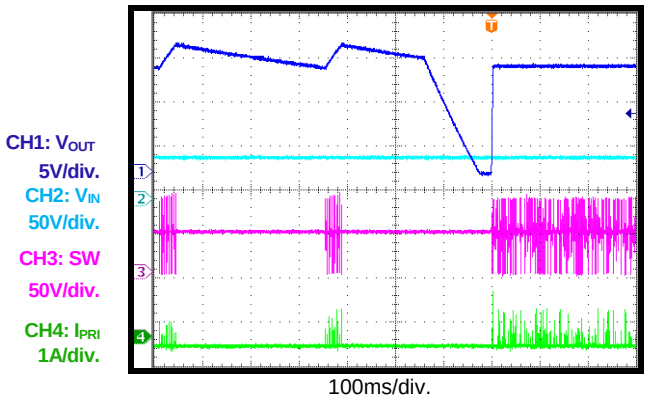
OVP Entry

I_{OUT} = 30mA to 2mA



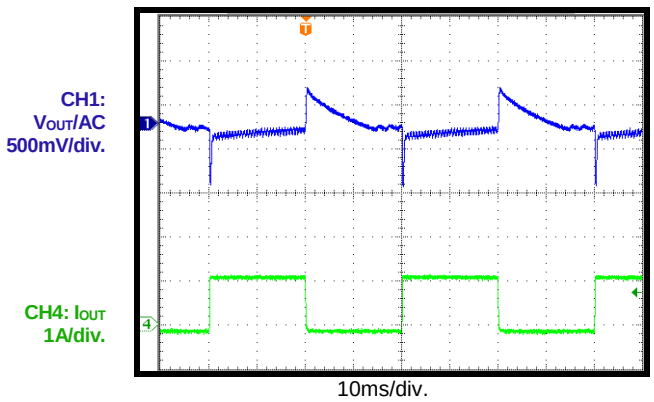
OVP Recovery

I_{OUT} = 2mA to 30mA



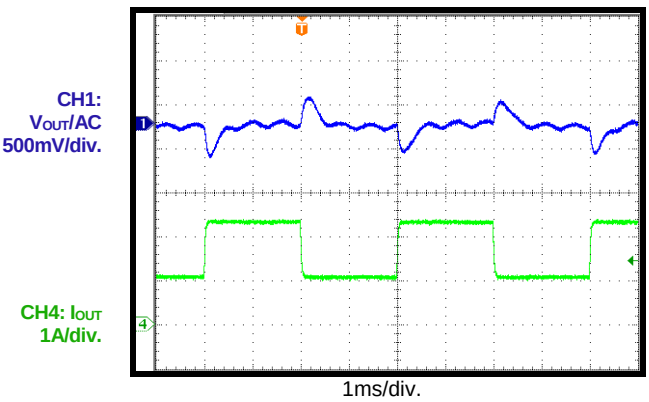
Load Transient

I_{OUT} = 30mA to 1.25A, I_{RAMP} = 50mA/µs,
R_{FBH} = 100kΩ, $R_{SENSE-GND}$ = 6.8kΩ



Load Transient

I_{OUT} = 1.25A to 2.5A, I_{RAMP} = 50mA/µs,
R_{FBH} = 100kΩ, $R_{SENSE-GND}$ = 6.8kΩ



FUNCTIONAL BLOCK DIAGRAM

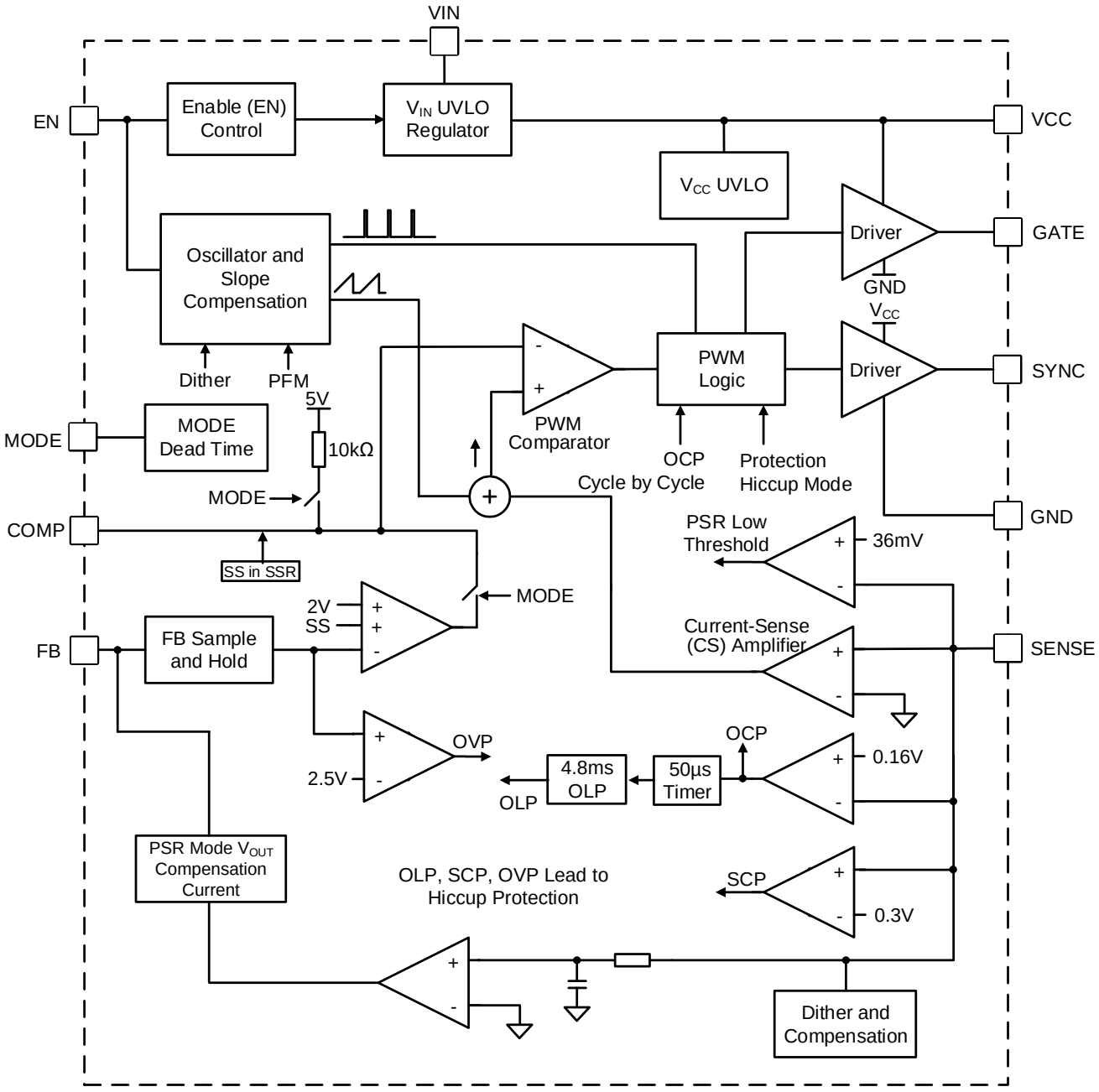


Figure 1: Functional Block Diagram

OPERATION

Start-Up and Power Supply

The MP6005 features an 80V internal start-up circuit. When the input voltage (V_{IN}) exceeds 5.5V, the VCC pin's capacitor is charged by the internal LDO regulator (LDO). Typically, if V_{IN} exceeds 10V, the VCC's pin voltage (V_{CC}) is regulated at 8.5V and VCC under-voltage lockout (UVLO) is 5.7V. Aside from VCC UVLO, the MP6005 also has EN UVLO (typically 2V). When V_{CC} exceeds the 5.7V UVLO threshold and the EN pin is pulled high, the part begins operating.

After the MP6005 turns on, the VCC pin can be powered by the auxiliary winding transformer to reduce IC power loss. The auxiliary power must be greater than V_{CC} regulation (8.5V) to override the internal LDO. The internal reverse-blocking circuit allows V_{CC} to exceed V_{IN} if V_{CC} has bias power. V_{CC} should be below 16V due to the pin's voltage rating.

If V_{IN} is below 8.5V and V_{CC} is not regulated at 8.5V, the internal high-voltage VCC LDO has a voltage drop of about 1.5V. This allows the MP6005 to work when V_{IN} is as low as 8V.

Enable (EN) Control

The EN pin is the on/off control for the MP6005. When the EN pin's voltage (V_{EN}) exceeds 1V, the MP6005's micro-power mode allows the device to turn on some of the internal circuits. If V_{EN} exceeds the turn-on threshold (2V), all functions are turned on and the GATE/SYNC driver signal starts up. The GATE/SYNC signal can be disabled if V_{EN} drops to about 1.8V. Micro-power mode is only disabled after V_{EN} drops below 0.4V. After shutdown, the MP6005 sinks a current below 1µA from the input power supply.

EN can program the VIN pin's start-up voltage through a resistor divider. The maximum recommended voltage for EN is 6.5V. If EN's divider voltage exceeds 6.5V, it is recommended to use a divider resistor to limit the current going into EN. One internal Zener diode on EN clamps V_{EN} when the divider voltage exceeds 6.5V. Ensure the clamped Zener diode current into EN is below 0.4mA with an external pull-up resistor.

Work Mode Detection

After turning on, the MP6005 produces a 40µA output current to the MODE pin to detect the resistor setting. If the MODE pin's voltage (V_{MODE}) exceeds 2.2V, the MP6005 works in primary-side regulation (PSR) mode, and the internal error amplifier (EA) turns on. If MODE is connected to GND through a resistor.

the MP6005 works in secondary-side regulation (SSR) mode and the internal EA turns off while COMP is pulled up to the internal 5V power source through a 10kΩ resistor. Table 1 shows MODE program options.

Table 1: MODE Program Options

MODE to GND Resistance (kΩ)			Work Mode	Dead Time (ns)
Min	Typ (1%)	Max		
0	0	3.3	SSR	100
7.32	7.5	8.2	SSR	150
16	16.9	18.7	SSR	200
32.4	32.4	33	SSR	300
64.9	Float	Float	PSR	150

In PSR mode, the output voltage (V_{OUT}) feedback signal is detected by auxiliary winding from the FB pin. Under light-load conditions, the MP6005 reduces the frequency accordingly. Under no-load conditions, the frequency remains above 30kHz. In SSR mode, the V_{OUT} feedback signal is detected by the COMP pin, and the MP6005 maintains a fixed frequency. The peak current is regulated by the COMP pin's voltage (V_{COMP}) until the MP6005's power-save mode (PSM) is triggered.

Once the MP6005 turns on, there is a 500µs period before the device starts switching. The MODE pin, dead time, dither, and V_{OUT} compensation are detected during this period.

The MODE pin determines the PSR and SSR modes. It also programs the dead time between the GATE and SYNC pins. Table 1 shows the programming options.

The MODE detection current lasts about 200µs. Typically, a resistor from MODE to GND is sufficient. A capacitor from MODE to GND may be required for filtering in a noisy environment. This capacitor must be below 100pF to allow

MODE to rise to steady state before the MP6005 detects V_{MODE}.

Pulse-Width Modulation (PWM) Operation

The MP6005 can be set for flyback or forward topology. In flyback topology, the external N-channel MOSFET turns on at the beginning of each cycle and forces the transformer current to increase. The current through this MOSFET is sensed after the sum of the SENSE current and slope compensation exceed V_{COMP}. After the current is sensed, the external MOSFET turns off. The transformer current then transmits energy from the primary-side winding to the secondary-side winding, and charges the output capacitor through the Schottky diode. The transformer's primary-side current is controlled by V_{COMP}, which is controlled by the output feedback voltage. Therefore, the output voltage controls the transformer current to satisfy the load. In forward topology, energy is transferred from the primary-side to secondary-side winding while the primary-side N-channel MOSFET is on. The primary-side peak current is controlled by V_{COMP}, which is controlled by an external TL431 regulator and optocoupler feedback.

See the Voltage Control section below for details on output voltage feedback.

Voltage Control

PSR Mode

Unlike traditional flyback with optoisolator feedback, the MP6005 can detect the feedback (FB) pin's auxiliary winding voltage during the secondary-side output diode conduction period.

Assume the secondary winding acts as the master, and the auxiliary winding acts as the slave. When the secondary-side diode conducts, the feedback voltage can be calculated with Equation (1):

$$V_{FB} = \frac{N_A}{N_S} \times (V_{OUT} + V_{DOF}) \times \frac{R_{FBL}}{R_{FBH} + R_{FBL}} \quad (1)$$

Where V_{DOF} is the output diode forward-drop voltage, V_{OUT} is the output voltage, N_A is the auxiliary winding turn, N_S is the secondary-side output winding, and R_{FBH} and R_{FBL} are the resistor dividers for feedback sampling.

Figure 2 shows feedback sample control in discontinuous conduction mode (DCM).

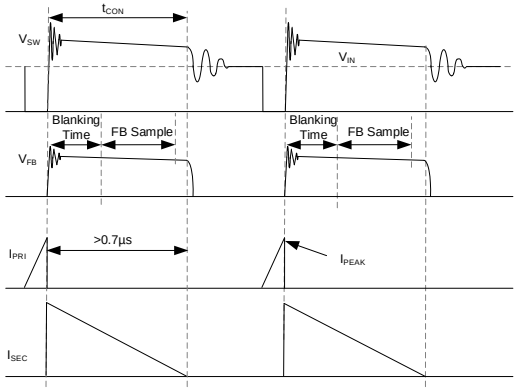


Figure 2: Discontinuous Conduction Mode (DCM) Condition Feedback Sample Control

Figure 3 shows feedback sample control in continuous conduction mode (CCM).

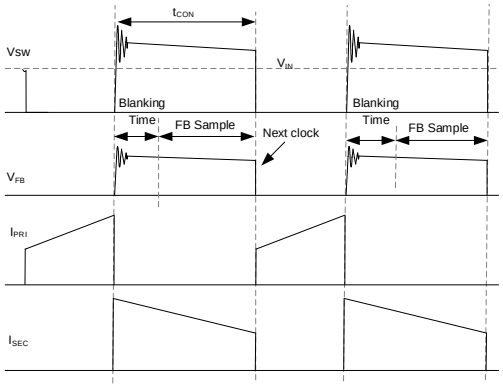


Figure 3: Continuous Conduction Mode (CCM) Condition Feedback Sample Control

The MP6005 regulates the primary-side MOSFET V_{SENSE} current above 36mV and begins sampling the auxiliary-winding voltage after the power MOSFET turns off. A 300ns blanking time is added to avoid spike ringing due to leakage inductance. To guarantee a sufficient feedback sample period under light-load conditions, the output diode current conduction time (t_{CON}) should exceed 600ns before the diode current drops to 0A in each cycle. It is recommended to design the transformer to ensure that t_{CON} exceeds 700ns when V_{SENSE_PK} = 33mV. The MP6005 GATE signal also provides a 1.2µs minimum off time, limited by a 70% max duty cycle, to guarantee sufficient feedback sample time while the MP6005 works in a high duty cycle. During the feedback sense period, the FB pin's signal is sent to the negative EA input, and remains there after the sense window has elapsed. The EA voltage output (V_{EA}) is generated on the

COMP pin, and controls the transformer peak current to match the regulated output voltage.

Secondary-Side Regulation (SSR) Mode

The MP6005 can work in secondary-side regulation (SSR) mode. In SSR mode, the V_{OUT} signal is fed back to the COMP pin through one optocoupler, and the PSR feedback voltage detection is disabled. The FB pin should be connected to GND.

The MP6005 has a fixed frequency while in SSR mode under light-load conditions. The peak current continues to drop towards V_{COMP} until the PSM threshold is triggered. The 36mV minimum current limit does not work in SSR mode.

In SSR mode, the MP6005 supports both flyback and forward topology. In PSR mode, the MP6005 only supports flyback topology.

Output Voltage Compensation

In PSR mode, the auxiliary winding waveform reflects the secondary-side winding voltage, but the output voltage differs from the winding output voltage due to the output diode voltage drop and the power winding resistance (see Figure 4). The dropout voltage varies as the conduction current changes. As the current varies, the resistance from the SENSE pin to GND sets the compensation gain of the dropout voltage. The current-sense (CS) signal is filtered internally, and controls the current sinking from the FB pin based on the average voltage from the SENSE pin. There are three types of current gain from the average V_{SENSE} to the FB sinking current (see Table 2 for SENSE programming options). The FB sinking current creates a voltage drop on the FB pin's high-side (HS) feedback resistor to compensate for V_{OUT}.

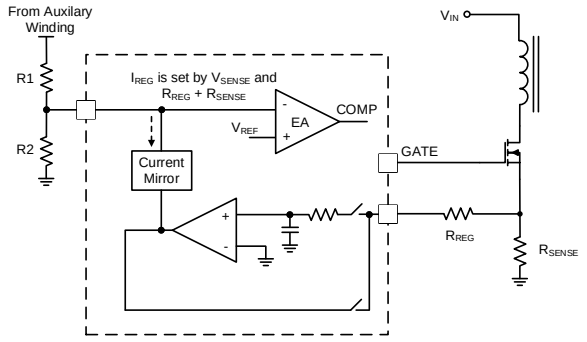


Figure 4: Output Voltage Compensation

The voltage compensation function is disabled in SSR mode.

Frequency Dithering

The MP6005 has a frequency dithering circuit that minimizes electromagnetic interference (EMI). During steady state, the frequency is fixed internally, but the frequency dithering circuit is added to the configured frequency with a 1.5kHz modulation. In PSR mode, frequency dithering is fixed at ±6% of the switching frequency. In SSR mode, frequency dithering can be set at ±3%, ±6%, or ±9%, depending on the resistor connected from the SENSE pin to GND.

Table 2 shows dithering and V_{OUT} compensation programming options.

Table 2: SENSE Program Options

SENSE to GND Resistance (kΩ) (13)			PSR Mode		SSR Mode
Min	Typ (1%)	Max	Dither Range (kHz)	I_{FB} / V_{SENSE} Ratio (μA/mV)	Dither Range (kHz)
0	0	1.3	0	0	0
3	3.3	3.6	±15	0.05	±7.5
6.2	6.8	7.5	±15	0.1	±15
12.7	12.7	13	±15	0.2	±22.5
24.9	25.5	28	±15	0	±22.5

After start-up, the SENSE detection current continues for about 200μs. Typically, a resistor from the SENSE pin to GND is sufficient. An additional capacitor from SENSE to GND may be required for filtering in a noise environment.

Notes:

13) $R_{SENSE-GND}$ is the resistance from the SENSE pin to GND, which includes the CS resistor from the MOSFET source to GND and the resistor from the MOSFET source to the SENSE pin.

Current Sense (CS) and Over-Current Protection (OCP)

The MP6005's external MOSFET current is sensed by the SENSE pin, which amplifies V_{SENSE} to feed the high-speed current comparator for current control mode. The current comparator uses V_{SENSE} and the slope compensation as one of its inputs, and compares that value to V_{COMP}. If the amplified current exceeds V_{COMP}, then the comparator output decreases and turns off the power MOSFET.

If V_{SENSE} exceeds the current-limit threshold (typically 160mV), the MP6005 turns off the GATE output.

Then the internal oscillator begins the next cycle and senses the current again. The MP6005 limits the MOSFET current cycle by cycle.

Error Amplifier (EA)

In PSR mode, the MP6005 senses the feedback voltage (V_{FB}) during the flyback period with the feedback pulse signal. The feedback signal is then held and fed to the error amplifier (EA). The EA regulates V_{COMP} based on the feedback signal, and V_{COMP} controls the transformer peak current to regulate V_{OUT}.

In SSR mode, the internal EA is disabled and the COMP pin is pulled up by an internal resistor. The external optocoupler can be connected to COMP for V_{OUT} signal feedback.

Light-Load Control

Under light-load conditions in PSR mode, V_{COMP} decreases to regulate the low transformer peak current. If the peak current signal is below 36mV, the MP6005 stops decreasing the transformer current, and instead decreases the frequency. As a result, the transferred energy decreases, and V_{OUT} is regulated.

In light-load PSR mode, the MP6005 sets the minimum frequency above 30kHz. This helps the device detect the output voltage and avoid audible noise. The minimum frequency requires some load to maintain V_{OUT}, so that V_{OUT} does not rise and trigger over-voltage protection (OVP).

Under light-load conditions in SSR mode, the MP6005 maintains a fixed frequency and V_{COMP} continues to drop toward the PSM threshold.

Over-Voltage Protection (OVP)

The MP6005 includes over-voltage protection (OVP). If V_{FB} exceeds 125% of V_{REF}, the MP6005 turns off the GATE signal and enters hiccup mode. Once the fault has been removed, the MP6005 turns on again after a 340ms delay, and then resumes normal operation. Connect the FB pin to GND if the OVP function is not used.OVP sampling has a blanking time to avoid mistriggering due to the oscillation of the leakage inductance and parasitic capacitance.

Overload Protection (OLP)

The MP6005 limits the peak current cycle by cycle under OCP conditions. If the load continues to increase after triggering OCP, V_{OUT} decreases and the peak current triggers OCP for each cycle.

The MP6005 sets overload detection by monitoring V_{SENSE}. Once the internal soft start is complete, overload protection (OLP) turns on. If an OCP signal longer than 4.8ms is detected, the MP6005 turns off the gate driver. After a 340ms delay, the MP6005 turns on again with the next cycle. During OLP, a 50µs one-shot timer is activated after one OCP pulse. This means if there is one OCP pulse in a 50µs period, the MP6005 registers this event as OCP. If the OCP condition is removed before 4.75ms, the MP6005 resumes normal operation.

Short-Circuit Protection (SCP)

When the output is shorted to GND, the MP6005 works in OCP mode and the current is limited cycle by cycle.

If the peak current is not limited by the 160mV V_{SENSE} in each cycle because of the gate driver's minimum on time, the current may run out of control and the transformer may saturate. If V_{SENSE} reaches 300mV, the MP6005 turns off the gate driver and enters hiccup protection with a 340ms off time.

Once the short circuit is removed, V_{OUT} recovers after a 340ms delay and then enters the next cycle.

Soft Start (SS)

The MP6005 employs soft start (SS) by charging an internal capacitor from a current source. During the soft-start period, the SS signal ramps up slowly. In the event of a command shutdown, thermal shutdown, or protection condition, the soft-start capacitor is completely discharged.

In PSR mode, the soft-start signal clamps the feedback V_{REF}. From 0V to 2V, the feedback reference soft-start time is typically 4.7ms.

In SSR mode, the soft-start signal clamps V_{COMP} until it reaches the switching current level. The soft-start signal continues to ramp up at the same rate. V_{COMP}'s ramp time from 1.5V to 3.5V is typically 4.7ms.

Minimum On Time

The parasitic transformer capacitance and GATE signal create a current spike on the SENSE resistor when the power MOSFET turns on. The MP6005 includes a 250ns leading-edge blanking period to avoid false termination of the switching pulse. During this blanking period, the CS comparator turns off and the gate driver remains on.

Gate Driver

The MP6005 has a high-current gate driver for the primary-side N-channel MOSFET. This driver has strong driving capability and benefits for MOSFET selection by allowing the MOSFET's V_{GS} to be charged quickly. If Q_G is low, then the switching speed should remain low as well. It is recommended to use a series resistor above 5Ω to reduce EMI.

The MP6005 has a SYNC driver pin that controls the second switch. If SYNC is high, the second switch turns off. If SYNC is low, the second switch turns on. Figure 4 shows the phase and dead time relationships between the GATE and SYNC pins.

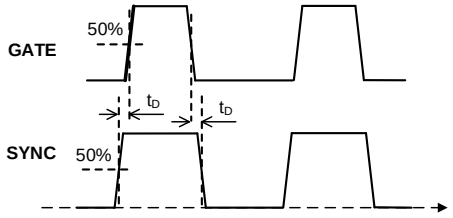


Figure 5: GATE and SYNC Driver

Both GATE and SYNC maintain a low voltage if UVLO or another protection mode has turned off the IC.

Transformer Inductance

In PSR mode, the MP6005 samples V_{OUT} during the flyback time, and the secondary diode conduct time with minimum peak current (controlled by 33mV minimum sense limit) should be longer than 0.7μs. The transformer inductance can be calculated with Equation (2):

$$L_{PRI} \geq (V_{OUT} + V_{DOF}) \times \frac{N_P}{N_S} \times 0.7\mu. \times \frac{R_{SENSE}}{33mV} \quad (2)$$

Where L_{PRI} is the transformer's primary inductance, and V_{DOF} is the output rectifier diode's forward drop.

There is no inductance limit in SSR mode. However, if the IC is designed to work in continuous conduction mode (CCM), set the peak current high to avoid triggering PSM, which may lead to a larger V_{OUT} ripple, (particularly in SYNC mode forward topology).

Thermal Shutdown

Thermal shutdown prevents thermal runaway. If the silicon die temperature exceeds its upper threshold, the MP6005 turns off. Once the temperature returns to below its lower threshold, thermal shutdown ends and the device turns on again with the next new cycle.

APPLICATION INFORMATION

Setting the Output Voltage

The MP6005 has two feedback modes: primary-side regulation (PSR) and secondary-side regulation (SSR).

In PSR mode, the converter detects the auxiliary winding voltage from the FB pin. The resistor dividers (R_{FBH} and R_{FBL}) are used for feedback sampling (see Figure 5).

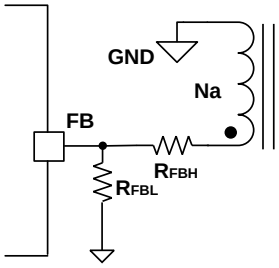


Figure 6: Feedback in PSR Mode

When the primary-side power MOSFET turns off, the auxiliary winding voltage is proportional to the output winding. V_{OUT} can be estimated with Equation (3):

$$V_{OUT} = \frac{V_{REF} \times (R_{FBH} + R_{FBL})}{R_{FBL}} \times \frac{N_S}{N_A} - V_{DOF} \quad (3)$$

Where N_S is the transformer's secondary side winding turns, N_A is the transformer's auxiliary winding turns, V_{DOF} is the output rectifier diode's forward drop, and V_{REF} is the reference voltage of FB.

When the main power MOSFET turns on, the auxiliary winding voltage is negative, and V_{FB} is limited by an internal circuit. The FB current can be estimated with Equation (4):

$$I_{FB} = \frac{1}{R_{FBH}} \times (\frac{V_{IN} \times N_A}{N_P}) \quad (4)$$

R_{FBH} should be high enough to limit FB's negative current to less than 1mA. Due to FB's parasitic capacitance, R_{FBH} should be lower than 100kΩ.

In SSR Mode, V_{OUT} is set by an external TL431 regulator, For example, if the regulator's V_{REF} = 2.5V and V_{OUT} = 12V, then the upper and lower divider resistor ratio is 3:8. The regulator generates an amplified signal and controls the MP6005's COMP pin through an optocoupler (e.g. a PC357). The COMP pin controls the current, and the feedback signal regulates V_{OUT}.

Setting Work Mode

After the MP6005 turns on, it outputs a 40μA current to the MODE pin to detect the MODE resistance. If V_{MODE} exceeds 2.2V, the MP6005 works in PSR. Otherwise, the MP6005 works in SSR. The MODE pin programs the dead time between the GATE and SYNC pins. See Table 1 on page 15 for more details on MODE programming options.

Setting Enable (EN) Control

The EN pin programs the VIN pin's start-up voltage through a resistor divider. Figure 7 shows the programmable UVLO through EN.

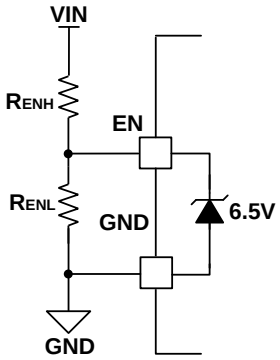


Figure 7: Programmable UVLO through EN

EN's recommended maximum voltage is 6.5V. If the EN divider voltage exceeds 6.5V, the resistance connected to VIN (R_{ENH}) limits the current flowing to the EN pin. If the divider voltage exceeds 6.5V, an internal Zener diode on the EN pin clamps V_{EN}. Ensure the clamped Zener diode current is below 0.4mA.

Setting the VCC Power Supply

V_{CC} is regulated by an internal LDO from the VIN pin. V_{CC} is typically regulated at 8.5V. It is recommended to use a decoupling capacitor between the VCC pin and GND.

In flyback mode, it is recommended to use a minimum 1μF capacitor. VCC can also be powered by transformer auxiliary winding to reduce high-voltage LDO power loss.

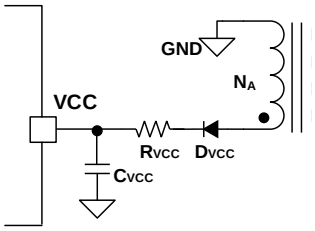


Figure 8: Flyback VCC from N_A Winding

The auxiliary winding supply voltage can be calculated with Equation (5):

$$V_{CC} = \frac{N_A}{N_S} \times (V_{OUT} + V_{DOF}) - V_{DVCCF} \quad (5)$$

Where V_{DVCCF} is the D_{VCC} diode voltage drop from the auxiliary winding.

In forward mode, it is recommended to have the VCC capacitor be less than 4.7µF. VCC can also be powered by the auxiliary winding transformer. Figure 9 shows VCC from the N_A winding in forward mode.

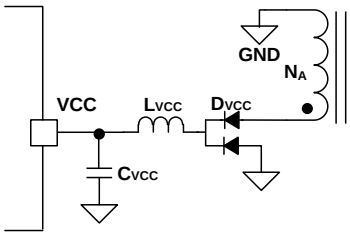


Figure 9: Forward VCC from N_A Winding

The auxiliary winding supply voltage can be calculated with Equation (6):

$$V_{CC} = \frac{N_A}{N_S} \times V_{OUT} \quad (6)$$

V_{CC} should be less than 16V.

Setting Output Voltage (V_{OUT}) Compensation and Frequency Dithering

The SENSE pin sets the output voltage (V_{OUT}) compensation and frequency dithering functions. After turning on, the MP6005 outputs a 100µA current to the SENSE pin to detect the SENSE resistance. Based on the resistance, the MP6005 determines the compensation and frequency dithering type. See Table 2 on page 17 for SENSE programming options.

The V_{OUT} compensation function only works in PSR mode.

Setting the Current-Sense (CS) Resistor

The external MOSFET current is sensed by a sensing resistor. If V_{SENSE} exceeds the current-limit threshold (typically 160mV), the MP6005 turns off the GATE output for the cycle.

To avoid exceeding the current limit, the voltage across the sense resistor (R_{SENSE}) should be less than 80% of the current limit voltage (160mV). R_{SENSE} can be estimated with Equation (7):

$$R_{SENSE} = \frac{0.8 \times 160_{mV}}{I_{PEAK}} \quad (7)$$

Where I_{PEAK} is the primary-side peak current.

Selecting a Power MOSFET

The MP6005 drives a wide variety of N-channel MOSFETs. The critical parameters of selecting a MOSFET are the maximum drain-to-source voltage ($V_{DS(MAX)}$), maximum current ($I_{D(MAX)}$), on resistance ($R_{DS(ON)}$), total gate charge (Q_G), and turn-on threshold (V_{TH}).

In flyback mode, the off-state voltage can be calculated with Equation (8):

$$V_{MOSFET} = V_{IN} + N \times V_{OUT} \quad (8)$$

To avoid a voltage spike when the power MOSFET turns off, $V_{DS(MAX)}$ should exceed 1.5 times the V_{MOSFET}.

In forward mode, the off-state voltage across the MOSFET can be calculated with Equation (9):

$$V_{MOSFET} = \frac{D \times V_{IN}}{1 - D} + V_{IN} \quad (9)$$

Where D is the duty cycle with a 70% maximum duty cycle limit.

The maximum current through the power MOSFET occurs once V_{IN} is at its minimum and the output power is at its maximum. The current rating should exceed 1.5 times I_{RMS}.

The MOSFET's on resistance determines the conduction loss. To reduce conduction loss, the on resistance should be as low as possible. Q_G is important for MOSFET selection since it determines the commutation time. A high Q_G

leads to high switching loss, while a low Q_G may cause fast turn-on/off speed, which determines the spike and kick.

The turn-on threshold voltage (V_{TH}) is also important. The GATE pin is powered by VCC, so V_{TH} must be lower than VCC.

Selecting a Transformer for Flyback Application

A transformer is an important component of a flyback converter because it determines the duty cycle, peak current, efficiency, MOSFET value, output diode rating, and more. A good transformer should account for the winding ratio, primary-side inductance, saturation current, leakage inductance, current rating, and core selection.

The transformer winding ratio determines the duty cycle, which can be calculated with Equation (10):

$$D = \frac{N \times V_{OUT}}{N \times V_{OUT} + V_{IN}} \quad (10)$$

Where N is the primary winding transformer to output winding ratio, and D is the duty cycle.

For most applications, it is recommended to have a duty cycle of about 45%.

The primary-side inductance affects the input current ripple ratio factor. A high inductance value results in a large transformer size and high cost. A low inductance value results in a high switching peak current and RMS current, which can decrease efficiency. Choose a primary-side inductor to set the current ripple ratio factor between 30% and 50%. The primary-side inductance can be estimated with Equation (11):

$$L_P = \frac{V_{IN} \times D^2}{2 \times n \times I_{IN} \times f_{SW}} \quad (11)$$

Where *n* is the current ripple ratio, I_{IN} is the input current, and L_P is the primary inductance.

Calculate L_P based on the minimum input voltage condition.

The transformer should have a high saturation current to support the switching peak current; otherwise, the transformer inductance decreases sharply. The SENSE resistor can be used to limit the switching peak current.

The energy stored in the leakage inductance cannot couple to the secondary side, which causes a high spike when the MOSFET turns off. This decreases efficiency and increases MOSFET stress. Normally, the transformer leakage inductance is less than 3% of the transformer inductance.

The current rating counts the maximum RMS current, which allows current to flow through each winding. Uncontrolled current density can cause high resistive power loss.

Setting the Diode Conduct Time (Only for PSR Flyback Mode)

In PSR mode, the MP6005 starts sampling the auxiliary-winding voltage after the primary power MOSFET turns off. A 300ns blanking time helps avoid spike ringing from the leakage inductance. To guarantee a sufficient sample FB period, the output diode's current-conduction time (t_{CON}) should not exceed 600ns under light-load conditions. Design the transformer to ensure t_{CON} exceeds 700ns when V_{SENSE_PK} = 33mV, which can be estimated with Equation (12):

$$\frac{33mV \times L_P \times N_S}{R_{SENSE} \times N_P \times (V_{OUT} + V_{DOF})} \geq 700ns \quad (12)$$

Where V_{DOF} is the output diode's forward-drop voltage.

Resistance Capacitor Diode (RCD) Snubber for Flyback Application

The transformer leakage inductance causes spikes and excessive ringing on the drain voltage waveform. The RCD snubber circuit limits the voltage spike (see Figure 10).

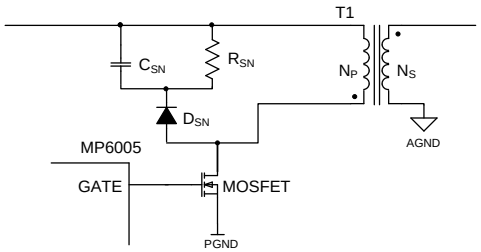


Figure 10: RCD Snubber

The power dissipation of the snubber circuit can be estimated with Equation (13):

$$P_{SN} = \frac{1}{2} \times L_K \times I_{PEAK}^2 \times f_{SW} \quad (13)$$

Where L_K is the leakage inductance, and I_{PEAK} is the peak switching current.

Since R_{SN} consumes the leakage inductance power loss, R_{SN} can be calculated with Equation (14):

$$R_{SN} = \frac{V_{SN}^2}{P_{SN}} \quad (14)$$

Where V_{SN} is the expected snubber voltage on C_{SN}.

The snubber capacitor (C_{SN}) achieves an appropriate voltage ripple on the snubber, which can be calculated with Equation (15):

$$\Delta V_{SN} = \frac{V_{SN}}{R_{SN} \times C_{SN} \times f_{SW}} \quad (15)$$

A 15% ripple is acceptable for most applications.

Selecting an Output Diode for Flyback Applications

The flyback output rectifier diode supplies current to the output capacitor when the primary-side MOSFET is turned off. Use a Schottky diode to reduce power loss due to the diode's forward voltage and recovery time. The diode should have a reverse voltage 1.5 times greater than V_{DIODE}, which can be calculated with Equation (16):

$$V_{DIODE} = \frac{V_{IN}}{N} + V_{OUT} \quad (16)$$

The average current rating must exceed the maximum expected load current, and the peak current rating must exceed the output winding peak current.

It is recommended to use an RC snubber circuit for the output diode.

Selecting a Transformer for Forward Applications

The forward transformer transfers energy to the output. The forward transformer's key parameters are the winding ratio, primary winding turns, current rating, and core selection. The transformer winding ratio determines the duty cycle, which can be calculated with Equation (17):

$$D = \frac{V_{OUT} \times N}{V_{IN}} \quad (17)$$

Where N is the transformer primary winding to output winding ratio.

A 45% duty cycle is recommended for most applications.

When the power MOSFET turns on, the transformer transfers energy to the output, while V_{IN} generates a primary-side inductance current in the transformer. The transformer requires enough primary winding to avoid saturation. The primary-side inductance peak current can be calculated with Equation (18):

$$I_{EXC} = \frac{V_{OUT} \times N}{2 \times L_P \times f_{SW}} \quad (18)$$

Where I_{EXC} is the primary-side inductance peak current, and L_P is the primary inductance.

Using I_{EXC} to calculate the primary winding and enough margins is needed for some extreme conditions, such as load transient or OCP.

The current rating depends on the maximum RMS current, which flows through each winding. A controlled current density is necessary to avoid high resistive power loss.

Selecting a SYNC MOSFET for Forward Applications

The MP6005 supports active clamp forward applications. The active P-channel MOSFET clamp should be equal to the main power MOSFET's maximum voltage, and its maximum current should exceed the primary-side inductance peak current and RMS current.

Selecting an Output MOSFET for Forward Applications

The forward output requires two diodes to conduct current. If higher efficiency is required, the MOSFETs can replace the diodes (see Figure 11).

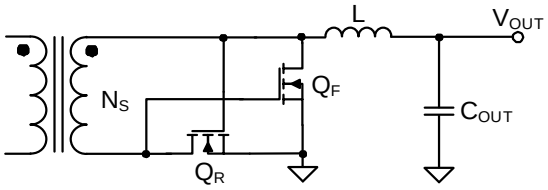


Figure 11: Forward Output MOSFET

The MOSFET voltage rating should exceed the V_{DS} maximum. The Q_R maximum V_{DS} voltage (V_R) can be calculated with Equation (19):

$$V_R = \frac{D \times V_{IN}}{N \times (1 - D)} \quad (19)$$

The Q_F maximum V_{DS} voltage (V_F) can be calculated with Equation (20):

$$V_F = \frac{V_{IN}}{N} \quad (20)$$

Where N is the transformer primary winding to output winding ratio, and D is the primary duty cycle. Some margin is typically necessary.

The MOSFET current rating should exceed its maximum RMS current and peak current. The Q_R RMS current (I_R) can be calculated with Equation (21):

$$I_R = I_{OUT} \times \sqrt{D} \times \sqrt{1 + \frac{1}{3} \times (\frac{I_{PP}}{I_{OUT}})^2} \quad (21)$$

The Q_F RMS current (I_F) can be calculated with Equation (22):

$$I_F = I_{OUT} \times \sqrt{1 - D} \times \sqrt{1 + \frac{1}{3} \times (\frac{I_{PP}}{I_{OUT}})^2} \quad (22)$$

Where I_{PP} is the peak-to-peak current.

Since one MOSFET's drain is the other MOSFET's gate, the Q_R gate driver voltage is equal to V_F, and the Q_F gate driver voltage is equal to V_R. If the driver voltage exceeds the maximum GATE voltage, a clamp circuit is required. The turn-on resistance determines the conduction loss, and Q_G determines the circuit driver loss. Both the turn-on resistance and Q_G should remain low to achieve high efficiency and low temperature rise.

Selecting an Output Inductor for Forward Applications

The forward output inductor supplies constant current to the output load while the main power MOSFET turns on. A larger-value inductor results in less ripple current and a lower output voltage ripple. However, larger-value inductors are larger in size, and have a higher series resistance and lower current saturation. To determine the inductance, allow the peak-to-peak ripple current in the inductor to be approximately 30% to 50% of the maximum output current. The inductance value can be calculated with Equation (23):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT} \times N}{V_{IN}}) \quad (23)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_{SW} is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that does not saturate under the maximum inductor peak current.

Selecting an Input Capacitor

An input capacitor is required to supply the AC ripple current to the inductor while limiting noise at the input source. A low-ESR capacitor is required to minimize noise. It is recommended to use ceramic capacitors, but tantalum or low-ESR electrolytic capacitors can also be used. For ceramic capacitors, the capacitance dominates the input ripple at the switching frequency.

In flyback mode, the input ripple can be estimated with Equation (24):

$$\Delta V_{IN} = I_{IN} \times \frac{V_{IN}}{f_{SW} \times C_{IN} \times (N \times V_{OUT} + V_{IN})} \quad (24)$$

Where ΔV_{IN} is the input voltage ripple, I_{IN} is the input current, and C_{IN} is the input capacitor.

In forward mode, the input ripple can be estimated with Equation (25):

$$\Delta V_{IN} = \frac{I_{IN}}{f_{SW} \times C_{IN}} \times (1 - \frac{V_{OUT} \times N}{V_{IN}}) \quad (25)$$

Equation (25) omits the primary-side inductance current that makes the current ripple smaller.

Selecting an Output Capacitor

The output capacitor maintains the DC output voltage. For the best results, it is recommended to use ceramic capacitors or low-ESR capacitors to minimize the output voltage ripple. For ceramic capacitors, the capacitance dominates the output ripple at the switching frequency.

In flyback mode, the output ripple can be estimated with Equation (26):

$$\Delta V_{OUT} = \frac{N \times V_{OUT}}{(V_{IN} + N \times V_{OUT}) \times f_{SW}} \times \frac{I_{OUT}}{C_{OUT}} \quad (26)$$

If the voltage ripple is too high, place two capacitors on either side of the inductor to

create a Pi (π) filter. This is known as a Pi (π) filter. Choose an inductor between 0.1μH and 0.47μH to achieve sufficient V_{OUT} ripple and system stability.

In forward mode, the output ripple can be estimated with Equation (27):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT} \times N}{V_{IN}}) \quad (27)$$

Design Example

Table 3 shows an example of PSR flyback topology design.

Table 3: PSR Flyback Design Example

V_{IN}	36V to 57V
V_{OUT}	12V
I_{OUT}	2.5A

Figure 15 shows a detailed schematic of a typical PSR flyback application circuit (see the Typical Performance Characteristics section on page 11 for more details). For more detailed device applications, refer to the corresponding evaluation board datasheet.

Table 4 shows an example of SSR forward topology design.

Table 4: SSR Forward Design Example

V_{IN}	36V to 57V
V_{OUT}	5V
I_{OUT}	4.8A

Figure 16 shows a detailed schematic of a typical SSR forward application circuit. For more detailed device applications, refer to the corresponding evaluation board datasheet.

PCB Layout Guidelines

Efficient layout is critical for stable operation. Poor layout may result in reduced performance, excessive EMI, resistive loss, and system instability. For the best results, see Figure 12, Figure 13, and Figure 14, and follow the guidelines below:

For Flyback Applications:

1. For minimal noise and ringing, keep the input loop as short as possible between the input capacitor, transformer, MOSFET, sense resistor, and GND plane.
2. Keep the output loop between the rectifier diode, output capacitor, and transformer as short as possible.
3. Make the clamp loop circuit between D2, C5, and the transformer as small as possible.
4. For the best decoupling, place the VCC capacitor as close to the VCC pin as possible.
5. Place the feedback trace far away from any noise sources, such as the SW pin.
6. Place the COMP components as close to the COMP pin as possible.
7. Use a single-point connector between power GND and signal GND.

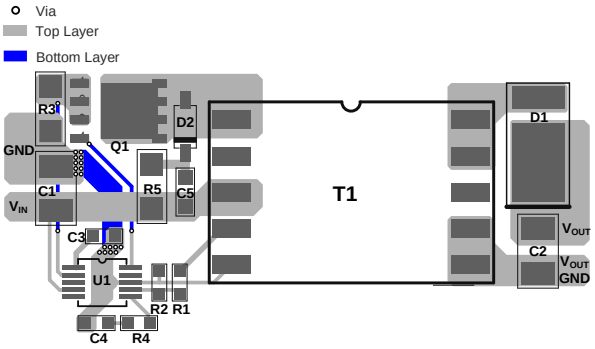


Figure 12: Recommended PCB Layout for Flyback Application (14)

Note:

14) The recommended PCB layout for flyback applications is based on the flyback schematic on page 1.

For Forward Applications:

1. For minimal noise and ringing, keep the input loop between the input capacitor, transformer (Q1), and sense resistor as short as possible.
2. Additionally, for minimal noise and ringing, make the output high-frequency current loop between D1 and D2 transformers as short as possible.
3. For the best decoupling, place the VCC capacitor close to the VCC pin.
4. Place the V_{COMP} trace far away from any noise sources, such as SW.
5. Use a single-point connection between power GND and signal GND.

For more detailed information, refer to the corresponding evaluation board datasheet.

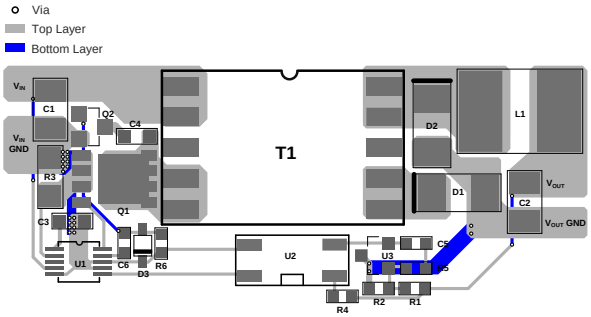


Figure 13: Recommended PCB Layout for Forward Application

Figure 14 shows a typical forward layout schematic.

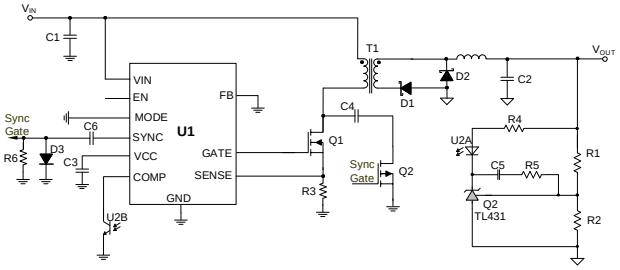


Figure 14: Typical Forward Application Layout Schematic

TYPICAL APPLICATION CIRCUITS

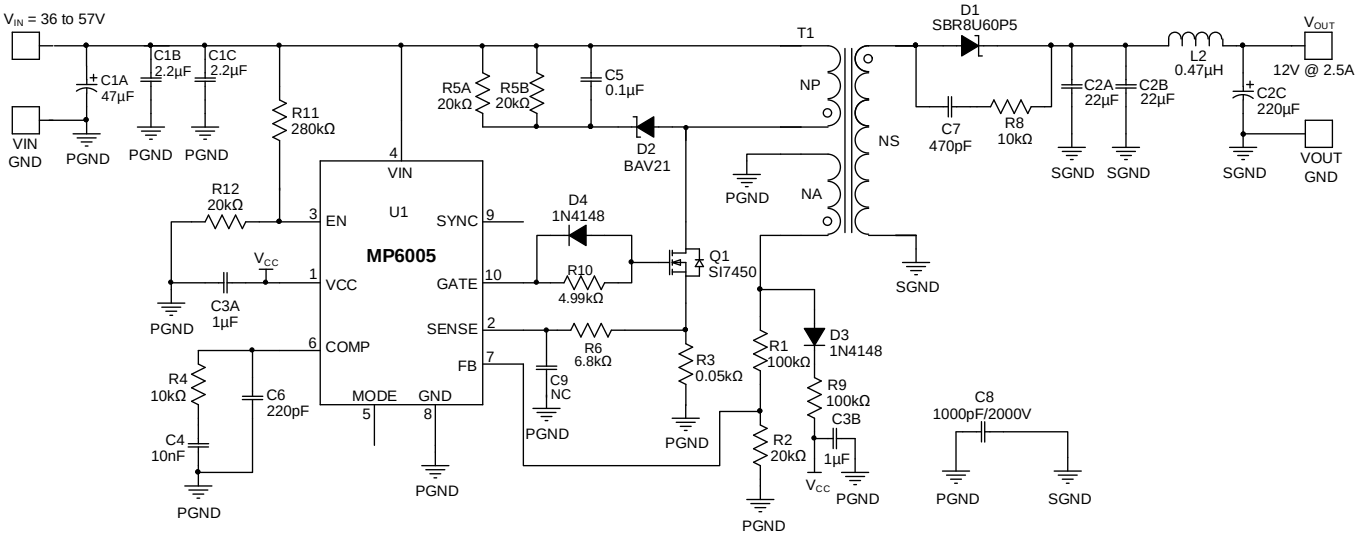


Figure 15: Typical PSR Flyback Application Circuit (15)

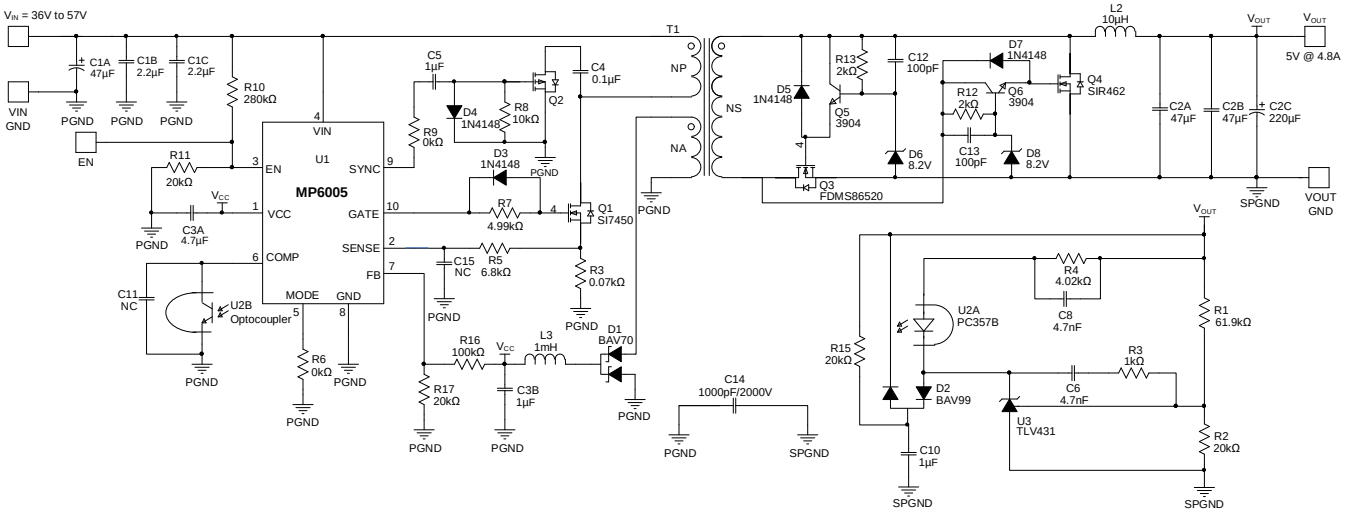


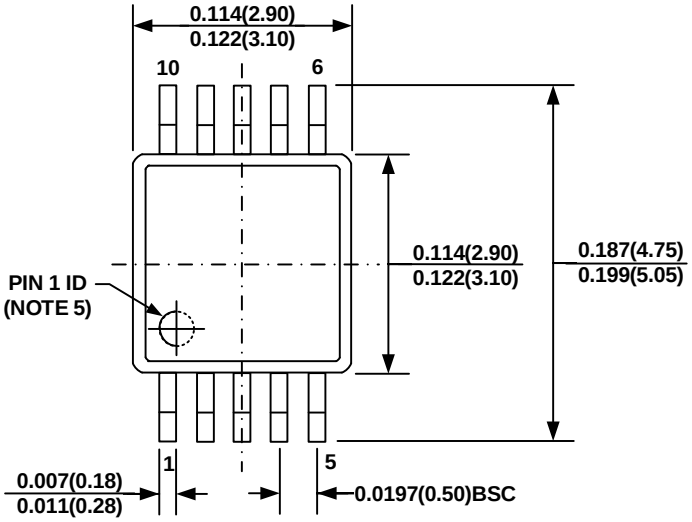
Figure 16: Typical SSR Forward Application Circuit (16)

Notes:

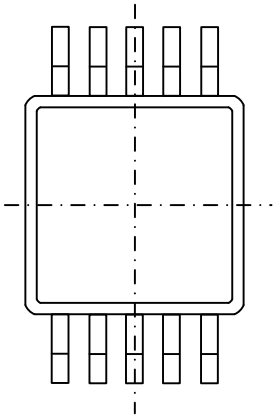
15) V_{IN} = 36V to 57V, V_{OUT} = 12V, I_{OUT} = 2.5A.
16) V_{IN} = 36V to 57V, V_{OUT} = 5V, I_{OUT} = 4.8A.

PACKAGE INFORMATION

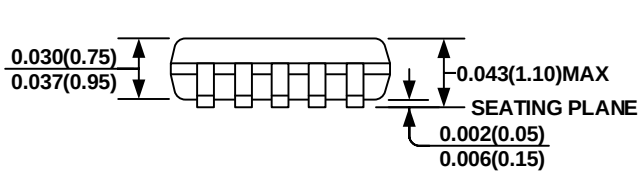
MSOP10



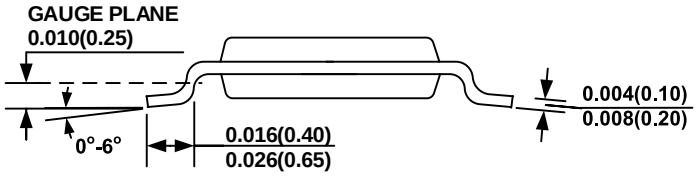
TOP VIEW



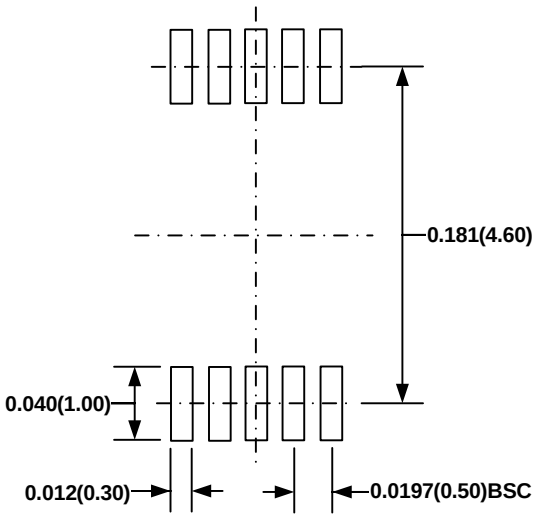
BOTTOM VIEW



FRONT VIEW



SIDE VIEW

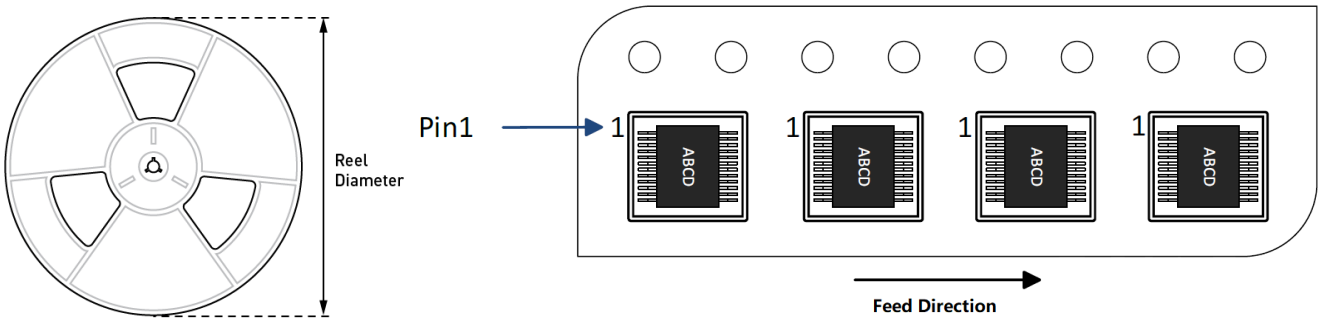


RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS THE HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-817, VARIATION BA.
7) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6005GK– Z	MSOP10	2500	50	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/5/2021	Initial Release	-

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