

DESCRIPTION

The MP62055 Power Distribution Switch features internal current limiting to prevent damage to host devices due to faulty load conditions. The MP62055 analog switch features 115mΩ on-resistance and operates from 2.7V to 5.5V input. It is available with a guaranteed current limit, making it ideal for load switching applications. The MP62055 has built-in protection for both over current and increased thermal stress. For over current, the device will limit the current by changing to a constant current mode.

As the temperature increases as a result of short circuit, the device will shut off. The device will recover once the device temperature reduces to approx 120°C.

The MP62055 is available in a TSOT23-5 package.

FEATURES

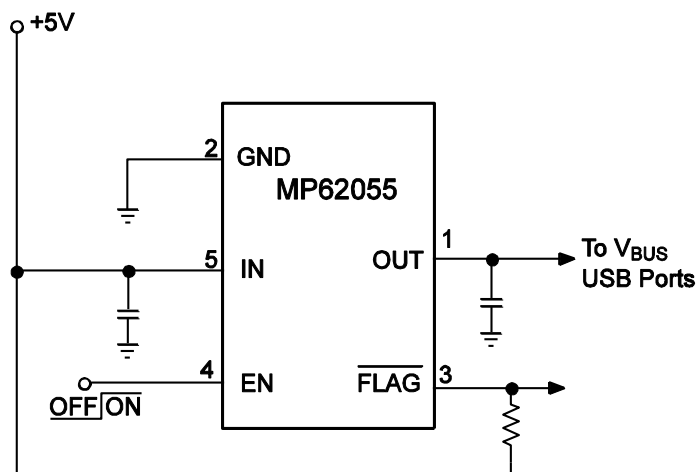
- 500mA Continuous Current
- Accurate Current Limit
- 2.7V to 5.5V Supply Range
- 90uA Quiescent Current
- 115mΩ MOSFET
- Thermal-Shutdown Protection
- Under-Voltage Lockout
- 8ms FLAG Deglitch Time
- No FLAG Glitch During Power Up
- Reverse Current Blocking
- TSOT23-5 Package
- UL File # E322138

APPLICATIONS

- Smartphone and PDA
- Portable GPS Device
- Set-top-box
- USB Power Distribution

All MPS parts are lead-free, halogen free, and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology" are Registered Trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION



SINGLE-CHANNEL



UL Recognized Component

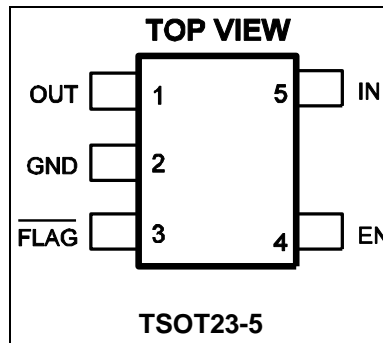
ORDINARY INFORMATION

Part Number	Enable	Switch	Maximum Continuous Load Current	Typical Short-Circuit Current @ T _A =25°C	Package	Top Marking	Free Air Temperature (T _A)
MP62055EJ	Active High	Single	500mA	1100mA	TSOT23-5	6G	-40°C to +85°C

* For Tape & Reel, add suffix -Z (e.g. MP62055EJ-Z).

For RoHS Compliant Packaging, add suffix -LF (e.g. MP62055EJ-LF-Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

IN	-0.3V to +6V
EN, FLAG, OUT to GND	-0.3V to +6V
Continuous Power Dissipation (T _A = +25°C) ⁽²⁾	0.56W
Junction Temperature	150°C
Lead Temperature	260°C
Storage Temperature	-65°C to +150°C
Operating Junct. Temp (T _J)	-40°C to +125°C

Thermal Resistance ⁽³⁾	θ_{JA}	θ_{JC}
TSOT23-5	220	110

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA} . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage
- Measured on JESD51-7 4-layer PCB.

ELECTRICAL CHARACTERISTICS ⁽⁴⁾
 $V_{IN}=5V$, $T_A=+25^{\circ}C$, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Units
IN Voltage Range		2.7		5.5	V
Supply Current	Single Channel		90	120	μA
Shutdown Current	Device Disable, $V_{OUT}=\text{float}$, $V_{IN}=5.5V$		1		μA
Off Switch Leakage	Device Disable, $V_{IN}=5.5V$		1		μA
Current Limit		550		1100	mA
Trip Current	Current Ramp (slew rate $\leq 100A/s$) on Output		1	1.4	A
Under-voltage Lockout	Rising Edge	1.95		2.65	V
Under-voltage Hysteresis			250		mV
FET On Resistance	$I_{OUT}=100mA$, and $-40^{\circ}C < T_A < 85^{\circ}C$		115	168	m Ω
EN Input Logic High Voltage		2			V
EN Input Logic Low Voltage				0.8	V
FLAG Output Logic Low Voltage	$I_{SINK}=5mA$			0.4	V
FLAG Output High Leakage Current	$V_{IN}=V_{FLAG}=5.5V$			1	μA
Thermal Shutdown			140		$^{\circ}C$
Thermal Shutdown Hysteresis			20		$^{\circ}C$
V_{OUT} Rising Time, T_r ⁽⁵⁾	$V_{IN}=5.5V$, $C_L=1\mu F$, $R_L=11\Omega$		0.9		ms
	$V_{IN}=2.7V$, $C_L=1\mu F$, $R_L=11\Omega$		1.7		ms
V_{OUT} Falling Time, T_f ⁽⁵⁾	$V_{IN}=5.5V$, $C_L=1\mu F$, $R_L=11\Omega$			0.5	ms
	$V_{IN}=2.7V$, $C_L=1\mu F$, $R_L=11\Omega$			0.5	ms
Turn On Time, T_{on} ⁽⁶⁾	$C_L=100\mu F$, $R_L=11\Omega$			3	ms
Turn Off Time, T_{off} ⁽⁶⁾	$C_L=100\mu F$, $R_L=11\Omega$			10	ms
FLAG Deglitch Time		4	8	15	ms
EN Input Leakage			1		μA
Reverse Leakage Current	$OUT=5.5V$, $IN=GND$		0.2		μA

NOTE:

 4) Production test at $+25^{\circ}C$. Specifications over the temperature range are guaranteed by design and characterization.

5) Measured from 10% to 90%.

6) Measured from (50%) EN signal to (90%) output signal.

PIN FUNCTIONS

Pin #	Name	Description
1	OUT	Power-Distribution Switch Output.
2	GND	Ground
3	$\overline{\text{FLAG}}$	IN-to-OUT Over-current, active-low output flag. Open-Drain.
4	EN	Enable Input. Active High.
5	IN	Input Voltage. Accepts 2.7V to 5.5V input.

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = +25^\circ\text{C}$, unless otherwise noted.

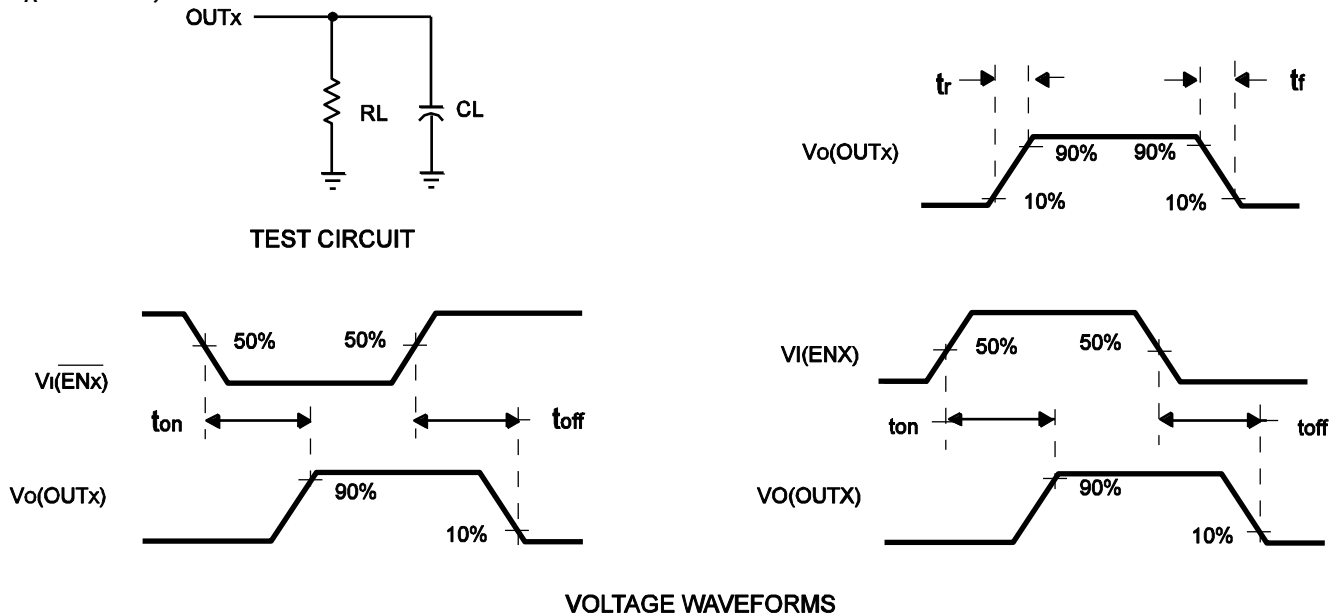


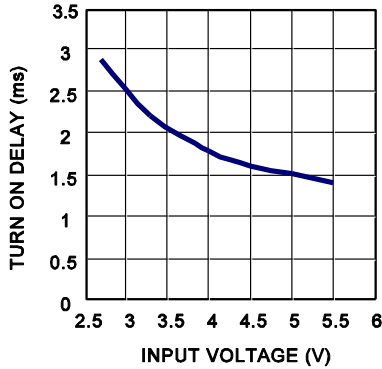
Figure 1—Test Circuit and Voltage Waveforms

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}=5.5V$, $C_L = 2.2\mu F$, $T_A = +25^\circ C$, unless otherwise noted.

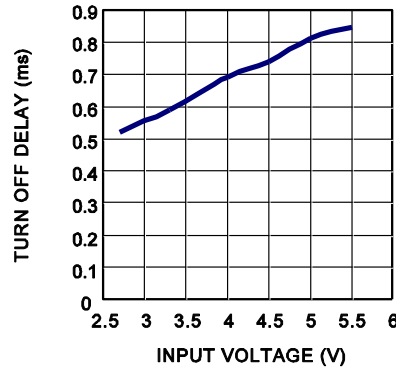
Turn on Delay vs. Input Voltage

$V_{EN}=5V$, $R_L=11\Omega$



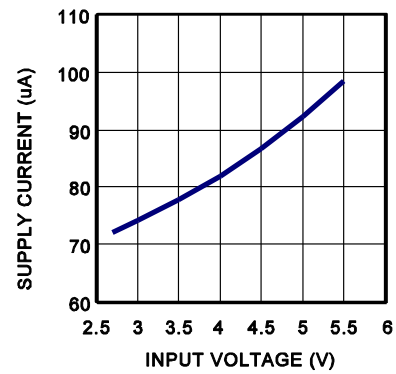
Turn off Delay vs. Input Voltage

$V_{EN}=5V$, $R_L=11\Omega$



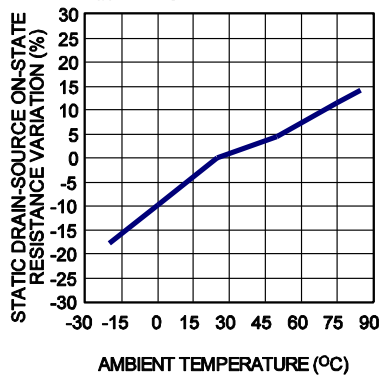
Supply Current, Output Enabled vs. Input Voltage

$V_{EN}=5V$



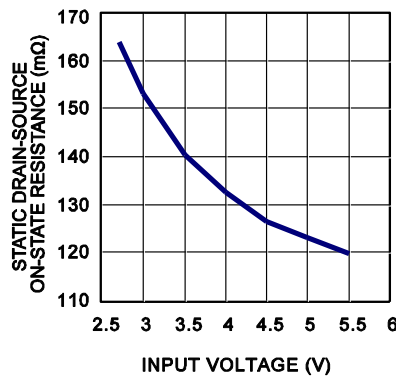
Static Drain-Source On-State Resistance Variation vs. Ambient Temperature

$V_{IN}=5V$, $I_O=0.1A$



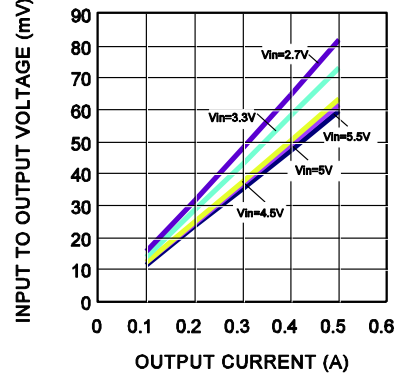
Static Drain-Source On-State Resistance vs. Input Voltage

$V_{EN}=5V$, $I_{OUT}=0.5A$



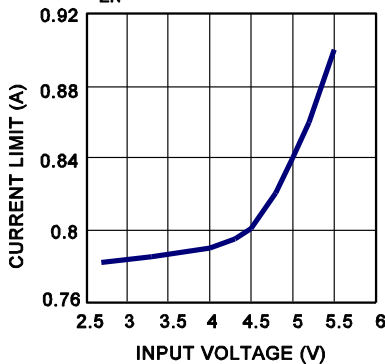
Input to Output Voltage vs. Load Current

$V_{EN}=5V$

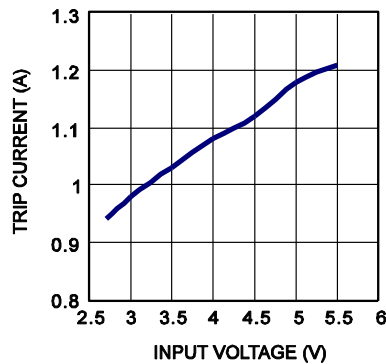


Current Limit vs. Input Voltage

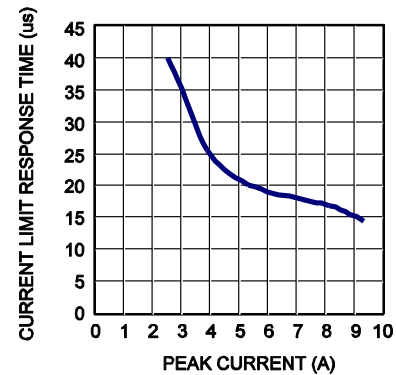
$V_{EN}=5V$



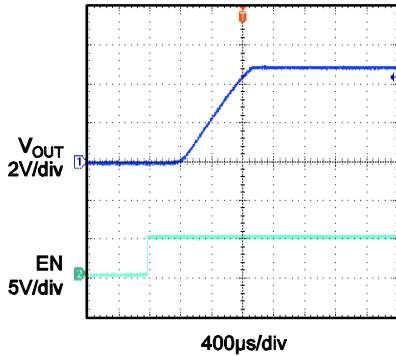
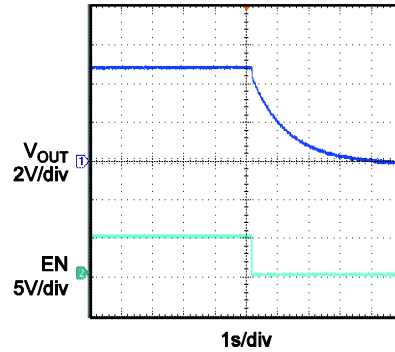
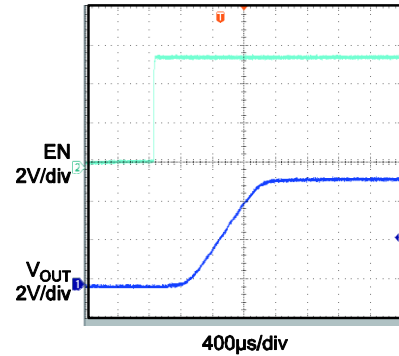
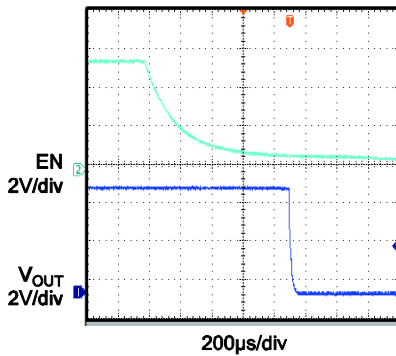
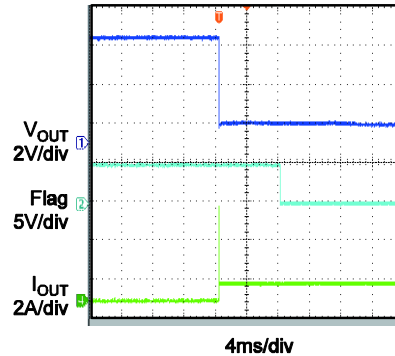
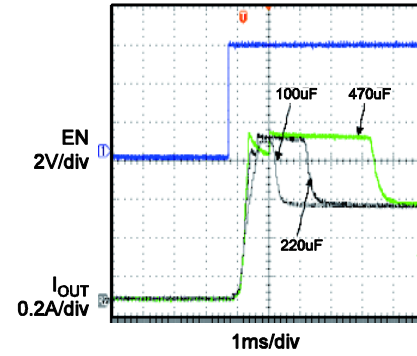
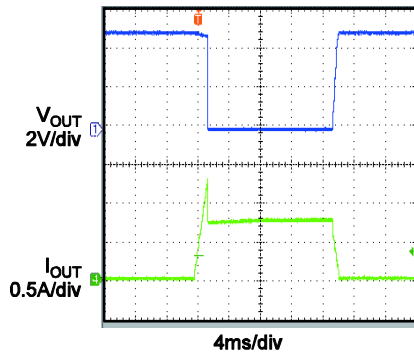
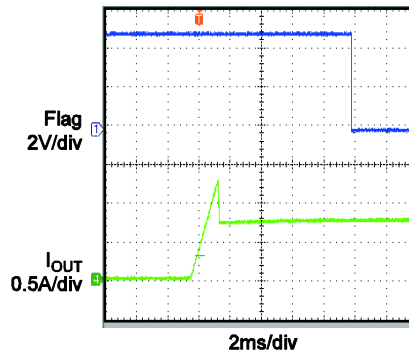
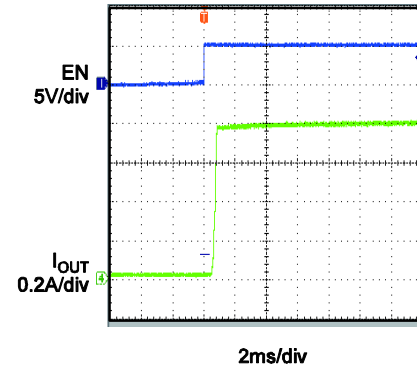
Threshold Trip Current vs. Input Voltage



Current Limit Response Time vs. Peak Current



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*
 $V_{IN}=5.5V$, $C_L = 2.2\mu F$, $T_A = +25^\circ C$, unless otherwise noted.

Turn On Delay and Rise Time with 0.1 μF Load
 $V_{EN}=5V$, $C_L=0.1\mu F$

Turn Off Delay and Fall Time with 0.1 μF Load
 $V_{EN}=5V$, $C_L=0.1\mu F$

Turn On Delay and Rise Time
 $R_L=11\Omega$, $C_L=1\mu F$

Turn Off Delay and Fall Time
 $R_L=11\Omega$, $C_L=1\mu F$

1 Ω Load Connected to Enabled Device

Inrush Current with Different Load Capacitance
 $R_L=11\Omega$, Start up by EN

Threshold Trip Current with Ramped Load on Enabled Device

Ramped Load on Enabled Device

Short Circuit Current, Device Enabled into Short


Thermal Protection

The purpose of thermal protection is to prevent damage in the IC by allowing excessive current to flow and heating the junction. The die temperature is internally monitored until the thermal limit is reached. Once this temperature is reached, the switch will turn off and allow the chip to cool. The switch has a built-in hysteresis.

Under-voltage Lockout (UVLO)

This circuit is used to monitor the input voltage to ensure that the MP62055 is operating correctly. This UVLO circuit also ensures that there is no operation until the input voltage reaches the minimum spec.

Enable

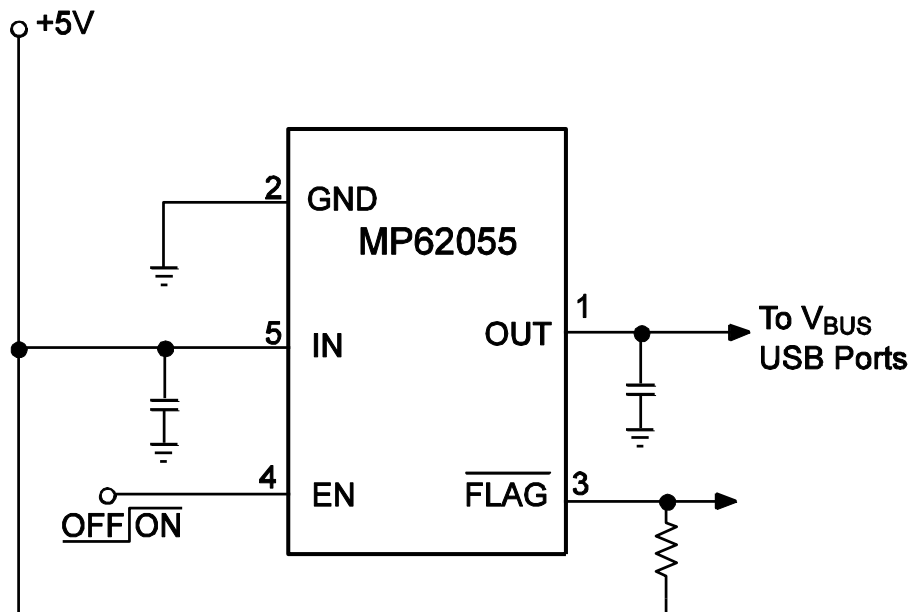
The logic pin disables the chip to reduce the supply current. The device will operate once the enable signal reaches the appropriate level. The input is compatible with both COMS and TTL.

APPLICATION INFORMATION

Power-Supply Considerations

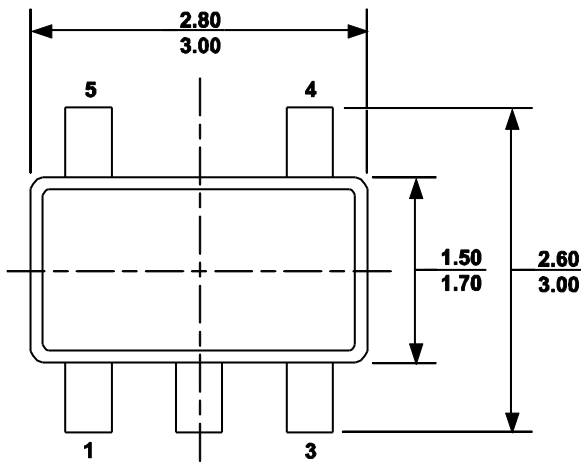
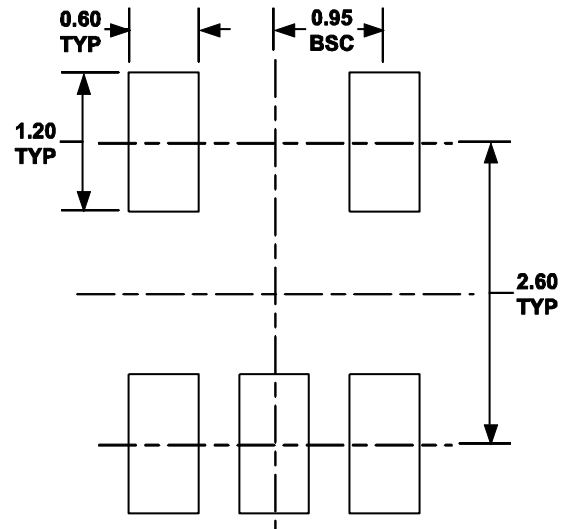
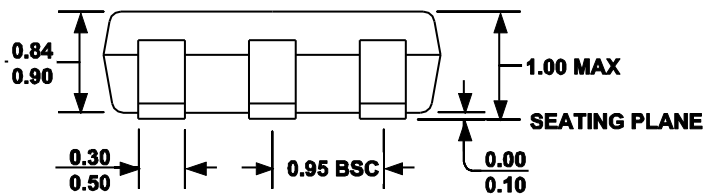
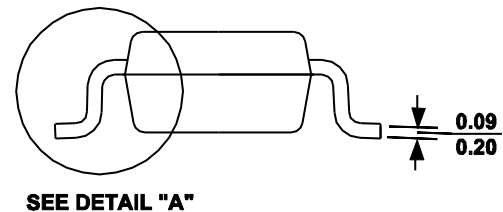
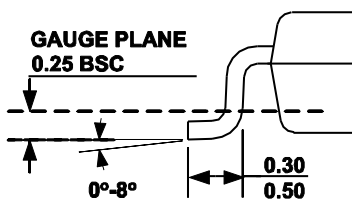
Over 10 μ F capacitor between IN and GND is recommended. This precaution reduces power-supply transients that may cause ringing on the input and improves the immunity of the device to short-circuit transients.

In order to achieve smaller output load transient ripple, placing a high-value electrolytic capacitor on the output pin(s) is recommended when the load is heavy.



SINGLE-CHANNEL

Figure 3—Application Circuit

PACKAGE INFORMATION
TSOT23-5

TOP VIEW

RECOMMENDED LAND PATTERN

FRONT VIEW

SEE DETAIL "A"
SIDE VIEW

DETAIL "A"
NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for [Power Switch ICs - Power Distribution](#) *category:*

Click to view products by [Monolithic Power Systems](#) *manufacturer:*

Other Similar products are found below :

[TCK111G,LF\(S\)](#) [FPF1018](#) [DS1222](#) [TCK2065G,LF](#) [SZNCP3712ASNT3G](#) [MIC2033-05BYMT-T5](#) [MIC2033-12AYMT-T5](#) [MIC2033-05BYM6-T5](#) [SLG5NT1437VTR](#) [SZNCP3712ASNT1G](#) [DML1008LDS-7](#) [KTS1670EDA-TR](#) [KTS1640QGDV-TR](#) [KTS1641QGDV-TR](#) [FPF2260ATMX](#) [U6513A](#) [MIC2012YM-TR](#) [TPS2104DBVR](#) [TPS22958NDGKR](#) [MIC2098-1YMT-TR](#) [MIC94062YMT TR](#) [MP6231DN-LF](#) [MIC2015-1.2YM6 TR](#) [MIC2075-2YM](#) [MIC94068YML-TR](#) [SIP32461DB-T2-GE1](#) [NCP335FCT2G](#) [TCK105G,LF\(S\)](#) [AP2411S-13](#) [AP2151DSG-13](#) [AP2172MPG-13](#) [MIC94094YC6-TR](#) [MIC94093YC6-TR](#) [MIC94064YC6-TR](#) [MIC2505-1YM](#) [MIC94305YMT-TR](#) [MIC94085YFT-TR](#) [MIC94081YFT-TR](#) [MIC94042YFL-TR](#) [MIC94041YFL-TR](#) [MIC2005-1.2YM6-TR](#) [TPS2032QDRQ1](#) [NCP333FCT2G](#) [BTS3050TFATMA1](#) [NCP331SNT1G](#) [TPS2092DR](#) [TPS2063DR](#) [VNV35N07-E](#) [MIC2008YML-TR](#) [MIC2040-1YMM](#)