# MP6540, MP6540A

## 35V, 3A, Three-Phase Power Stage

## DESCRIPTION

The MP6540 and MP6540A are 3-phase, brushless DC motor drivers that integrate three half-bridges consisting of six N-channel power MOSFETs, pre-drivers, gate drive power supplies, and current sense amplifiers.

The MP6540 has enable and PWM inputs for each half-bridge. The MP6540A has separate high-side and low-side inputs; otherwise, both parts are identical. References to the MP6540 in this document also apply to the MP6540A unless otherwise noted.

The MP6540 can deliver up to 10A of peak current for one second and 3A continuously (depending on thermal and PCB conditions). The MP6540 uses an internal charge pump to generate the gate drive supply voltage for the high-side MOSFETs and a trickle charge circuit that maintains sufficient gate drive voltage to operate at 100% duty cycle.

Internal safety features include thermal shutdown, under-voltage lockout (UVLO), and over-current protection (OCP).

The MP6540 is available in a QFN-26 (5.0mmx5.0mm) package.

## FEATURES

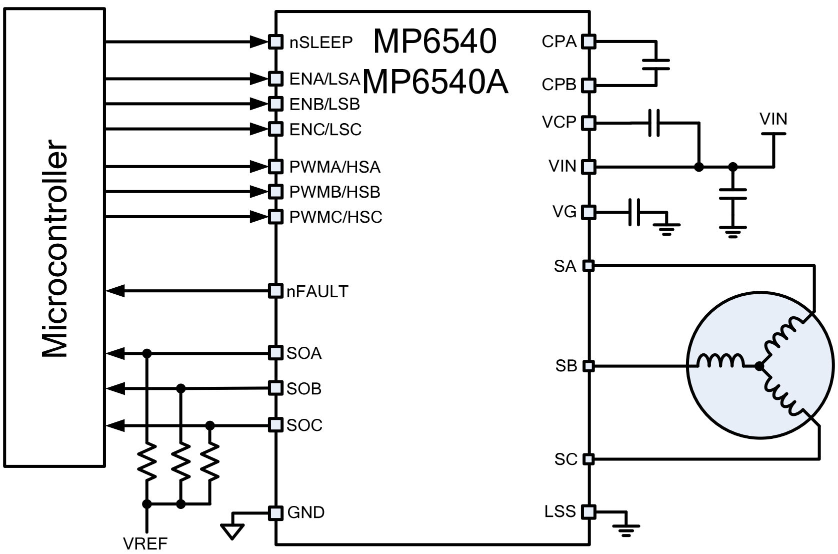
- 5.5V to 35V Operating Supply Voltage
- Three Integrated Half-Bridge Drivers
- 3A Output Current, 10A Peak Current
- MOSFET On Resistance: HS + LS 50mΩ
- MP6540: PWM and Enable Inputs
  MP6540A: HS and LS Inputs
- Internal Charge Pump Supports 100% Duty Cycle Operation
- Automatic Synchronous Rectification
- UVLO and Thermal Shutdown Protection
- Over-Current Protection (OCP)
- Integrated Bidirectional Current Sense Amplifiers
- Available in an FCQFN-26 (5mmx5mm) Package

## APPLICATIONS

- Brushless DC Motors
- Permanent Magnet Synchronous Motors



## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number | Package | Top Marking |
|---|---|---|
| MP6540GU* | QFN-26 (5mmx5mm) | *See Below* |
| MP6540AGU** | QFN-26 (5mmx5mm) | *See Below* |

* For Tape & Reel, add suffix –Z (e.g.: MP6540GU–Z).
** For Tape & Reel, add suffix –Z (e.g.: MP6540AGU–Z).

## TOP MARKING (MP6540GU)

MPSYYWW
MP6540
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP6540: Part number
LLLLLLL: Lot number

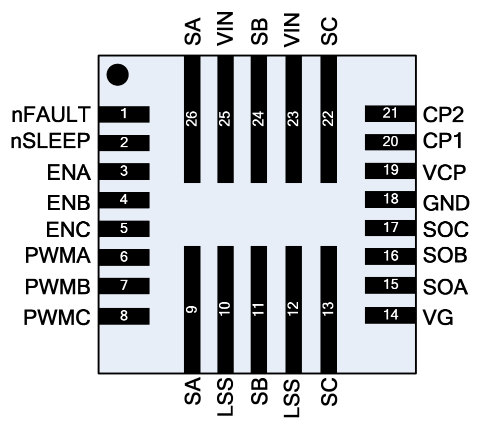
## TOP MARKING (MP6540AGU)

MPSYYWW
MP6540A
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
M6540A: Part number
LLLLLLL: Lot number

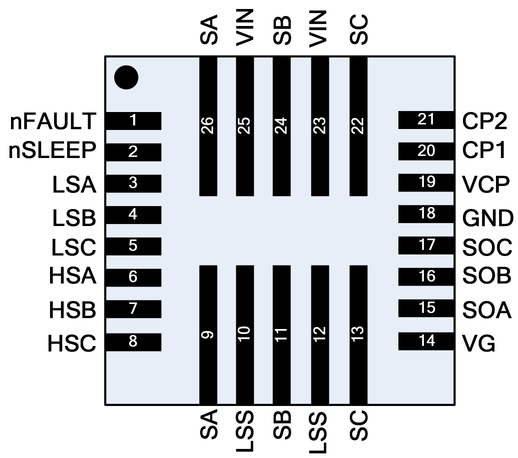
## PACKAGE REFERENCE

**TOP VIEW**




**MP6540**

**TOP VIEW**




**MP6540A**

**QFN-26 (5mmx5mm)**

## PIN FUNCTIONS

| QFN-26 Pin # | MP6540 | MP6540A | Description |
|---|---|---|---|
| 1 | nFAULT | | **Fault indication.** nFAULT is an open-drain output type. nFAULT is in logic low during fault conditions. |
| 2 | nSLEEP | | **Sleep mode input.** Drive nSLEEP to logic low to enter low-power sleep mode. Drive nSLEEP to logic high for normal operation. nSLEEP is pulled down internally. |
| 3 | ENA | - | **Enable pin for phase A.** |
| | - | LSA | **Enable low-side MOSFET for phase A.** |
| 4 | ENB | - | **Enable pin for phase B.** |
| | - | LSB | **Enable low-side MOSFET for phase B.** |
| 5 | ENC | - | **Enable pin for phase C.** |
| | - | LSC | **Enable low-side MOSFET for phase C.** |
| 6 | PWMA | - | **PWM input pin for phase A.** |
| | - | HSA | **Enable high-side MOSFET for phase A.** |
| 7 | PWMB | - | **PWM input pin for phase B.** |
| | - | HSB | **Enable high-side MOSFET for phase B.** |
| 8 | PWMC | - | **PWM input pin for phase C.** |
| | | HSC | **Enable high-side MOSFET for phase C.** |
| 9, 26 | SA | | **Phase A output.** |
| 10, 12 | LSS | | **Low-side source connection for phase A, B, and C.** LSS must be connected to GND directly. |
| 11, 24 | SB | | **Phase B output.** |
| 13, 22 | SC | | **Phase C output.** |
| 14 | VG | | **Low-side gate drive voltage bypass.** Connect a 4.7µF, 10V, X7R ceramic capacitor from VG to ground. |
| 15 | SOA | | **Current sense output for phase A.** |
| 16 | SOB | | **Current sense output for phase B.** |
| 17 | SOC | | **Current sense output for phase C.** |
| 18 | GND | | **Ground.** |
| 19 | VCP | | **Charge pump output.** Connect a 1µF, 16V, X7R ceramic capacitor from VCP to VIN. |
| 20 | CP1 | | **Charge pump capacitor pins.** Connect a 100nF, X7R ceramic capacitor rated for at least VIN between CP1 and CP2. |
| 21 | CP2 | | |
| 23, 25 | VIN | | **Input power.** |

## ABSOLUTE MAXIMUM RATINGS (1)

Input voltage ($V_{IN}$) ........................... -0.3V to 40V
CP2, VCP ........................................ -0.3V to 40V
CP1 ................................................. -0.3V to 15V
SA/B/C ............................................ -0.3V to 40V
ESD rating (HBD)......................................... 2kV
All other pins to GND ..................... -0.3V to 6.5V
Continuous power dissipation ($T_A$ = +25°C) (2)
QFN-26 (5mmx5mm)................................3.47W
Storage temperature .................-55°C to +150°C
Junction temperature .............................. +150°C
Lead temperature (solder) ...................... +260°C

### *Recommended Operating Conditions* (3)

Input voltage ($V_{IN}$) ............................ 5.5V to 35V
Operating junction temp. ($T_J$)....-40°C to +125°C

### *Thermal Resistance* (4)

| | $\theta_{JA}$ | $\theta_{JC}$ | |
|---|---|---|---|
| QFN-26 (5mmx5mm) | 22.4 | 18.4 | °C/W |

**NOTES:**
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 24V, $T_A$ = 25°C, LSS = GND = 0V, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| Input supply voltage | $V_{IN}$ | | 5.5 | | 35 | V |
| Quiescent current | $I_Q$ | nSLEEP = 1, ENx = 0 | | 0.8 | 1.3 | mA |
| | $I_{SLEEP}$ | nSLEEP = 0 | | 0.75 | 3.5 | µA |
| Operation current | | nSLEEP = 1, ENx = 1, PWMx = 20kHz | | 4 | 5.5 | mA |
| | | nSLEEP = 1, ENx = 1, PWMx = 50kHz | | 8 | 9.5 | mA |
| | | nSLEEP = 1, ENx = 1, PWMx = 100kHz | | 14 | 16.5 | mA |
| | | nSLEEP = 1, ENx = 1, PWMx = 200kHz | | 25 | 29.5 | mA |
| **Control Logic** | | | | | | |
| Input logic low threshold | $V_{IL}$ | | 0.8 | | 1.45 | V |
| Input logic high threshold | $V_{IH}$ | | 1.1 | | 2 | V |
| Logic input current | $I_{IN(H)}$ | V = 5V | | 4.7 | 6 | µA |
| | $I_{IN(L)}$ | V = 0V | -1 | | 1 | µA |
| Power-up delay | $t_{PUD}$ | At $V_{IN}$ rising or nSLEEP rising | 1.4 | | 4.7 | mS |
| Internal pull-down resistance | $R_{PD}$ | All logic inputs | | 1 | | MΩ |
| nFAULT pull-down $R_{ON}$ | $R_{ON(NFAULT)}$ | | | 27 | | Ω |
| **Protection Circuits** | | | | | | |
| UVLO threshold | $V_{UVLO}$ | $V_{IN}$ rising | 4 | | 5.5 | V |
| UVLO hysteresis | $\Delta V_{UVLO}$ | | | 250 | | mV |
| HS OCP threshold | $I_{OCP(HS)}$ | | 10 | 13 | 17 | A |
| LS OCP threshold | $I_{OCP(LS)}$ | | 10 | 13 | 17 | A |
| OCP deglitch time | $t_{OCD}$ | | | 0.4 | | µs |
| OCP retry time | $t_{OCR}$ | | | 10 | | ms |
| Thermal shutdown (5) | $T_{TSD}$ | | | 150 | | °C |
| Thermal shutdown hysteresis (5) | $\Delta T_{TSD}$ | | | 25 | | °C |
| **Current Sense** | | | | | | |
| Current sense ratio | | LS-FET current = ±3A | 1/10580 | 1/9200 | 1/7500 | A/A |
| Current sense output current | | LS-FET current = 1A | 95 | 116 | 135 | µA |
| | | LS-FET current = -1A | 95 | 112 | 135 | µA |
| Current sense output voltage swing | | Sink or source 0.25A into Sx | 0 | | 5.5 | V |
| **Output** | | | | | | |
| HS-FET on resistance | $R_{ON(HS)}$ | $I_{OUT}$ = 1A, $T_J$ = 25°C | | 25 | 29 | mΩ |
| | | $I_{OUT}$ = 1A, $T_J$ = 125°C | | 32 | | mΩ |
| LS-FET on resistance | $R_{ON(LS)}$ | $I_{OUT}$ = 1A, $T_J$ = 25°C | | 20 | 23.5 | mΩ |
| | | $I_{OUT}$ = 1A, $T_J$ = 125°C | | 26 | | mΩ |
| Output rise time | | $I_{OUT}$ = 1A | | 30 | | V/nS |
| Output fall time | | $I_{OUT}$ = 1A | | 18.5 | | V/nS |

## ELECTRICAL CHARACTERISTICS *(continued)*

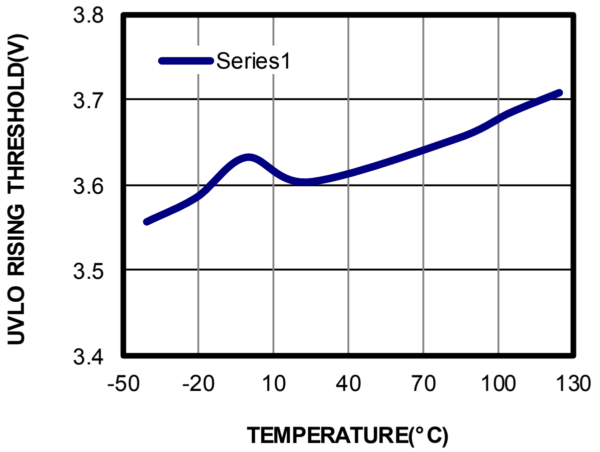
**$V_{IN}$ = 24V, $T_A$ = 25°C, LSS = GND = 0V, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Charge Pump** | | | | | | |
| Charge pump output voltage | $V_{CP}$ | | | $V_{IN}$ + 5.5 | | V |
| $V_{CP}$ switching freq | $f_{CP}$ | | | 193 | | kHz |

**NOTE:**
5) Guaranteed by design.

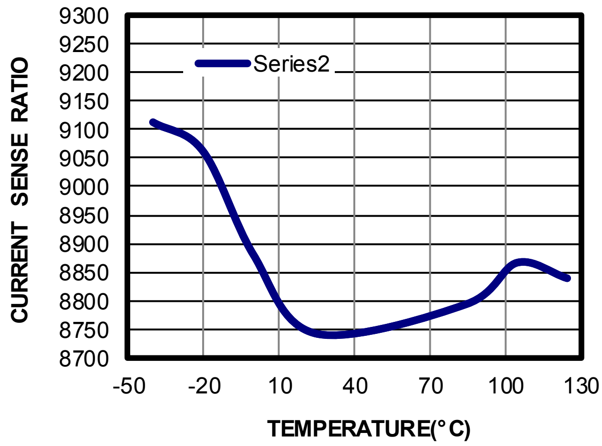
## TYPICAL CHARACTERISTICS

**UVLO Rising Threshold vs. Temperature**



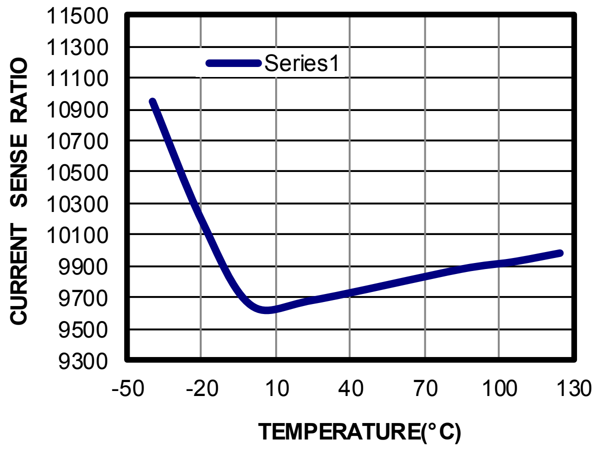

**A Phase Current Sense Ratio vs. Temperature**

$V_{IN}$ = 24V, $I_{OUT}$ = 1A



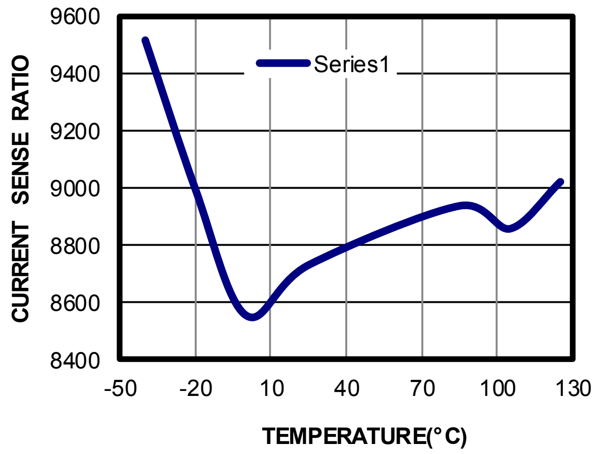

**B Phase Current Sense Ratio vs. Temperature**

$V_{IN}$ = 24V, $I_{OUT}$ = 1A



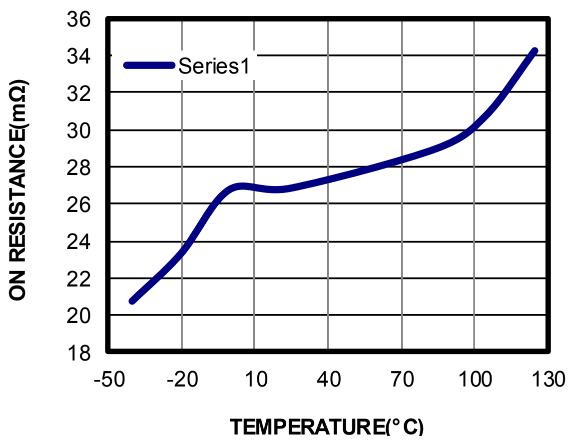

**C Phase Current Sense Ratio vs. Temperature**

$V_{IN}$ = 24V, $I_{OUT}$ = 1A



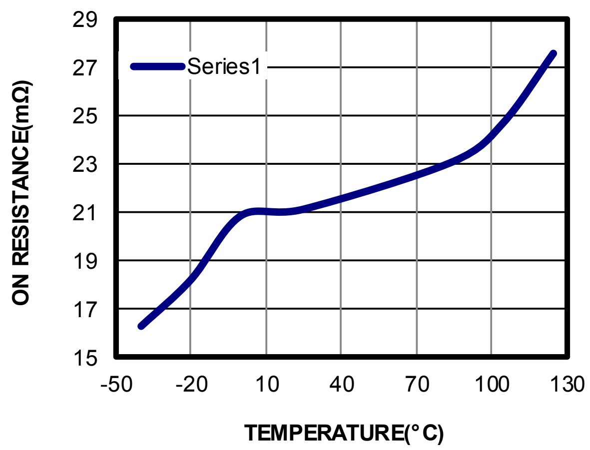

**HS On Resistance vs. Temperature**

$V_{IN}$ = 24V, $I_{OUT}$ = 1A




**LS On Resistance vs. Temperature**

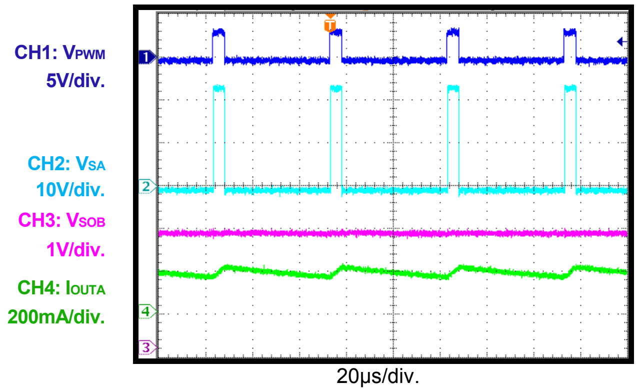
$V_{IN}$ = 24V, $I_{OUT}$ = 1A



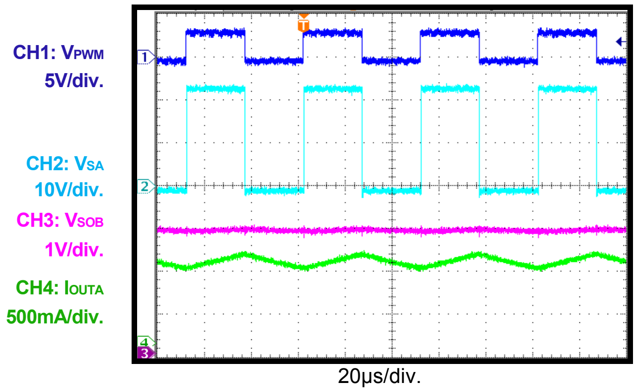
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 24V, A phase switching with 20kHz frequency, B phase LS on, C phase disable, $V_{REF}$ = 5V, current sense resistor divider = 5kΩ, $T_A$ = 25°C, resistor + inductor load: 5Ω + 1mH/phase with star connection, unless otherwise noted.**

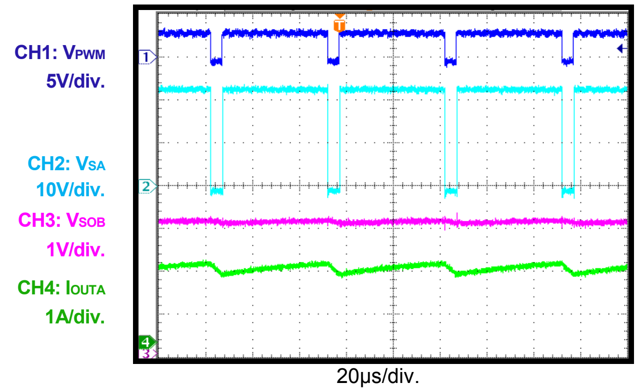
**Steady State**
Duty = 10%



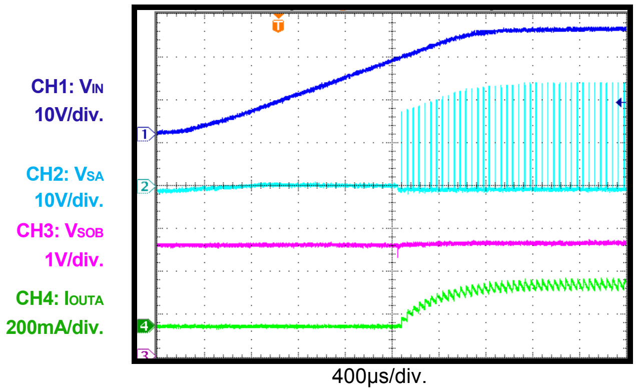

**Steady State**
Duty = 50%



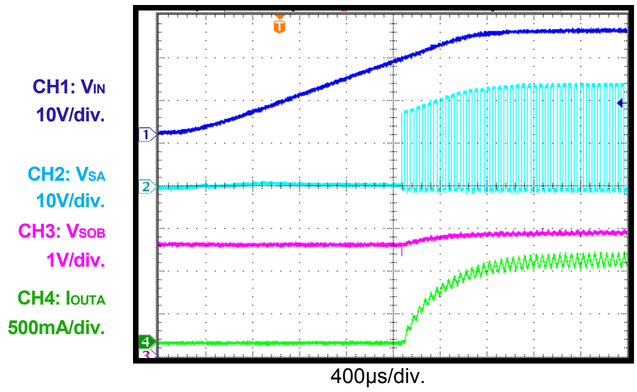

**Steady State**
Duty = 90%



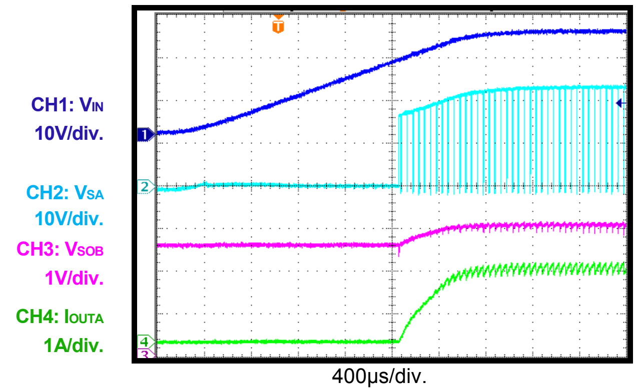

**Power Ramp-Up**
Duty = 10%




**Power Ramp-Up**
Duty = 50%



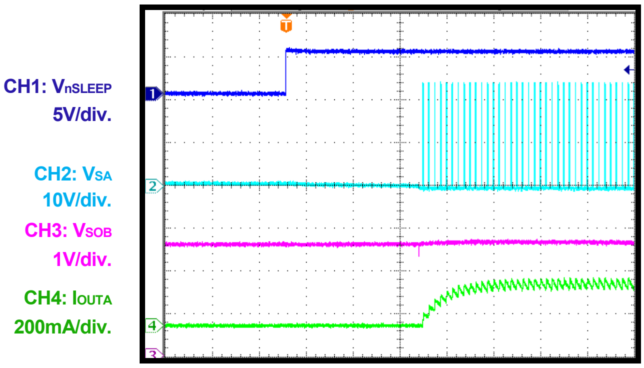

**Power Ramp-Up**
Duty = 90%



## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

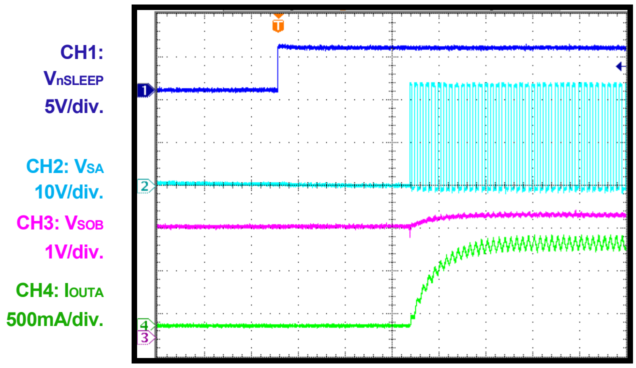
**$V_{IN}$ = 24V, A phase switching with 20kHz frequency, B phase LS on, C phase disable, $V_{REF}$ = 5V, current sense resistor divider = 5kΩ, $T_A$ = 25°C, resistor + inductor load: 5Ω + 1mH/phase with star connection, unless otherwise noted.**

**Sleep Recovery**
Duty = 10%



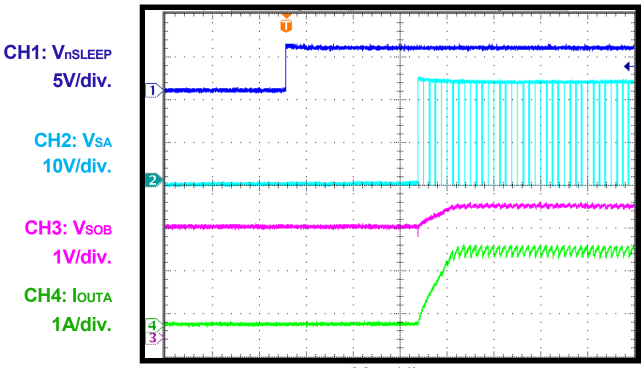

400μs/div.

**Sleep Recovery**
Duty = 50%



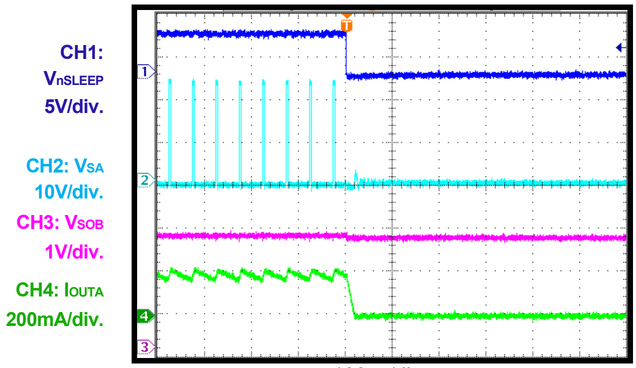

400μs/div.

**Sleep Recovery**
Duty = 90%



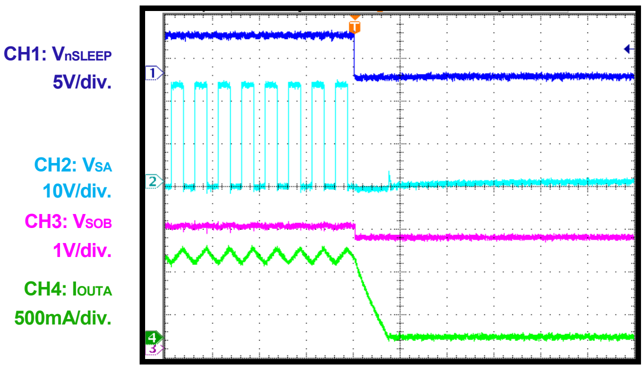

400μs/div.

**Sleep Entry**
Duty = 10%



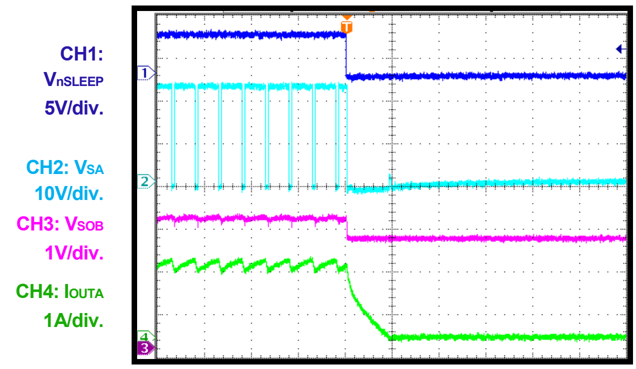

100μs/div.

**Sleep Entry**
Duty = 50%




100μs/div.

**Sleep Entry**
Duty = 90%




100μs/div.

## BLOCK DIAGRAM

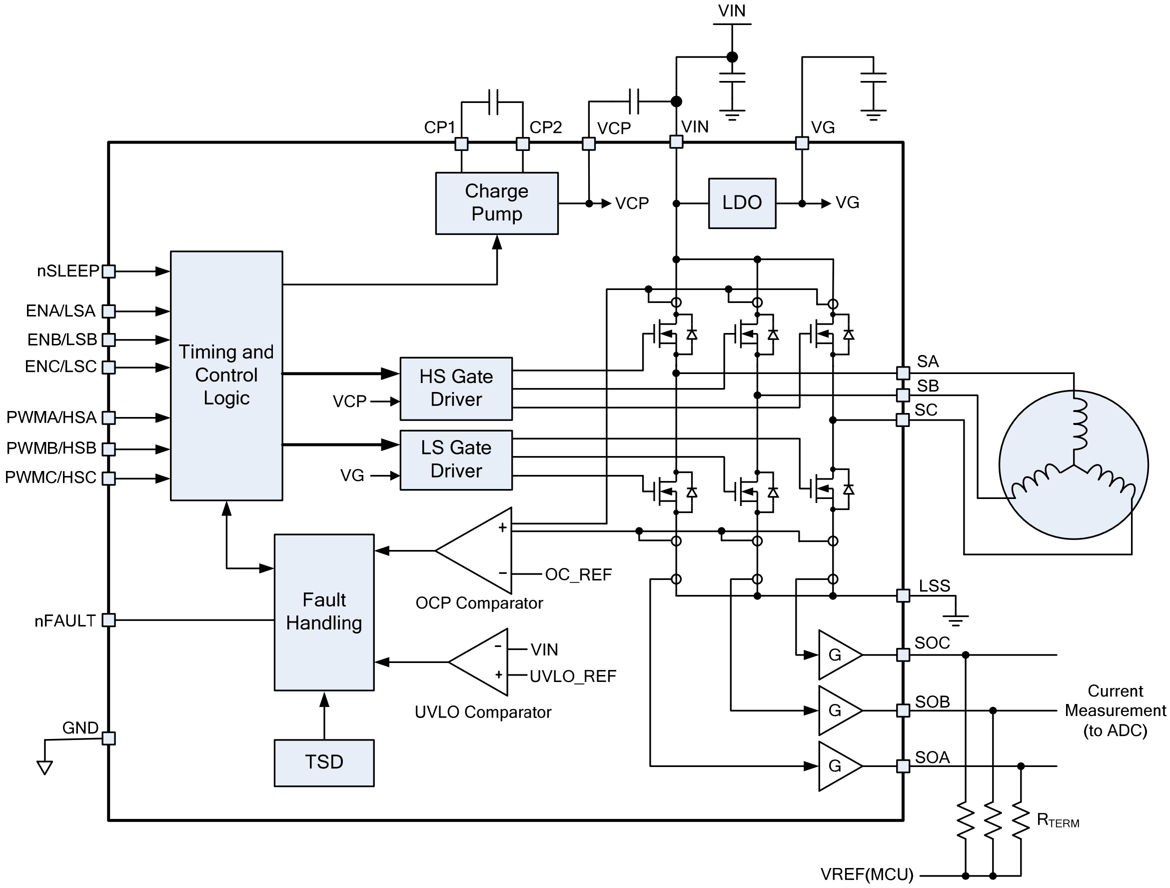



**Figure 1: Function Block Diagram**

# OPERATION

## Input Logic

The MP6540 has three logic input pins (ENA, ENB, ENC) that enable corresponding outputs (SA, SB, SC). When ENx is low, the corresponding output is disabled (output is at high impedance), and the PWM input on that phase is ignored. When ENx is high, the output is enabled, and the PWM input controls the state of the output (see Table 1).

**Table 1: PWM Input Logic Truth Table**

| ENx | PWMx | Sx |
|---|---|---|
| H | H | VIN |
| H | L | GND |
| L | X | High impedance |

The MP6540A has separate inputs that are used to enable the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) of each phase independently (see Table 2).

**Table 2: HS + LS Input Logic Truth Table**

| HSx | LSx | Sx |
|---|---|---|
| L | L | High impedance |
| L | H | GND |
| H | L | VIN |
| H | H | High impedance |

Note that the logic inputs have internal, weak, pull-down resistors.

## nSLEEP Operation

Driving nSLEEP low puts the device into a low-power sleep state. In this state, all internal circuits are disabled. All inputs are ignored when nSLEEP is active low. When waking up from sleep mode, approximately 1ms of time must pass before the device responds to the inputs. The nSLEEP input has a weak pull-down resistor.

## Current Sense Amplifiers

The current flowing in each of the three outputs is sensed by the internal current sensing circuits. An output pin for each phase sources or sinks a current proportional to the current flowing in each phase. Note that only the current flowing in the LS-FET is sensed and is sensed in both forward and reverse directions.

To convert this current into a voltage (i.e.: to input to an A/D converter), a termination resistor ($R_{TERM}$) is used as a reference voltage. When there is no current flowing, the resulting output is equal to the reference voltage. When current is flowing, the voltage is above or below the reference voltage according to Equation (1):

$$V = V_{TERM} + (R_{TERM} * I_{OUT}) / 9{,}200 \qquad (1)$$

To terminate the outputs when using an A/D converter with inputs that are ratiometric to its supply voltage, connect two equal-value resistors to the ADC supply and ground. The resulting ADC code is half-scale at zero current.

Figure 2 shows a simplified drawing of the current measurement circuit.

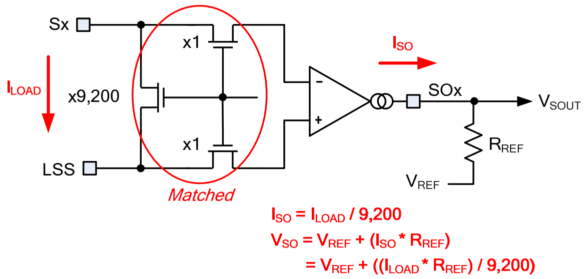



**Figure 2: Current Measurement Circuit**

## Automatic Synchronous Rectification

When driving a current through an inductive load and the output MOSFETs are both turned off, the recirculation current must continue flowing. This current is passed through the MOSFET body diodes, typically. To prevent excess power dissipation in the body diodes, the MP6540 implements an automatic synchronous rectification feature.

When both the HS-FET and LS-FET are turned off and the voltage on an Sx output pin is driven below ground, the LS-FET is turned on until the current flowing through it reaches near zero or until the HS-FET is commanded to turn on. Similarly, if Sx rises above VIN, the HS-FET is turned on until the current reaches near zero or the LS-FET is turned on.

### nFAULT Output

The MP6540 provides an nFAULT output pin, which is driven to active low in the case of a fault condition, such as over-current or over-temperature. nFAULT is an open-drain output and must be pulled up by an external pull-up resistor.

### Input Under-Voltage Lockout (UVLO) Protection

If at any time the voltage on VIN falls below the under-voltage lockout (UVLO) threshold voltage, all circuitry in the device is disabled, and the internal logic is reset. Operation resumes when VIN rises above the UVLO threshold.

### Thermal Shutdown

If the die temperature exceeds safe limits, all output MOSFETs are disabled, and the nFAULT pin is driven low. Once the die temperature falls to a safe level, operation resumes automatically.

### Over-Current Protection (OCP)

The over-current protection (OCP) circuit limits the current through each MOSFET by disabling its gate driver. If the over-current limit threshold is reached and lasts longer than the over-current deglitch time, all six output MOSFETs are disabled (outputs have high impedance), and nFAULT is driven low. During this time, synchronous rectification is used to decay the current. The outputs are disabled for 10ms (typical) and are re-enabled automatically.

Over-current conditions on both high- and low-side devices (i.e.: a short to ground, supply, or across the motor winding) results in an over-current shutdown.

A simplified diagram of the OCP circuit for one output is shown in Figure 3.

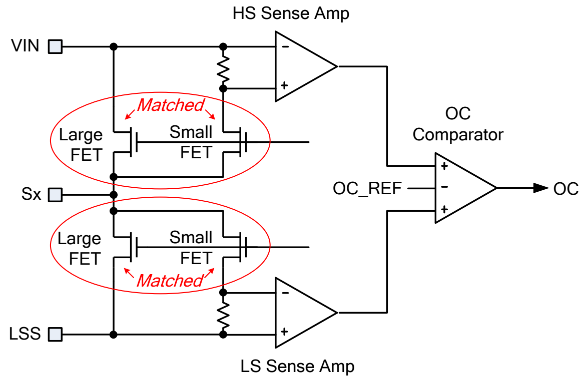



**Figure 3: OCP Measurement Circuit**

### Charge Pump and VG Regulator

An internal LDO regulator generates a low-side gate drive voltage of approximately 5.5V. A bypass capacitor of 4.7 - 10μF is required from VG to ground.

A charge pump is used to generate the gate drive for the HS-FETs. The charge pump requires two external capacitors: a 0.1μF ceramic capacitor rated for at least VIN between the CP1 and CP2 pins, and a 1μF ceramic capacitor rated for at least 10V between VIN and VCP.

# APPLICATION INFORMATION

## Charge Pump External Capacitors

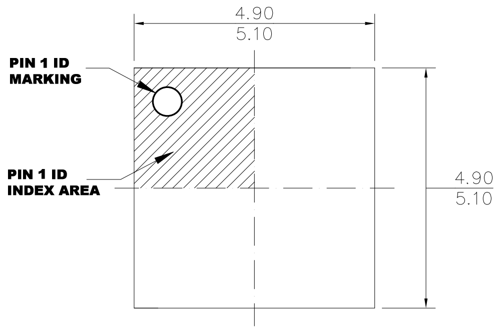
The external charge pump capacitors should be selected using Table 3.

**Table 3: External Charge Pump Capacitor Selector**

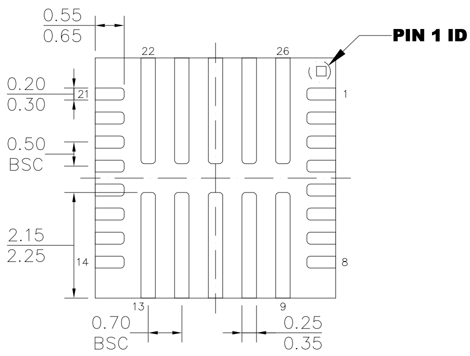
| | Min | Nom | Max | Unit |
|---|---|---|---|---|
| CP1 - CP2 capacitance | | 0.1 | | μF |
| CP1 - CP2 cap voltage | $V_{IN}$ | | | V |
| $V_{CP}$ - $V_{IN}$ capacitance | | 1 | | μF |
| $V_{CP}$ - $V_{IN}$ cap voltage | 10 | | | V |
| $V_G$ capacitance | 4.7 | | 10 | μF |
| $V_G$ cap voltage | 10 | | | V |

# PACKAGE INFORMATION

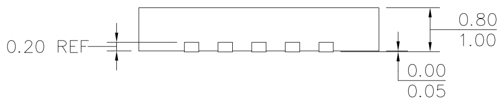
## QFN-26 (5mmx5mm)



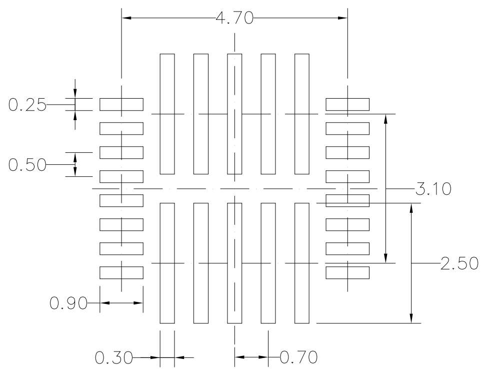

**TOP VIEW**




**BOTTOM VIEW**




**SIDE VIEW**




**RECOMMENDED LAND PATTERN**

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) REFERENCEIS MO-220.
5) DRAWING IS NOT TO SCALE.