MP6903

Fast Turn-off Intelligent Controller

The Future of Analog IC Technology®

DESCRIPTION

The MP6903 is a low-drop diode emulator that, combined with an external switch, replaces Schottky diodes in high-efficiency LLC converters. The chip regulates the forward drop of an external switch to about 70mV and switches it off as soon as the voltage goes negative. MP6903 has a light-load sleep mode that reduces the quiescent current to < 300μA.

FEATURES

- Works with Standard and Logic-Level FETS
- Compatible with Energy Star, 1W Standby Requirements
- V_{DD} Range from 8V to 24V
- 70mV V_{DS} Regulation Function (1)
- Fast Turn-Off: Total Delay of 20ns
- Max 400kHz Switching Frequency
- Light Load Mode Function (1) with <300μA Quiescent Current
- Supports DCM, CCM and CrCM Operation
- Supports High-Side and Low-Side Rectification
- Power Savings of Up to 1.5W for a Typical Notebook Adapter

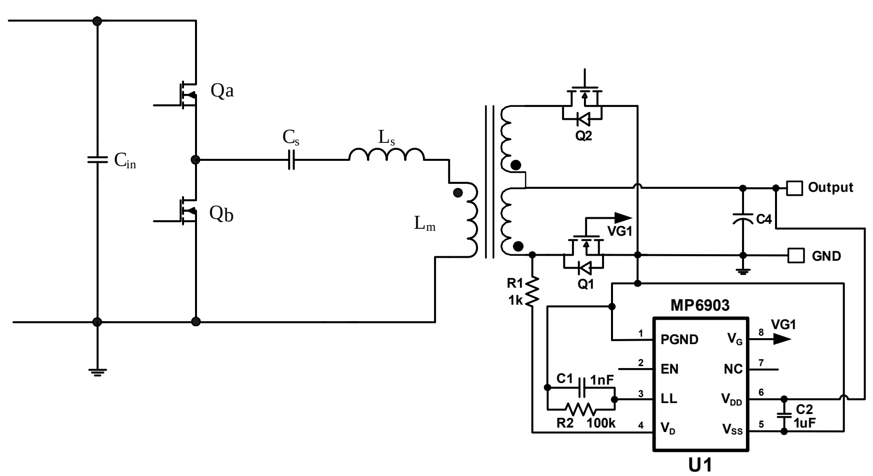
APPLICATIONS

- Industrial Power Systems
- Distributed Power Systems
- Battery Powered Systems
- LLC Converters

Notes:

1) Related issued patent: US Patent US8,067,973; US8,400,790. CN Patent ZL201010504140.4; ZL200910059751.X. Other patents pending.

TYPICAL APPLICATION

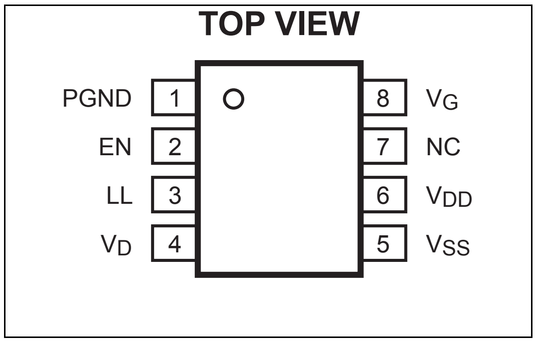


ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6903DS	SOIC8	MP6903

* For Tape & Reel, add suffix –Z (e.g. MP6903DS–Z);
For RoHS Compliant Packaging, add suffix –LF (e.g. MP6903DS–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS [2]

V_{DD} to V_{SS}......................................-0.3V to +27V
PGND to V_{SS}................................-0.3V to +0.3V
V_G to V_{SS}... -0.3V to V_{DD}
V_D to V_{SS}.....................................-0.7V to +180V
LL, EN to V_{SS}...............................-0.3V to +6.5V
Maximum Operating Frequency............. 400kHz
Continuous Power Dissipation (T_A=25°C) [3]
.... 1.4W
Junction Temperature...............................150°C
Lead Temperature (Solder).......................260°C
Storage Temperature .... -55°C to +150°C

Recommended Operation Conditions [4]

V_{DD} to V_{SS}..8V to 24V
Operating Junction Temp. (T_J).... -40°C to +125°C

Thermal Resistance [5] θ_{JA} θ_{JC}

SOIC8 ....90 ...... 45 ... °C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12V, -40°C ≤T_J≤ 125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
V_{DD} Voltage Range			8		24	V
V_{DD} UVLO Rising			4.8	6.0	7.0	V
V_{DD} UVLO hysteresis			0.8	1	1.2	V
Operating Current	I_{CC}	C_{LOAD}=5nF, f_{SW}=100kHz		8	10	mA
Quiescent Current	I_q	V_{SS}-V_D=0.5V		2	3	mA
Shutdown Current		V_{DD} =4V		190	260	μA
		V_{DD}=20V, EN=0V		350	420	μA
Light-Load Mode Current				290	400	μA
Thermal Shutdown (6)				180		°C
Thermal Shutdown Hysteresis (6)				40		°C
Enable UVLO Rising			1.1	1.5	1.9	V
Enable UVLO Hysteresis				0.2	0.4	V
Internal Pull-up Current on EN Pin				10	15	μA
CONTROL CIRCUITRY SECTION						
V_{SS} –V_D Forward Voltage	V_{fwd}		55	70	85	mV
Turn-on delay	t_{Don}	C_{LOAD} = 5nF, -20°C≤T_J≤125°C		250	380	ns
		C_{LOAD} = 5nF, -40°C≤T_J<-20°C		650		ns
	t_{Don}	C_{LOAD} = 10nF, -20°C≤T_J≤125°C		400	680	ns
		C_{LOAD} = 10nF, -40°C≤T_J<-20°C		1200		ns
Input Bias Current on V_D Pin		V_D = 180V		0.5	3	μA
Minimum On-Time	t_{MIN}	C_{LOAD} = 5nF	0.4	0.8	1.2	μs
Light-Load-Enter Delay	$t_{LL-Delay}$	R_{LL}=100kΩ	80	120	150	μs
Light-Load-Enter Pulse Width	t_{LL}	R_{LL}=100kΩ	1.3	1.75	2.2	μs
Light-Load-Enter Pulse Width Hysteresis	t_{LL-H}	R_{LL}=100kΩ		0.2		μs
Light-Load Resistor Value	R_{LL}		30		300	kΩ
Light-Load Mode Exit Pulse Width Threshold (V_{DS})	V_{LL-DS}		-400	-250	-150	mV
Light-Load Mode Enter Pulse Width Threshold (V_{GS}) (6)	V_{LL-GS}			1.0		V
GATE DRIVER SECTION						
V_G (Low)		I_{LOAD}=1mA		0.05	0.1	V
V_G (High)		V_{DD} >17V	13	14.5	16	V
		V_{DD} <17V	V_{DD}-2.2			
Turn Off Threshold (V_{SS}-V_D) (6)				-30		mV
Turn Off Threshold During Blanking Time (V_{SS}-V_D) (6)				-100		mV
Turn-Off Propagation Delay		V_D=V_{SS}		15		ns
Turn-Off, Total Delay	t_{Doff}	V_D =V_{SS}, C_{LOAD}=5nF, R_{GATE}=0Ω		60	120	ns
	t_{Doff}	V_D =V_{SS}, C_{LOAD}=10nF, R_{GATE}=0Ω		60	120	ns
Pull Down Impedance				1	2	Ω
Pull Down Current (6)		3V <V_G<10V		2		A

Notes:

6) Guaranteed by Design and Characterization. Not tested in Production.

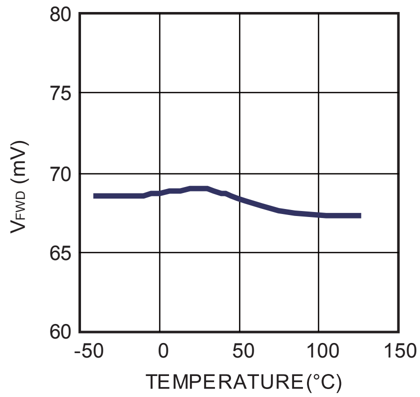
PIN FUNCTIONS

Pin #	Name	Description
1	PGND	Power Ground. Return for driver switch.
2	EN	Enable. Active high.
3	LL	Light Load Time Set. Connect a resistor to set the light load timing.
4	VD	MOSFET Drain Voltage Sense.
5	VSS	Ground. Also used as reference for VD.
6	VDD	Supply Voltage.
7	NC	No Connection.
8	VG	Gate Drive Output.

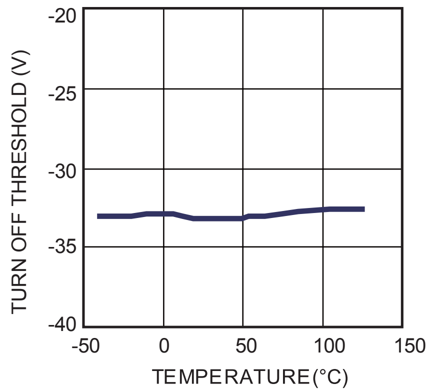
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 12V, unless otherwise noted.

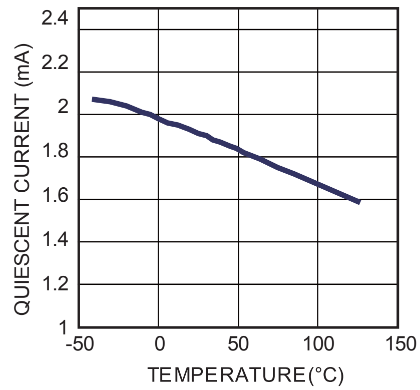
V_{FWD} vs. Temperature



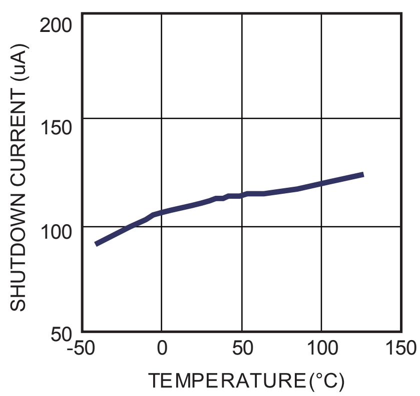
Turn off threshold vs. Temperature



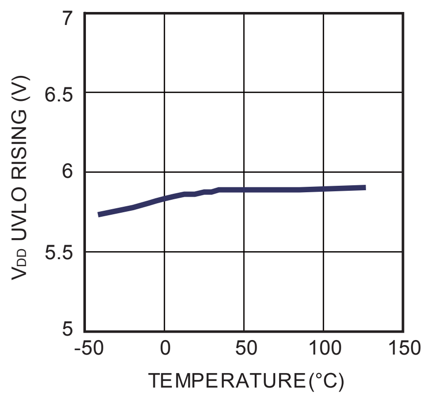
Quiescent Current vs. Temperature



Shutdown Current vs. Temperature

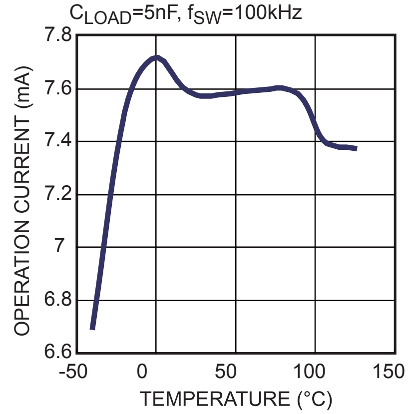


V_{DD} UVLO Rising vs. Temperature

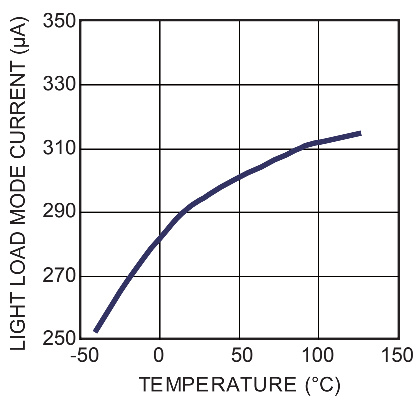


Operation Current vs. Temperature

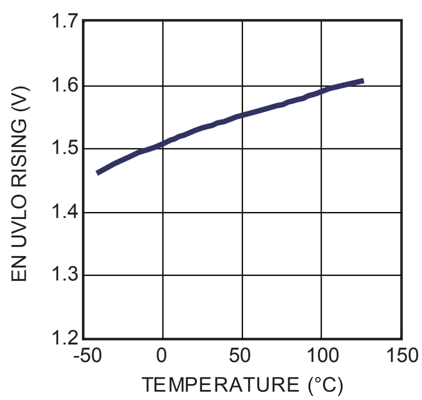
C_{LOAD}=5nF, f_{SW}=100kHz



Light Load Mode Current vs. Temperature

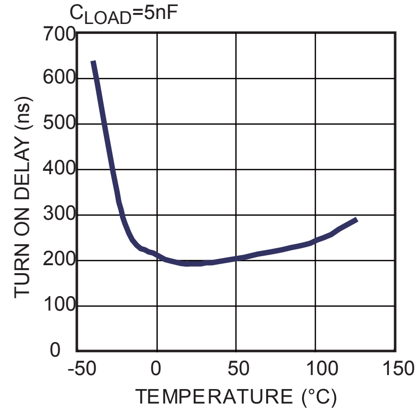


EN UVLO Rising vs. Temperature



Turn On Delay vs. Temperature

C_{LOAD}=5nF

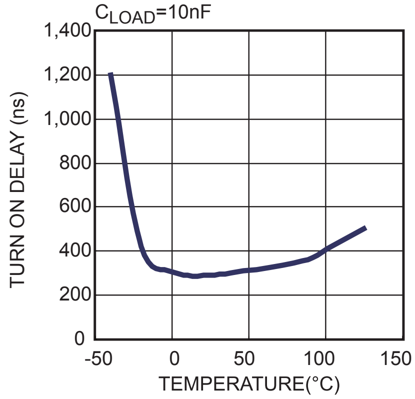


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} = 12V, unless otherwise noted.

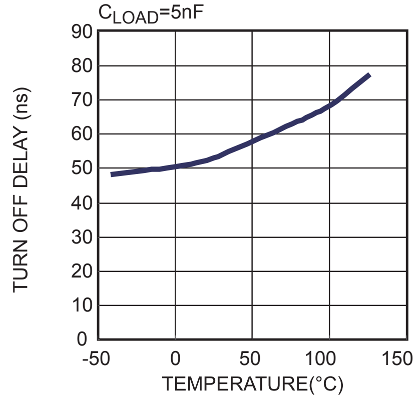
Turn On Delay vs. Temperature

C_{LOAD}=10nF



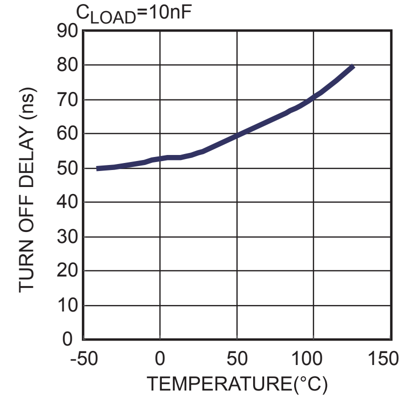
Turn Off Delay vs. Temperature

C_{LOAD}=5nF

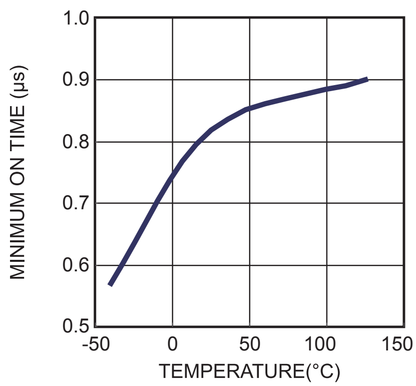


Turn Off Delay vs. Temperature

C_{LOAD}=10nF

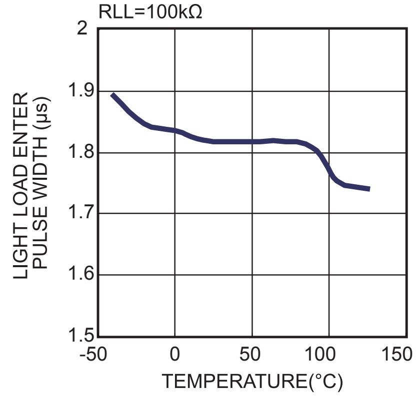


Minimum On Time vs. Temperature

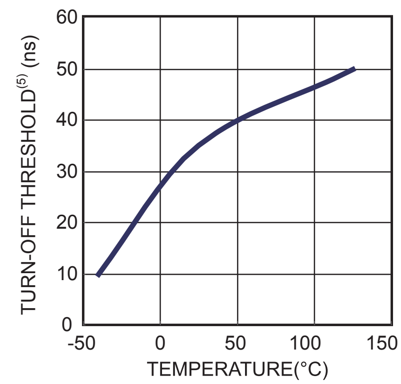


Light Load Enter Pulse Width vs. Temperature

RLL=100kΩ

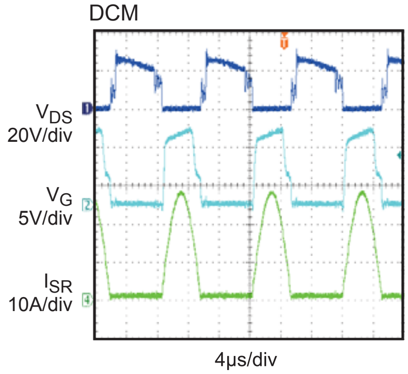


Turn-off Threshold(5) vs. Temperature



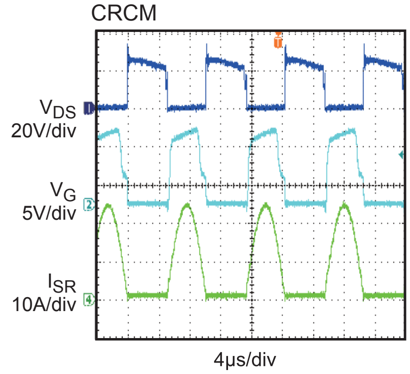
Operation in LLC Resonant Converter

V_{IN}=250V, V_{OUT}=12V, I_{OUT}=15A
DCM



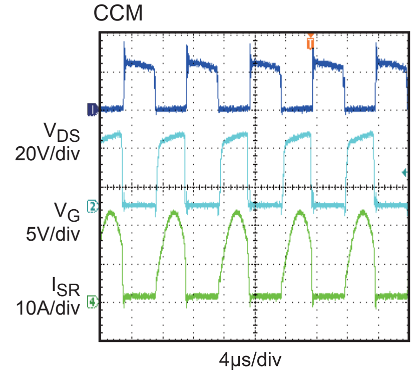
Operation in LLC Resonant Converter

V_{IN}=263V, V_{OUT}=12V, I_{OUT}=15A
CRCM



Operation in LLC Resonant Converter

V_{IN}=280V, V_{OUT}=12V, I_{OUT}=15A
CCM



FUNCTIONAL BLOCK DIAGRAM

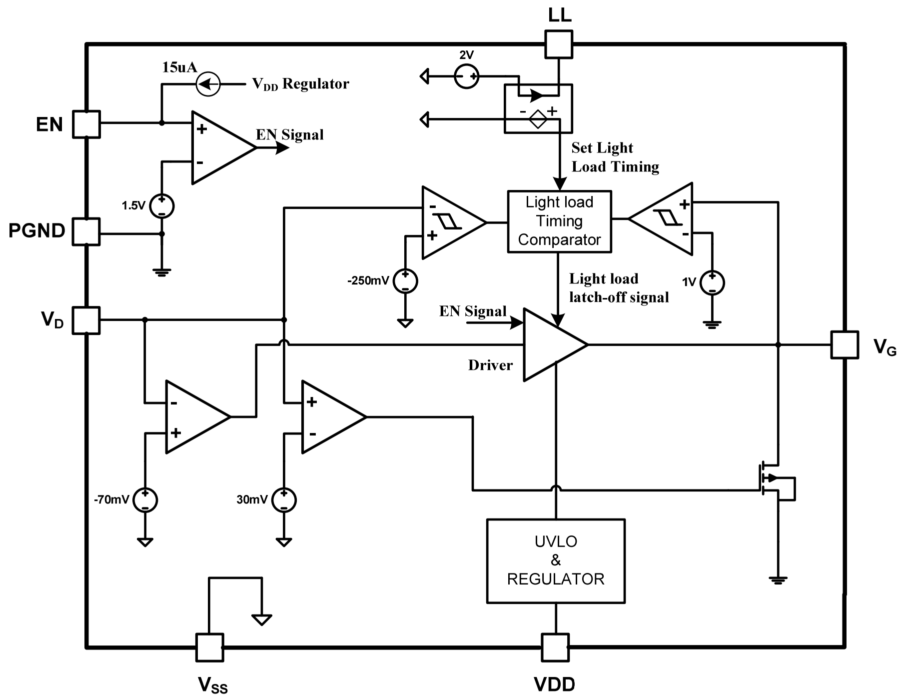


Figure 1: Functional Block Diagram

OPERATION

The MP6903 supports operation in discontinuous current mode (DCM), continuous current mode (CCM), and critical conduction mode (CrCM) condition. Operating in either a DCM or CrCM condition, the control circuitry controls the gate in forward mode and will turn the gate off when the MOSFET current goes low. In CCM operation, the control circuitry turns off the gate when very fast transients occur.

Blanking

The control circuitry contains a blanking function. When the MOSFET turns on or off, the blanking function ensures that the previous state extends for some minimum time period. The turn-on blanking time is ~0.8μs. During the turn-on blanking period, the turn-off threshold is not totally blanked, but changes the threshold voltage to approximately 100mV (instead of 30mV). This assures that the part can always turn off even during the turn-on blanking period. (The synchronous period is recommended to be greater than 0.8μs in CCM in the LLC Converter to avoid shoot-through.)

VD Clamp

A high-voltage JFET is used at the input because V_D can go as high as 180V. To avoid excessive currents when V_G goes below -0.7V, add a small resistor between V_D and the drain of the external MOSFET.

Under-Voltage Lockout (UVLO)

When V_{DD} drops below the UVLO threshold, the part goes into sleep mode and a 10kΩ resistor pulls the V_G pin low.

Enable pin

EN is internal pulled up by the regulator from V_{DD} with a ~15uA current source. Leave this pin open if unused.

When use external signal to control EN, it is highly recommended the pull down current be larger than 15uA to make sure the EN pin can be pulled to low.

Thermal shutdown

If the junction temperature of the chip exceeds 180°C, the VG will be pulled low and the part stops switching. The part will resume normal function after the junction temperature has dropped to 150°C.

Turn-On Phase

When the synchronous MOSFET is on, current flows through its body diode and generates a negative V_{DS}. This body diode voltage drop (< -500mV) is much smaller than the turn-on threshold of the control circuitry (-70mV), which then pulls the gate driver voltage high to turn on the synchronous MOSFET after about 250ns turn-on delay (shown in Figure 2).

When the turn-on delay ends, turn-on starts with a blanking time (minimum on-time: ~0.8µs), and the turn-off threshold changes from +30mV to +100mV. This blanking time helps to avoid errors around the turn-off threshold caused by turn-on ringing of the synchronous MOSFET.

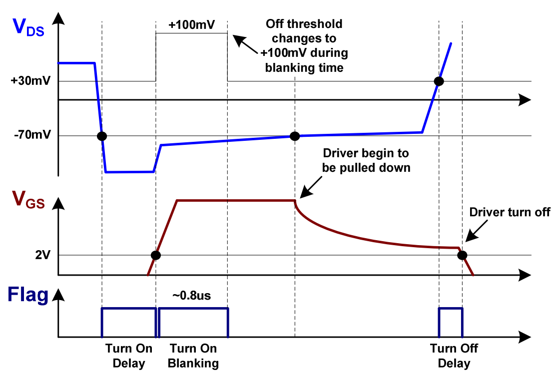


Figure 2: Turn On/Off Timing Diagram

Conducting Phase

When the synchronous MOSFET turns on, V_{DS} rises according to the MOSFET's ON resistance. When V_{DS} rises above the turn-on threshold (-70mV), the control circuitry stops pulling up the gate driver, so the gate voltage is pulled down by the internal pull-down resistance (10kΩ) and leakage to increase the ON resistance of the synchronous MOSFET, which to limit the V_{DS} slew rate, stabilizes V_{DS} to around -70mV even when the current through the MOSFET is fairly small. This function limits the driver voltage when the synchronous MOSFET is turned off (this function is still active during turn-on blanking, which means the gate driver could still be turned-off even with very small duty cycles of the synchronous MOSFET).

Turn-Off Phase

When V_{DS} triggers the turn-off threshold (30mV), the gate voltage is pulled to low after a 20ns turn-off delay (shown in Figure 2) by the control circuitry.

Figure 3 shows synchronous rectification operation at heavy load. The gate driver initially saturates due to the high current. After V_{DS} rises above -70mV, the gate driver voltage decreases to adjust the V_{DS} to around -70mV.

Figure 4 shows synchronous rectification operation at light load. The gate driver voltage never saturates due to the low current, but decreases as soon as the synchronous MOSFET turns on and adjusts the V_{DS}.

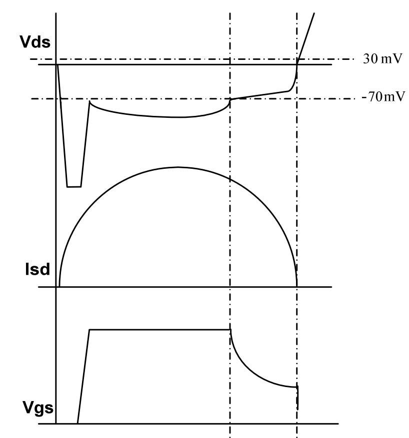


Figure 3: Synchronous Rectification Operation at Heavy Load

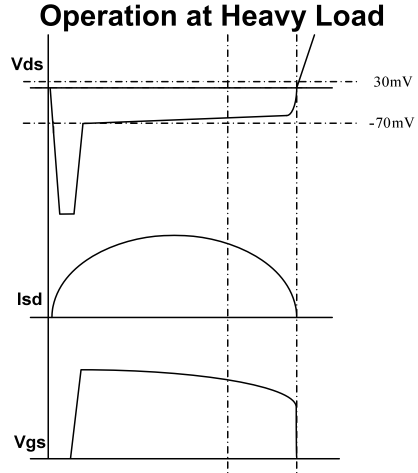


Figure 4: Synchronous Rectification Operation at Light Load

Light-Load Latch-Off Function

The gate driver of MP6903 is latched to save the driver loss at light-load condition to improve efficiency. See Figure5, when the synchronous MOSFET's conducting period keeps lower than light load timing (T_{LL}) for longer than the light-load-enter delay ($T_{LL-Delay}$), MP6903 enters light-load mode and latches off the gate driver. Here the synchronous MOSFET's conducting period is from turn on of the gate driver to the moment when V_{GS} drops to below 1V (V_{LL_GS}).

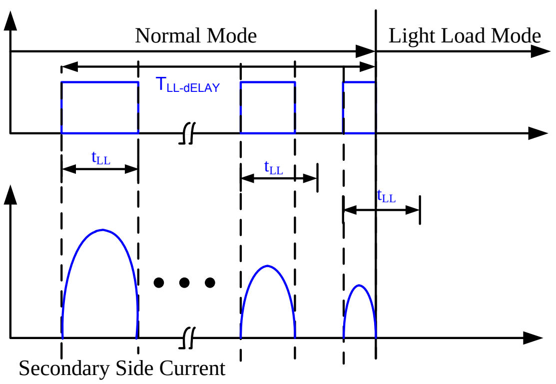


Figure 5: MP6903 Enters Light Load Mode

During light-load mode, MP6903 monitors the synchronous MOSFET's body diode conducting period by sensing the time duration of the V_{DS} below -250mV(V_{LL_DS}). If it is longer than T_{LL}+T_{LL-H} (T_{LL-H}, light-load-enter pulse width hysteresis), the light-load mode is finished and gate driver of MP6903 is unlatched to restart the synchronous rectification, see Figure6.

For MP6903, the light load enter timing (T_{LL}) is programmable by connecting a resistor (R_{LL}) on LL pin, by monitoring the LL pin current (the LL pin voltage keeps at ~2V internally), T_{LL} is set as following (a 1nF capacitor is recommended to decouple the noise on this pin):

$$T_{LL} \approx R_{LL}(k\Omega) \cdot \frac{2.2us}{100k\Omega}$$

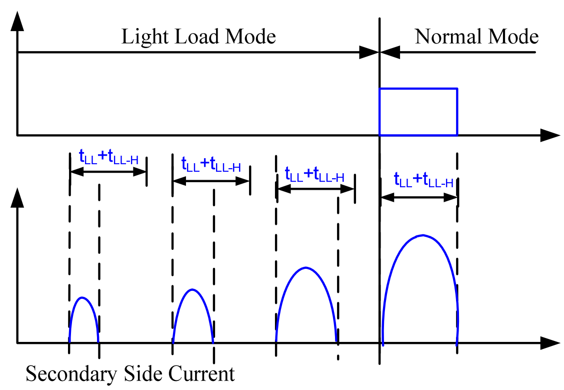
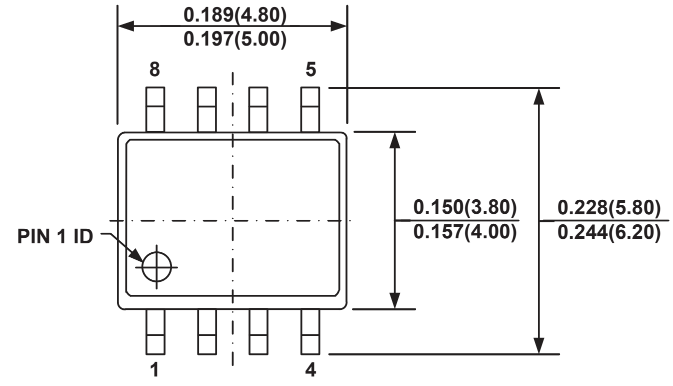


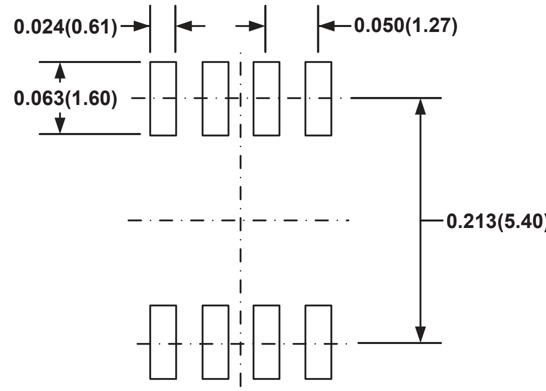
Figure 6: MP6903 Exits Light Load Mode

PACKAGE INFORMATION

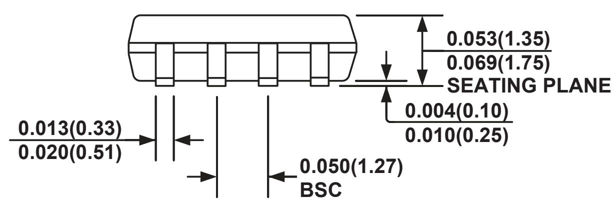
SOIC8



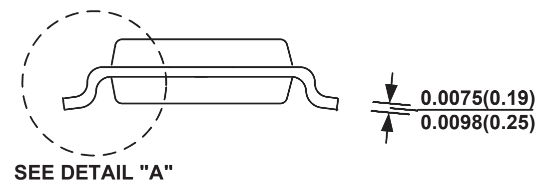
TOP VIEW



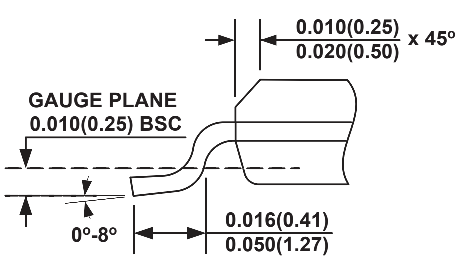
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.