MP6908

Fast Turn-Off Intelligent Rectifier with No Need for Auxiliary Winding

DESCRIPTION

The MP6908 is a low-drop diode emulator IC that, when combined with an external switch, replaces Schottky diodes in high-efficiency flyback converters. The MP6908 regulates the forward drop of an external synchronous rectifier (SR) MOSFET to about 40mV, which switches off once the voltage becomes negative.

The MP6908 can generate its own supply voltage for battery charging applications with potential low output voltage, and at short circuit output condition, or for high-side SR configuration. Programmable ringing detection circuitry prevents the MP6908 from turning on falsely at Vds oscillations during discontinuous conduction mode (DCM) and quasi-resonant operation.

The MP6908 is available in a space-saving TSOT23-6 package.

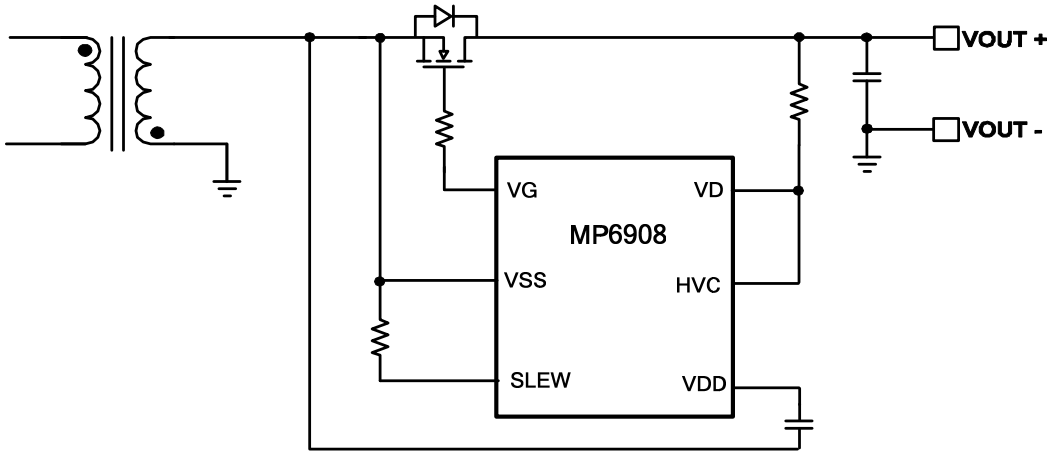
FEATURES

- Wide Output Range down to 0V, No Short Circuit Current Flows through Body Diode
- No Need for Auxiliary Winding for High-Side or Low-Side Rectification
- Ringing Detection Prevents False Turn-On during DCM and Quasi-Resonant Operations
- Works with Standard and Logic Level SR MOSFETS
- Compatible with Energy Star
- ~30ns Fast Turn-Off and Turn-On Delay
- ~100μA Quiescent Current
- Supports DCM, CCM, and Quasi-Resonant Operations
- Supports both High-Side and Low-Side Rectification
- TSOT23-6 Package Available

APPLICATIONS

- USB PD Quick Chargers
- Adaptors
- Flyback Power Supplies with Very Low and/or Variable Output Voltage

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6908GJ	TSOT23-6	*See Below*

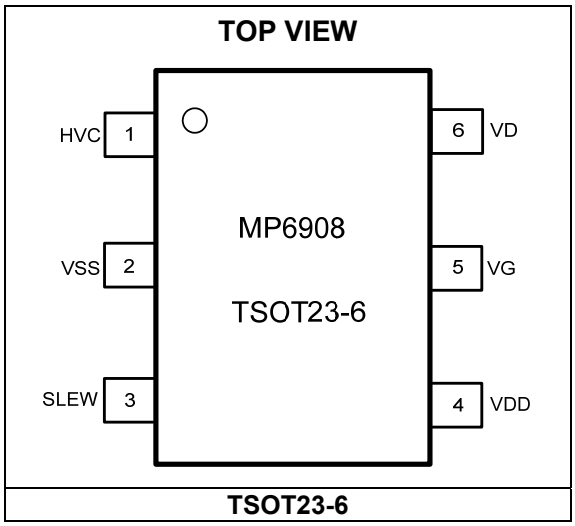
* For Tape & Reel, add suffix –Z (e.g. MP6908GJ–Z)

TOP MARKING

|AZEY

AZE: Product code of MP6908GJ
Y: Year code

PACKAGE REFERENCE



TSOT23-6

ABSOLUTE MAXIMUM RATINGS (1)

VDD, VG to VSS ..... -0.3V to +14V
VD, HVC to VSS ..... -1V to +180V
SLEW to VSS ..... -0.3V to +6.5V
Continuous power dissipation (T_A = +25°C)(2) 0.56W
Junction temperature ..... 150°C
Lead temperature (solder) ..... 260°C
Storage temperature ..... -55°C to +150°C

Recommended Operation Conditions (3)

VDD to VSS ..... 4V to 13V
VD, HVC to VSS ..... -1V to +150V
Maximum junction temperature (T_J) ..... 125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6	220	110	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VDD = 5V, T_J = -40°C~125°C, unless otherwise noted.

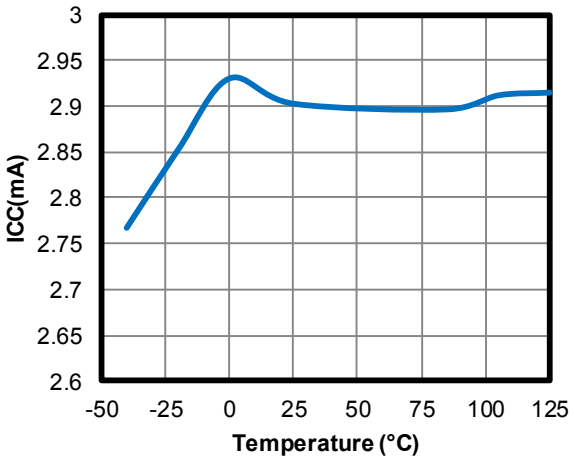
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Management Section						
VDD UVLO rising			3.55	3.75	3.95	V
VDD UVLO hysteresis			0.1	0.2	0.3	V
VDD maximum charging current	I_{VDD}	VDD = 7V, HVC = 40V	35	70	110	mA
		VDD = 4V, VD = 30V	20	40	60	
VDD regulation voltage		VD = 12V, HVC = 12V	8.5	9	9.5	V
		HVC = 3V, VD = 12V	4.6	5	5.4	
Operating current	I_{CC}	VDD = 9V, C_{LOAD} = 2.2nF, F_{SW} = 100kHz		2.9	3.5	mA
		VDD = 5V, C_{LOAD} = 2.2nF, F_{SW} = 100kHz		1.72	2.1	mA
Quiescent current	$I_{q(VDD)}$	VDD = 5V		100	130	µA
Shutdown current	$I_{SD(VDD)}$	VDD = UVLO - 0.1V			100	µA
Control Circuitry Section						
Forward regulation voltage (VSS - VD)	V_{fwd}		25	40	55	mV
Turn-on threshold (VDS)			-115	-86	-57	mV
Turn-off threshold (VSS - VD)			-6	3	12	mV
Turn-on delay	T_{Don}	C_{LOAD} = 2.2nF		30	50	ns
Turn-off delay	T_{Doff}	C_{LOAD} = 2.2nF		25	45	ns
Turn-off propagation delay(5)				15		ns
Turn-on blanking time	T_{B-ON}	C_{LOAD} = 2.2nF	0.75	1.1	1.45	µs
Turn-off blanking threshold (VDS)	V_{B-OFF}		2	2.5	3	V
Turn-off threshold during minimum on time (VDS)			1.3	1.8	2.1	V
Turn-on slew rate detection timer	T_{SLEW}	R_{SLEW} = 400kΩ	65	90	115	ns
Gate Driver Section						
VG (low)	V_{G-L}	I_{LOAD} = 10mA		0.01	0.02	V
VG (high)	V_{G-H}	I_{LOAD} = 0mA	4.9			V
Maximum source current (5)				0.5		A
Maximum sink current (5)				3		A
Pull-down impedance		Same as VG (low)		1	2	Ω

NOTE:

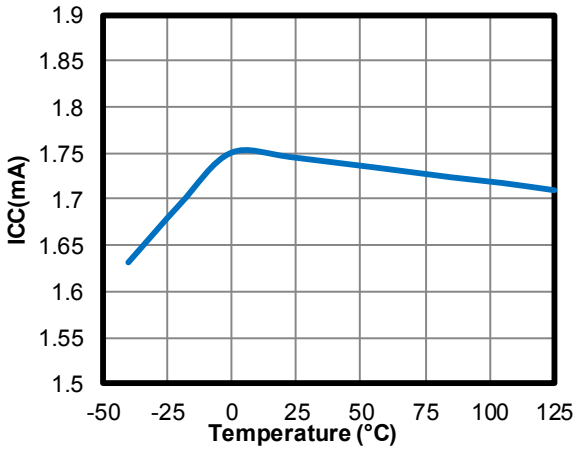
5) Guaranteed by characterization and design.

TYPICAL PERFORMANCE CHARACTERISTICS

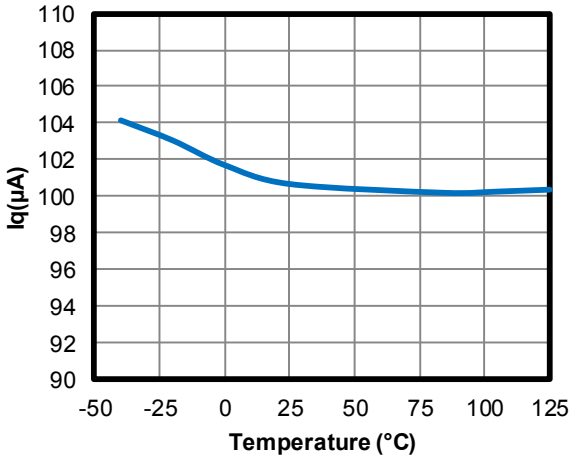
Operating Current vs. Temperature
VDD = 9V, C_{LOAD} = 2.2nF, F_{SW} = 100kHZ



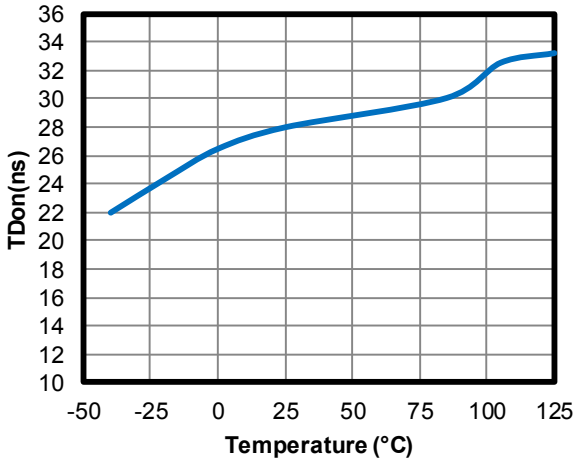
Operating Current vs. Temperature
VDD = 5V, C_{LOAD} = 2.2nF, F_{SW} = 100kHz



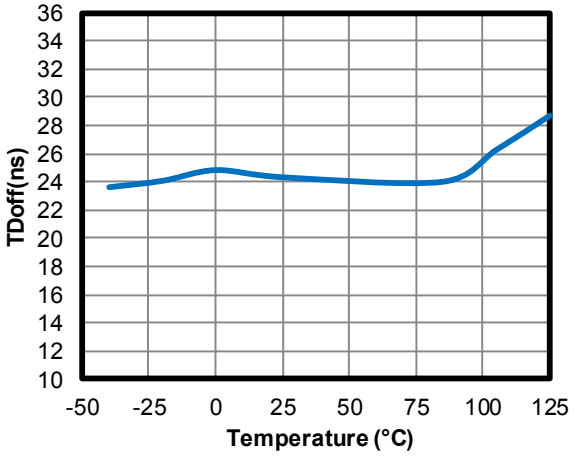
Quiescent Current vs. Temperature
VDD = 5V



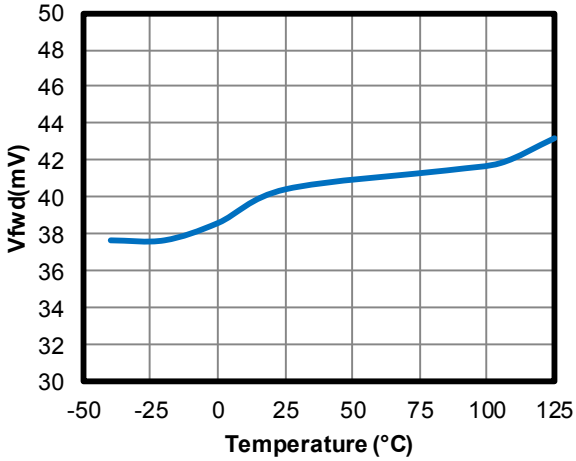
Turn-On Delay vs. Temperature
VDD = 9V, C_{LOAD} = 2.2nF



Turn-Off Delay vs. Temperature
VDD = 9V, C_{LOAD} = 2.2nF



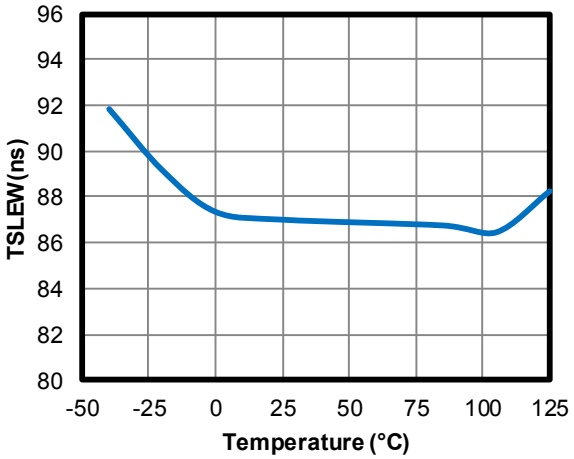
Forward Regulation Voltage (VSS - VD) vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

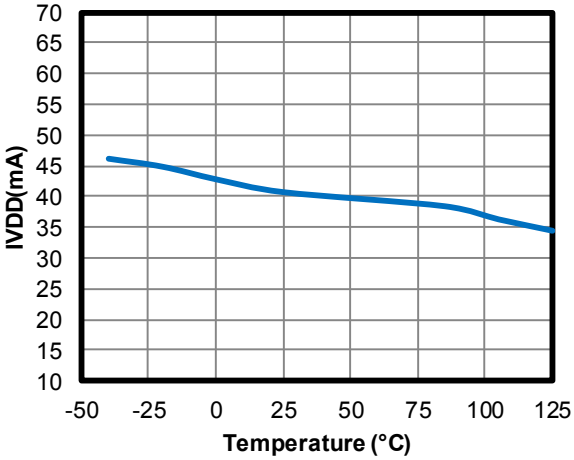
Turn-On Slew Rate Detection Timer vs. Temperature

R_{SLEW} = 400kΩ



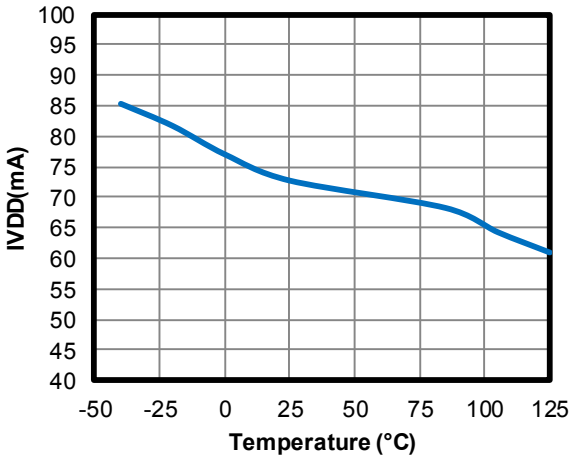
VDD Maximum Charging Current vs. Temperature

VDD = 4V, VD = 30V



VDD Maximum Charging Current vs. Temperature

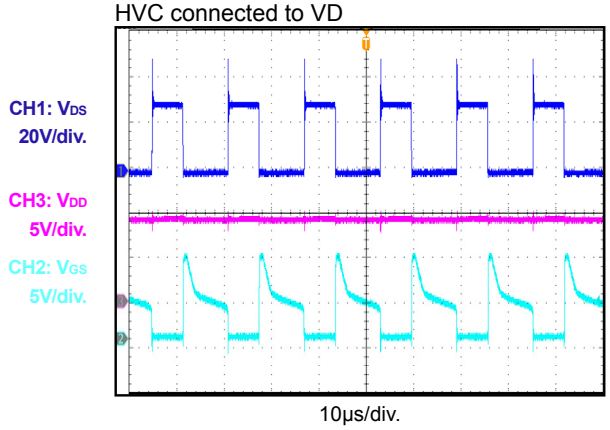
VDD = 7V, HVC = 40V



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

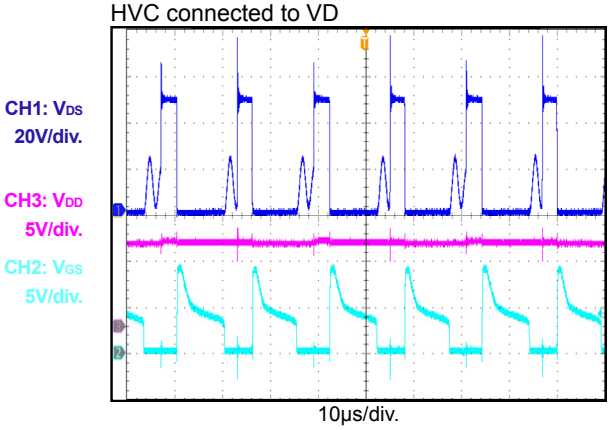
Operation in 36W Flyback Application

V_{IN} = 110V_{AC}, V_{OUT} = 12V, I_{OUT} = 3A,
HVC connected to VD



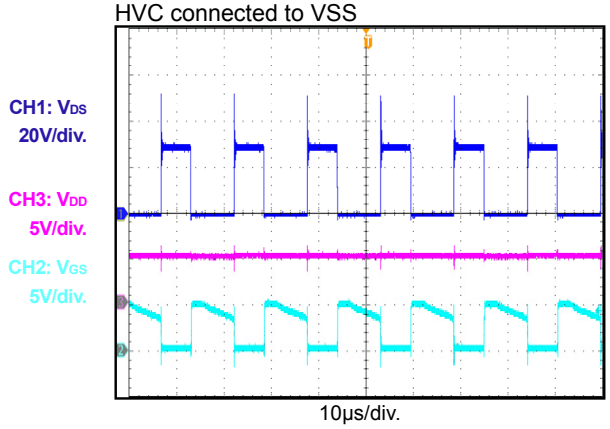
Operation in 36W Flyback Application

V_{IN} = 220V_{AC}, V_{OUT} = 12V, I_{OUT} = 3A,
HVC connected to VD



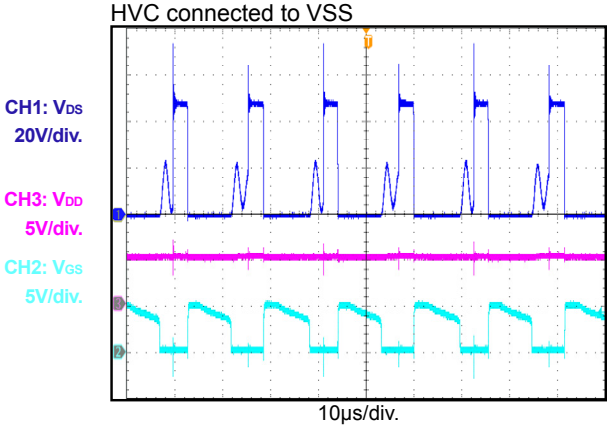
Operation in 36W Flyback Application

V_{IN} = 110V_{AC}, V_{OUT} = 12V, I_{OUT} = 3A
HVC connected to VSS



Operation in 36W Flyback Application

V_{IN} = 220V_{AC}, V_{OUT} = 12V, I_{OUT} = 3A
HVC connected to VSS



PIN FUNCTIONS

Pin #	Name	Description
1	HVC	**HV linear regulator input.**
2	VSS	**Ground.** VSS is also used as a MOSFET source sense reference for VD.
3	SLEW	**Programming for turn-on signal slew rate detection.** SLEW prevents the SR controller from turning on falsely by ringing below the turn-on threshold at VD in discontinuous conduction mode (DCM) and quasi-resonant mode. Any signal slower than the pre-set slew rate cannot turn on VG.
4	VDD	**Linear regulator output.** VDD is the supply of the MP6908.
5	VG	**Gate drive output.**
6	VD	**MOSFET drain voltage sense.**

BLOCK DIAGRAM

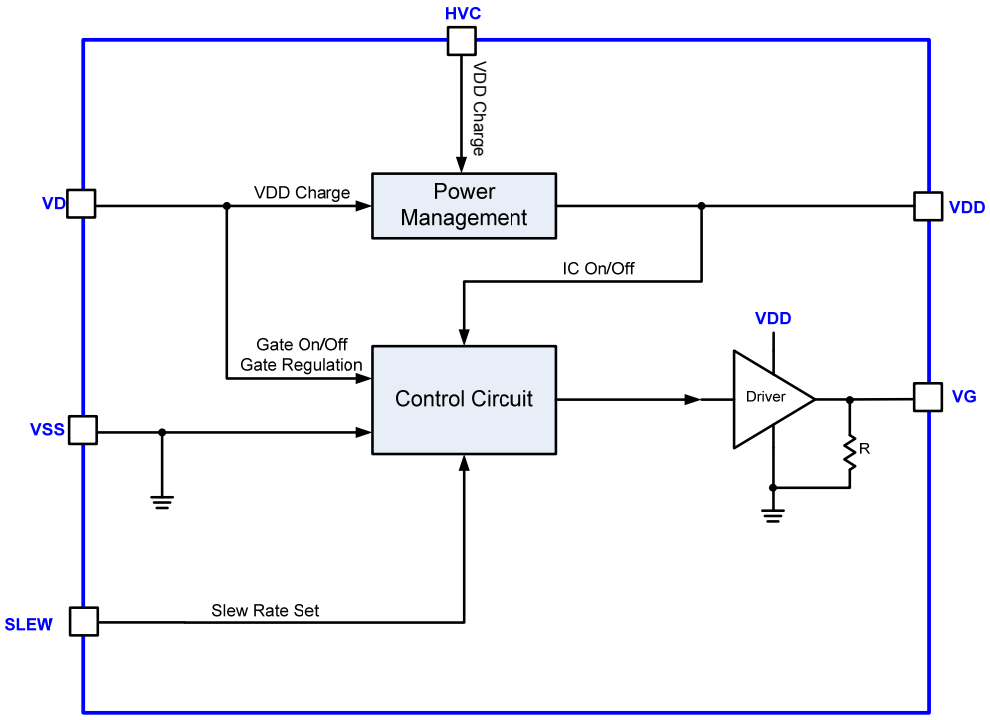


Figure 1: Functional Block Diagram

OPERATION

The MP6908 supports operation in discontinuous conduction mode (DCM), continuous conduction mode (CCM), and quasi-resonant flyback converters. The control circuitry controls the gate in forward mode and turns the gate off when the synchronous rectification (SR) MOSFET current drops to zero.

VDD Generation

The capacitor at VDD supplies power for the IC. It can be charged up by both HVC and VD.

When V_{HVC}<4.7V, the VD charges up the external capacitor at VDD via a current source with 40mA and regulates it at 5V.

When 4.7V<V_{HVC}<9.7V, VD stops charging, and HVC charges VDD via a current source with 70mA and regulates it at V_{HVC} -0.7V.

When V_{HVC}>9.7V, the HVC charges VDD via a current source with 70mA and clamps it at 9V.

Start-Up and Under-Voltage Lockout (UVLO)

When VDD rises above 3.75V, the MP6908 exits under-voltage lockout (UVLO) and is enabled. The MP6908 enters sleep mode, and V_{GS} is kept low once VDD drops below 3.55V.

Turn-On Phase

When V_{DS} drops to ~2V, a turn-on timer begins to count. This turn-on timer can be programmed by an external resistor on SLEW. If V_{DS} reaches the -86mV turn-on threshold from 2V within the time(T_{SLEW}) set by the timer, the MOSFET is turned on after a turn-on delay (around 30ns) (see Figure 2). If V_{DS} crosses -86mV after the timer ends, the gate voltage (VG) remains off. This turn-on timer prevents the MP6908 from turning on falsely due to ringing from DCM and quasi-resonant operations.

T_{SLEW} can be programmed with Equation (1):

$$T_{SLEW} = R_{SLEW} \times \frac{90ns}{400k\Omega} \quad (1)$$

Turn-On Blanking

The control circuitry contains a blanking function. When the MOSFET turns on, the control circuit ensures that the on state lasts for a specific period of time. The turn-on blanking time is ~1.1µs to prevent an accidental turn-off due to ringing. However, if V_{DS} reaches 2 - 3V within the turn-on blanking time, V_{GS} is pulled low immediately.

Conduction Phase

When V_{DS} rises above the forward voltage drop (-40mV) according to the decrease of the switching current, the MP6908 lowers the gate voltage level to enlarge the on resistance of the synchronous MOSFET.

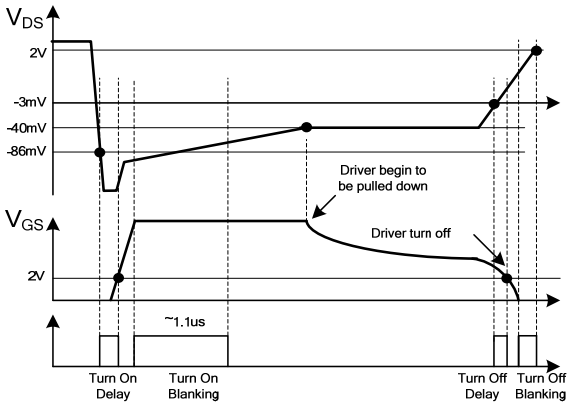


Figure 2: Turn-On/Turn-Off Timing Diagram

With this control scheme, V_{DS} is adjusted to be around -40mV even when the current through the MOSFET is fairly low. This function keeps the driver voltage at a very low level when the synchronous MOSFET is turned off, which boosts the turn-off speed and is especially important to CCM operation.

Turn-Off Phase

When V_{DS} rises to trigger the turn off threshold (-3mV), the gate voltage is pulled to zero after a very short turn-off delay of 25ns (see Figure 2).

Turn-Off Blanking

After the gate driver (V_{GS}) is pulled to zero by V_{DS} reaching the turn-off threshold (-3mV), a turn-off blanking time is applied, during which the gate driver signal is latched off. The turn-off blanking is removed when V_{DS} rises above 2V (see Figure 2).

APPLICATION INFORMATION

Slew Rate Detection Function

In DCM operations, the demagnetizing ringing may bring V_{DS} down below 0V. If Vds reaches the turn-on threshold during the ringing, SR controllers without the slew rate detection function may turn on the MOSFET by mistake. Figure 3 shows the waveform of this false turn-on situation. This does not only increase power loss, but may also lead to shoot through if the primary side FET is turned on within the minimum on time.

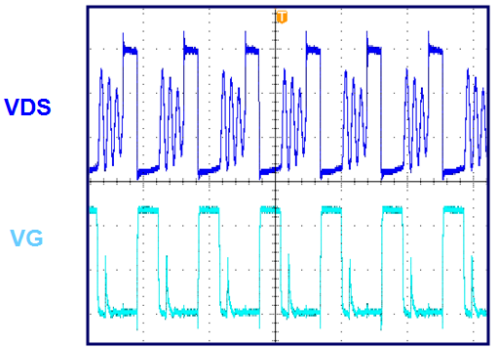


Figure 3: False Turn-on

(Without slew rate detection)

Considering the slew rate of the ringing is always much less than that when the primary MOSFET is really turned off, this false turn-on situation can be prevented by the slew rate detection function, as shown in Figure 4. When the slew rate is less than the threshold set by the R_{SLEW}, the IC does not turn on the gate even when V_{DS} reaches the turn-on threshold.

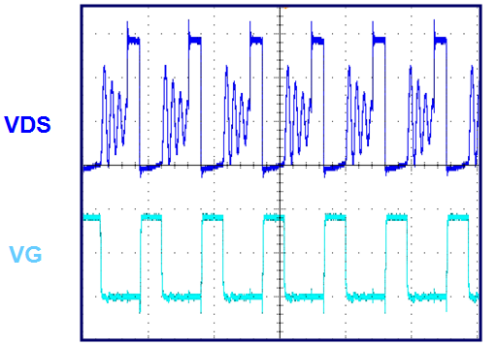


Figure 4: Prevent the False Turn-on

(With slew rate detection)

External resistor on VD and HVC

Over voltage conditions may lead to damage on the device, so there has to be appropriate application design to guarantee safe operation, especially on the high voltage pin.

One of the common over voltage conditions is when the body diode of the SR MOSFET is turned on, the forward voltage drop may exceed the negative rating on the VD pin. In this case, an external resistor is commended to be placed between VD and Drain of the MOSFET. In general, the resistance is recommended to be no less than 300 Ω.

On the other hand, this resistor cannot be too large, either, because it compromises the VDD supply and slow down the slew rate on the V_{DS} detection. In general, it is not recommended to use any resistance larger than 1kΩ, but for each practical case, it should be checked based on the condition of VDD supply and the slew rate.

In the applications where HVC may also suffer from negative voltage bias (e.g. in the high side setup without auxiliary winding), there should be also the same resistance be placed on HVC externally.

Typical System Implementations

Figure 5 shows the typical system implementation for the IC power supply derived from the output voltage (V_{OUT}), which is available in low-side rectification.

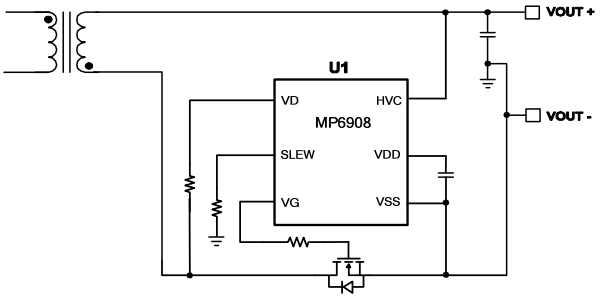


Figure 5: Low-Side Rectification

The MP6908 can support most applications, even when V_{OUT} is down to 0V for low-side rectification.

If the MP6908 is used for high-side rectification, a self-supply can be achieved three ways (see Figure 6-A, Figure 6-B, and Figure 7).

Figure 6-A shows HVC connected to VD. Here, VDD is generated and regulated at 9V.

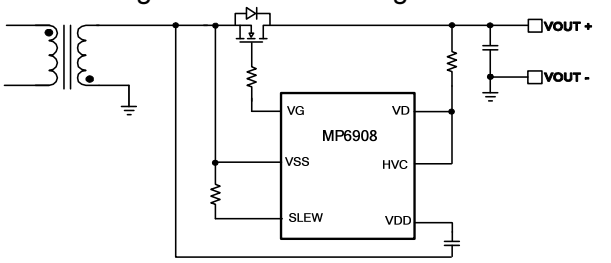


Figure 6-A: High-Side Rectification, VDD Regulated at 9V

Figure 6-B shows HVC connected to the secondary ground through an external diode. Here, VDD is generated from HVC and regulated at 9V. The maximum voltage at HVC can be calculated with Equation (2):

$$V_{HVC(\max)} = V_{IN} \times \frac{N_s}{N_p} \quad (2)$$

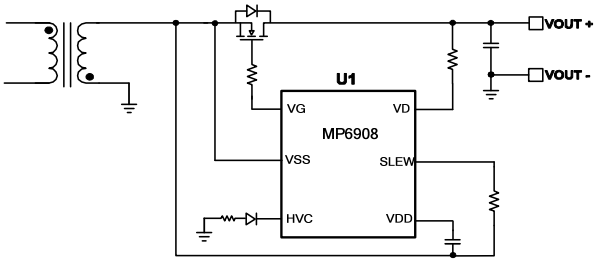


Figure 6-B: High-Side Rectification, VDD Regulated at 9V

HVC works the same as described above when V_{HVC} is below 4.7V since HVC is shorted to VSS (see Figure 7). Here, VDD is generated by V_{DS} and regulated at 5V.

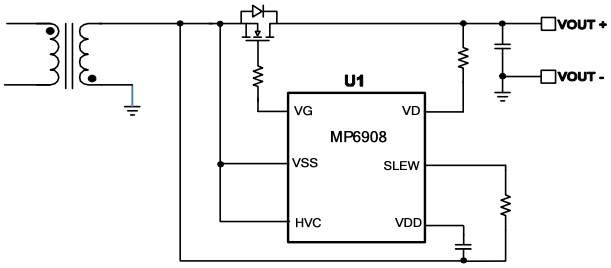


Figure 7: High-Side Rectification, VDD Regulated at 5V

SR MOSFET Selection

Power MOSFET selection is a tradeoff between the $R_{DS(ON)}$ and Q_G. To achieve higher efficiency, the MOSFET with the smaller $R_{DS(ON)}$ is preferred. Typically, Q_G is usually larger with a smaller $R_{DS(ON)}$, which makes the turn-on/turn-off speed lower and leads to larger power loss and driver loss. Because V_{DS} is adjusted at about -40mV during the driving period when the switching current is fairly small, a MOSFET with an $R_{DS(ON)}$ that is too low is not recommended because the gate driver is pulled low when V_{DS} = -I_{SD} x $R_{DS(ON)}$ becomes larger than -40mV. The MOSFET's $R_{DS(ON)}$ does not contribute to the conduction loss. The conduction loss is P_{CON} = -V_{DS} x I_{SD} ≈ I_{SD} x 40mV.

To achieve fairly high use of the MOSFET's $R_{DS(ON)}$, the MOSFET should be turned on completely for at least 50% of the SR conduction period. Calculate V_{DS} with Equation (3):

$$V_{DS} = -I_C \times R_{DS(ON)} = -I_{OUT} / D \times R_{DS(ON)} \le -V_{fwd} \quad (3)$$

Where V_{DS} is drain-source voltage of the MOSFET, D is the duty cycle of the secondary side, I_{OUT} is output current, and V_{fwd} is the forward voltage threshold (~40mV).

Figure 8 shows the typical waveform of a flyback application. Assume it has a 50% duty cycle. The MOSFET's $R_{DS(ON)}$ is recommended to be no lower than ~20/I_{OUT} (mΩ). For example. for a 5A application, the $R_{DS(ON)}$ should be no lower than 4mΩ.

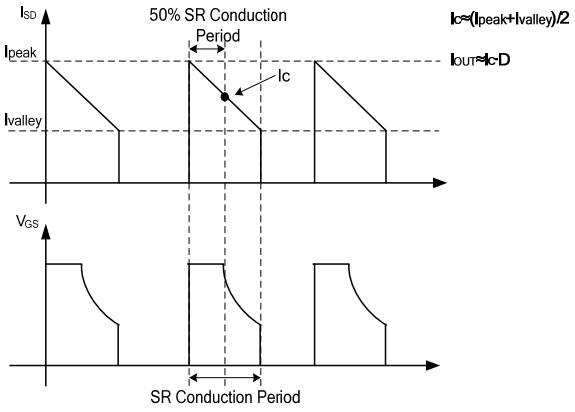


Figure 8: Synchronous Rectification Typical Waveforms in a Flyback Application

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 9, Figure 10, Figure 11, and follow the guidelines below.

Sensing for VD/VSS

1. Make the sensing connection (VD/VSS) as close as possible to the MOSFET (drain/source).
2. Make the sensing loop as small as possible.
3. Keep the IC out of the power loop to prevent the sensing loop and power loop from interrupting each other (see Figure 9).

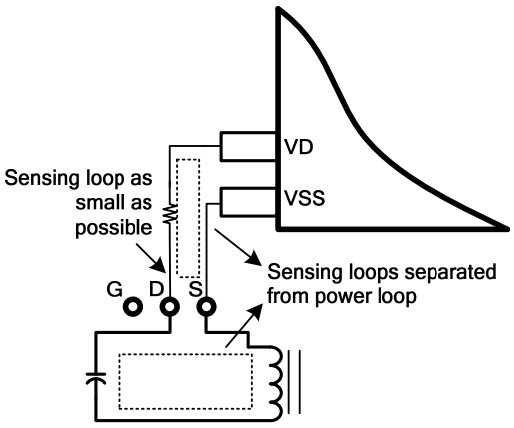


Figure 9: Voltage Sensing for VD/VSS

4. Place a decoupling ceramic capacitor from VDD to PGND close to the IC for adequate filtering.

Gate Driver Loop

1. Make the gate driver loop as small as possible to minimize the parasitic inductance.
2. Keep the driver signal far away from the VD sensing trace on the layout.

Layout Example

Figure 10 shows a layout example of a single layer with a through-hole transformer and a TO220 package SR MOSFET. RSN and CSN are the RC snubber network for the SR MOSFET. The sensing loop (VD and VSS to the SR MOSFET) is minimized and kept separate from the power loop. The VDD decoupling capacitor (C2) is placed beside VDD.

Figure 11 shows another layout example of a single layer with a PowerPAK/SO8 package SR MOSFET, which also has a minimized sensing loop and power loop to prevent the loops from interfering with one another.

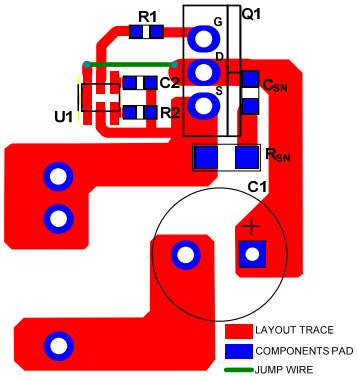


Figure 10: Layout Example with TO220 Package SR MOSFET

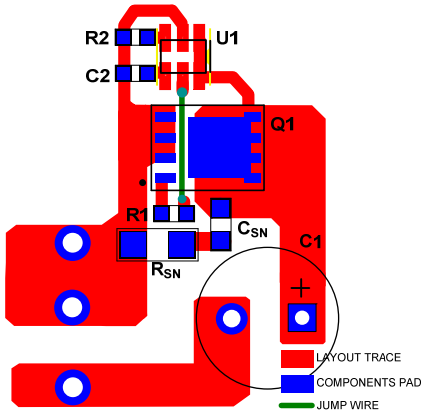
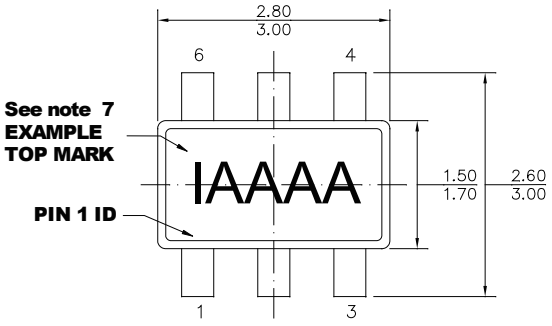


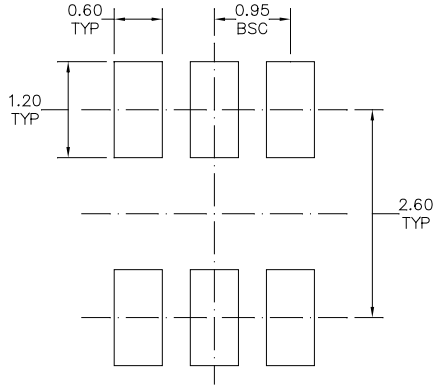
Figure 11: Layout Example with PowerPAK/SO8 SR MOSFET

PACKAGE INFORMATION

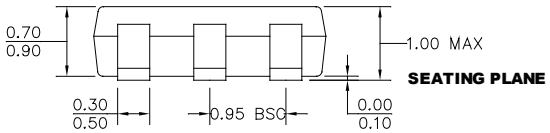
TSOT23-6



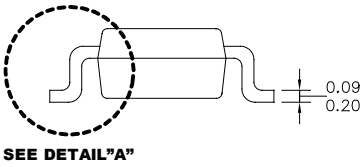
TOP VIEW



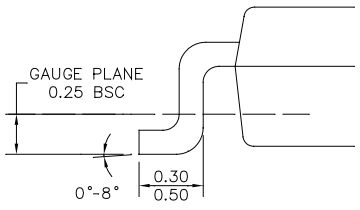
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

Revision History

Revision #	Revision Date	Description	Pages Updated
1.1	05/26/2020	Some min/max specifications are added in the EC table.	Page 3

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