MP8009

Fully Integrated, 802.3af/at Compliant PoE PD Interface with High-Efficiency Flyback/Forward Controller

DESCRIPTION

The MP8009 is an integrated IEEE 802.3af/at PoE compliant powered device (PD) power supply converter. It includes a PD interface and a high-efficiency flyback/forward controller.

The PD interface has all the functions of IEEE 802.3af/at, including detection, 1-event and 2-event classification, 120mA inrush current limit, 840mA operation current limit, and a 100V hot-swap MOSFET.

The flyback/forward controller is specifically designed to be cost-effective. It is a space-saving isolated solution with primary-side regulation (PSR) for flyback applications, and high-efficiency secondary-side regulation (SSR) for active clamped forward applications. It can be used in SSR flyback topologies.

The MP8009 can support a front-end solution for PoE PD applications with a minimal number of external components. It provides Hiccup Protection for Overload Protection (OLP), Short-Circuit Protection (SCP), Over-Voltage Protection (OVP), and Thermal Shutdown. It is available in a QFN-28 (4mmx5mm) package.

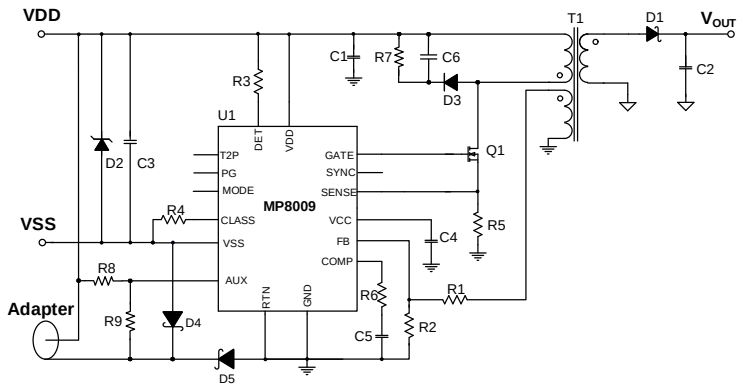
FEATURES

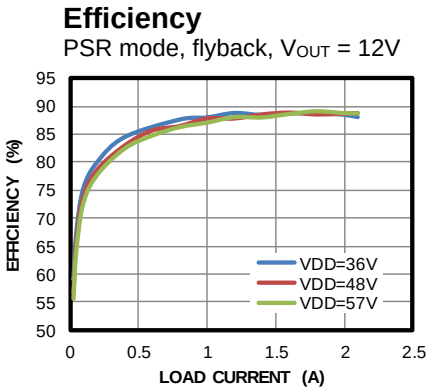
- Compatible with 802.3af/at Specifications
- 100V, 0.48Ω PD Integrated Pass Switch
- 120mA PD Inrush Current
- 840mA PD Operation Current Limit
- Supports >8.5V Auxiliary Adapter Supply
- Supports Flexible Topology Design:
  - Primary-Side Regulation (PSR) for Flyback Applications
  - Secondary-Side Regulation (SSR) for Flyback Applications
  - SSR for Active Clamp Forward Applications
- 2A GATE and 0.8A SYNC Drivers
- 160mV Switching Current-Sense Limit
- Output Diode Compensation in PSR Mode
- 250kHz Fixed Switching Frequency
- EMI Reduction with Frequency Dithering
- Available in a QFN-28 (4mmx5mm) Package

APPLICATIONS

- IEEE 802.3af/at-Compliant Devices
- Security Cameras
- Video Telephones
- WLAN Access Points
- Internet-of-Things (IoT) Devices

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP8009GV	QFN-28 (4mmx5mm)	*See Below*	2

* For Tape & Reel, add suffix –Z (e.g. MP8009GV–Z).

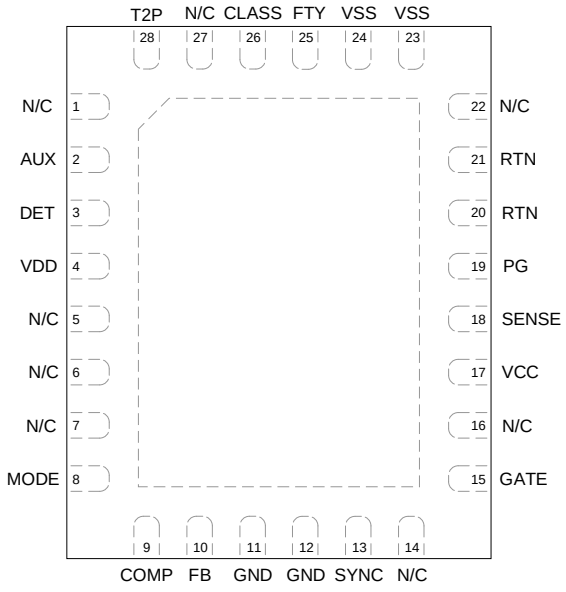
TOP MARKING

MPSYWW
MP8009
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP8009: Part number
LLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-28 (4mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 5, 6, 7, 14, 16, 22, 27	NC	**No connection**. It is recommended to connect the NC pins to GND.
2	AUX	**Auxiliary power input detector.** Use the AUX pin for auxiliary power applications. Drive VDD - AUX above 2.3V to disable the hot-swap MOSFET and CLASS functions. This forces T2P and PG to be active.
3	DET	**Detection.** Connect a 24.9kΩ resistor between VDD and DET for PoE detection.
4	VDD	**Positive power supply terminal for PoE and controller input power rail.**
8	MODE	**PSR/SSR mode and dead time setting.** Float the MODE pin for PSR applications. Connect the MODE pin to GND via a resistor for SSR applications. To set the dead time between GATE and SYNC, see the Work Mode Detection section on page 21.
9	COMP	**Loop compensation pin**. The COMP pin functions as the error amplifier (EA) output in PSR mode. It is internally pulled to 5V through a 10kΩ resistor in SSR mode.
10	FB	**Output voltage feedback and OVP monitor pin.** Connect one resistor divider from the sensing winding to regulate the output voltage in PSR mode. In SSR mode, the internal EA is disabled. FB detects the OVP signal in both PSR and SSR mode. Connect the FB pin to GND if not using the OVP function in SSR mode.
11, 12	GND	**Ground pin.**
13	SYNC	**Synchronous MOSFET gate driver pin.**
15	GATE	**Main MOSFET gate driver pin.**
17	VCC	**DC/DC internal circuit supply pin.** VCC is powered through an internal LDO from VDD. Connect a capacitor between VCC and GND to bypass the internal regulator. The VCC capacitor should be at minimum 1μF for flyback applications, or 4.7μF for forward applications. VCC can be powered from an external power source to reduce internal LDO loss.
18	SENSE	**Current-sense**, **PSR V_{OUT} compensation, and frequency dither setting.** SENSE is the power current sense pin. It can also set the V_{OUT} compensation and frequency dither function by connecting a resistor from the SENSE pin to the power current sense resistor. See the Output Voltage Compensation section on page 23 and the Frequency Dithering section on page 24 for more details.
19	PG	**PD supply power good indicator**. This signal enables the DC/DC converter internally. It is pulled up by an internal current source under high output conditions. It is recommended to float PG in most applications.
20, 21	RTN	**Drain of PD hot-swap MOSFET.** Connect RTN to GND. It is also recommended to connect the exposed thermal pad to GND and RTN for thermal dissipation.
23, 24	VSS	**Negative power supply terminal from PoE input power rail.**
25	FTY	**Factory use only.** FTY must be connected to VSS.
26	CLASS	**Classification.** Connect a resistor from CLASS to VSS to configure the classification current.
28	T2P	**Type-2 PSE indicator.** T2P is an open-drain output. T2P is pulled low to VSS to indicate the presence of a wall adapter or Type-2 PSE.

ABSOLUTE MAXIMUM RATINGS (1)

Pin Voltages with Respect to VSS:

VDD, RTN, DET, T2P, AUX, GND..... .....-0.3V to +100V
CLASS, FTY .....-0.3V to +6.5V

Pin Voltages with Respect to GND: (2)

VDD .....-0.3V to +100V
VCC, GATE, SYNC.....-0.3V to +18V
FB .....-0.5V to +5.5V (3)
MODE, COMP, SENSE .....-0.3V to +5.5V
PG .....-0.3V to +6.5V

Pin Voltages with Respect to VDD:

AUX .....-6.5V to +0.3V (4)

Pin Currents:

T2P sink current..... 10mA
PG sink current 0.5mA (5)
FB sink current..... ±2mA (3)
Continuous power dissipation (T_A = 25°C)
QFN-28 (4mmx5mm).....3.37W (6) (7)
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -55°C to +150°C

Recommended Operating Conditions (9)

Supply voltage (VDD) .....0V to 57V
VCC, GATE SYNC voltage..... 16V
Maximum T2P sink current 5mA
Maximum PG sink current..... 0.4mA (5)
Maximum FB sink current ..... ±1mA (3)
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}	
QFN-28 (4mmx5mm)			
EV8009-V-00A (7)	37	2	°C/W
JESD51-7 (8)	40	9	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) GND must be connected to RTN.
3) FB is clamped by internal circuit. The sink/source current should be limited (see the Output Voltage Setting section on page 28 for more details).
4) When the voltage between the VDD pin and the adapter ground is high, the AUX - VDD voltage may exceed -6.5V if the correct resistor divider is not selected. In this condition, the current should be limited by external resistor (see the Wall Power Adapter Detection Circuit section on page 27 for more details).
5) If PG is externally pulled up above 6.5V, the pull-up current should be limited. See the PG subsection of the Electrical Characteristics section on page 6 for the PG pin voltage rating description.
6) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
7) Measured on EV8009-V-00A, 2-layer, 139mmx41mm PCB.
8) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
9) The device is not guaranteed to function outside of its operating conditions.

ELECTRICAL CHARACTERISTICS

PD INTERFACE

The VDD, CLASS, DET, T2P, and RTN voltages are referred to VSS, and all other pin voltages are referred to GND. GND and RTN are shorted together. VDD - VSS = 48V, VSS = 0V, R_{DET} = 24.9kΩ, R_{CLASS} = 28.7Ω. T_J = -40°C to +125°C (10), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Detection						
Detection on	V_{DET-ON}	V_{DD} rising		1.9		V
Detection off	$V_{DET-OFF}$	V_{DD} rising		11		V
DET leakage current	V_{DET-LK}	V_{DET} = V_{DD} = 57V, measure I_{DET}		0.1	5	µA
Bias current		V_{DD} = 10.1V, float DET pin, not in mark event, measure I_{SUPPLY}			12	µA
Detection current	I_{DET}	V_{DD} = 2.5V, measure I_{SUPPLY}	96	99	102	µA
		V_{DD} = 10.1V, measure I_{SUPPLY}	395	410	425	µA
Classification						
Classification stability timer				90		µs
V_{CLASS} output voltage	V_{CLASS}	13V < V_{DD} < 21V, 1mA < I_{CLASS} < 42mA	1.1	1.16	1.21	V
Classification current	I_{CLASS}	13 ≤ V_{DD} ≤ 21V, guaranteed by V_{CLASS}				
		R_{CLASS} = 578Ω, 13V ≤ V_{DD} ≤ 21V	1.8	2	2.4	mA
		R_{CLASS} = 110Ω, 13V ≤ V_{DD} ≤ 21V	9.9	10.55	11.3	
		R_{CLASS} = 62Ω, 13V ≤ V_{DD} ≤ 21V	17.7	18.7	19.8	
		R_{CLASS} = 41.2Ω, 13V ≤ V_{DD} ≤ 21V	26.6	28.15	29.7	
		R_{CLASS} = 28.7Ω, 13V ≤ V_{DD} ≤ 21V	38.2	40.4	42.6	
Classification lower threshold	V_{CL-ON}	Class regulator turns on, V_{DD} rising	11.8	12.5	13	V
Classification upper threshold	V_{CL-OFF}	Class regulator turns off, V_{DD} rising	21	22	23	V
Classification hysteresis	V_{CL-H}	Low-side hysteresis		0.8		V
		High-side hysteresis		0.5		
Mark event reset threshold	V_{MARK-L}		4.5	5	5.5	V
Max mark event voltage	V_{MARK-H}		11	11.5	12	V
Mark event current	I_{MARK}		0.5	1.5	2	mA
Mark event resistance	R_{MARK}	2-point measure at 7V and 10V			12	kΩ
IC supply current during classification	$I_{IN-CLASS}$	V_{DD} = 17.5V, CLASS floating		220	300	µA
Class leakage current	$I_{LEAKAGE}$	V_{CLASS} = 0 V, V_{DD} = 57V			1	µA
PD UVLO						
VDD turn-on threshold	$V_{DD-VSS-R}$	V_{DD} rising	35	37.5	40	V
VDD turn-off threshold	$V_{DD-VSS-F}$	V_{DD} falling	29	31	33	V
VDD UVLO hysteresis	$V_{DD-VSS-HYS}$		4.9			V
IC supply current during operation	I_{IN}			450		µA

ELECTRICAL CHARACTERISTICS *(continued)*

PD INTERFACE

The VDD, CLASS, DET, T2P, and RTN voltages are referred to VSS, and all other pin voltages are referred to GND. GND and RTN are shorted together. VDD - VSS = 48V, VSS = 0V, R_{DET} = 24.9kΩ, R_{CLASS} = 28.7Ω. T_J = -40°C to +125°C (10), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Pass Device and Current Limit						
On resistance	R_{ON-RTN}	I_{RTN} = 600mA		0.48		Ω
Leakage current	I_{RTN-LK}	V_{DD} = V_{RTN} = 57V		1	15	μA
Current limit	I_{LIMIT}	V_{RTN} = 1V	720	840	920	mA
Inrush current limit	I_{INRUSH}	V_{RTN} = 2V		120		mA
Inrush current termination		V_{RTN} falling		1.2		V
Inrush to operation mode delay	t_{DELAY}		80	100		ms
Current foldback threshold		V_{RTN} rising		10		V
Foldback deglitch time		V_{RTN} rising to inrush current foldback		1		ms
T2P						
T2P output low voltage		I_{T2P} = 2mA, respect to VSS		0.1	0.3	V
T2P output high leakage current		V_{T2P} = 48V			1	μA
AUX						
AUX high threshold voltage (11)		Respect to VDD			-2.3	V
AUX low threshold voltage (11)		Respect to VDD	-0.6			V
AUX leakage current		V_{DD} - V_{AUX} = 6V			2	μA
VDD UVLO rising for adapter power		VDD - AUX = 3V, ramp VDD - VSS from low to high until T2P/PG signal response		7.25	8.5	V
VDD UVLO falling for adapter power		VDD - AUX = 3V, ramp VDD - VSS from high to low until T2P/PG signal reset		5		V
PG						
PG output high voltage		PG pin floating		5.5		V
Source current capability		PG is logic high, pull the PG pin down to 0V		30		μA
PG pull-down resistance		PG is logic low, pull the PG pin up to 1V		715		kΩ
PG threshold for DC/DC switching	V_{PG-R}	Start switching	1.93	2	2.07	V
PG hysteresis for DC/DC switching	V_{PG-HYS}	Stop switching		0.2		V

ELECTRICAL CHARACTERISTICS *(continued)*

PD INTERFACE

The VDD, CLASS, DET, T2P, and RTN voltages are referred to VSS, and all other pin voltages are referred to GND. GND and RTN are shorted together. VDD - VSS = 48V, VSS = 0V, R_{DET} = 24.9kΩ, R_{CLASS} = 28.7Ω. T_J = -40°C to +125°C (10), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PG high threshold for DC/DC micropower	V_{PG-H}	Start internal logic			1.0	V
PG lower threshold for DC/DC micropower	V_{PG-L}	Stop internal logic	0.4			V
PG enable DC/DC delay		PG on to GATE output		500		µs
PD Thermal Shutdown						
Thermal shutdown temperature (12)	T_{PD-SD}			150		°C
Thermal shutdown hysteresis (12)	T_{PD-HYS}			20		°C

ELECTRICAL CHARACTERISTICS *(continued)*

CONTROLLER

The VDD, CLASS, DET, T2P, and RTN voltages are referred to VSS, and all other pin voltages are referred to GND. GND and RTN are shorted together. VDD - VSS = 48V, VSS = 0V, R_{DET} = 24.9kΩ, R_{CLASS} = 28.7Ω. T_J = -40°C to +125°C (10), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply and UVLO						
VDD UVLO rising threshold	V_{DD-R}	V_{DD} rising, start charging V_{CC}	4.5	5.5	6.5	V
VDD UVLO falling threshold	V_{DD-F}	V_{DD} falling	3.8	4.8	5.8	V
VCC regulation voltage	V_{CC}	Load = 0mA to 20mA		8.5		V
VCC dropout voltage	$V_{CC-DROP}$	V_{DD} = 8V, I_{VCC} = 10mA		1.5		V
VCC UVLO rising threshold	V_{CC-R}	V_{DD} > V_{DD-R}, V_{CC} rising	5.4	5.7	6.0	V
VCC UVLO falling threshold	V_{CC-F}	V_{DD} > V_{DD-R}, V_{CC} falling	5.0	5.3	5.6	V
Quiescent current	I_Q	MODE pin floating, V_{FB} = -0.1V, SENSE = 100mV, COMP = 0V, I_Q = I_{DD} - I_{COMP}, GATE and SYNC floating		1250		µA
		MODE = 0V, V_{COMP} = 0V, GATE and SYNC floating, I_Q = I_{DD} - I_{COMP}		900		µA
Voltage Feedback						
FB reference voltage	V_{REF}	T_J = 25°C	1.98	2	2.02	V
		T_J = -40°C to +125°C	1.97	2	2.03	V
FB leakage current	I_{FB}	V_{FB} = 2V		10	50	nA
FB OVP threshold	V_{FBOVP}		120%	125%	130%	V_{REF}
OVP hiccup off time				340		ms
Minimum diode conduction time for FB sample	t_{SAMPLE}			0.5	0.6 (13)	µs
Regulation compensation current into FB		V_{SENSE} = 50mV, $R_{SENSE-GND}$ = 3.3kΩ (14)		2.7		µA
		V_{SENSE} = 50mV, $R_{SENSE-GND}$ = 6.8kΩ (14)		5.4		µA
		V_{SENSE} = 50mV, $R_{SENSE-GND}$ = 12.7kΩ (14)		10.8		µA
Error Amplifier						
Error amplifier transconductance	G_{EA}	MODE floating, V_{FB} is ±50mV from V_{REF}, V_{COMP} = 1.5V		0.59		mA/V
Amplifier maximum source current	I_{EA}	MODE floating, V_{COMP} = 1.5V, V_{FB} = 1.9V		-110		µA
Amplifier maximum sink current	I_{EA}	MODE floating, V_{COMP} = 1.5V, V_{FB} = 2.1V		110		µA

ELECTRICAL CHARACTERISTICS *(continued)*

CONTROLLER

The VDD, CLASS, DET, T2P, and RTN voltages are referred to VSS, and all other pin voltages are referred to GND. GND and RTN are shorted together. VDD - VSS = 48V, VSS = 0V, R_{DET} = 24.9kΩ, R_{CLASS} = 28.7Ω. T_J = -40°C to +125°C (10), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
COMP high voltage	V_{COMP}	MODE floating, V_{FB} = 1.9V		4		V
		MODE = 0V, float COMP		5		
COMP internal pull-up resistor		SSR mode		10		kΩ
Soft Start						
Internal soft-start time	t_{SS}	When MODE floating, test FB from 0V to 2V, When MODE = 0V, test COMP from 1.5V to 3.5V		4.7		ms
Current Sense						
Maximum current sense limit	$I_{LIMIT-MAX}$		140	160	180	mV
Low threshold current limit	$I_{LIMIT-MIN}$	In PSR mode	33	36	39	mV
SCP limit			240	300	360	mV
Current leading-edge blanking time	t_{LEB}			250		ns
Current-sense amplifier gain	G_{CS}			11		V/V
SENSE input bias current		V_{SENSE} = 160mV		10	50	nA
PWM switching						
Switching frequency	f_{SW}		225	250	275	kHz
Minimum foldback frequency in PFM mode		In PSR mode, COMP = 0V		30		kHz
Mode, Dead Time, Dither, V_{OUT} Compensation Setting (MODE and SENSE Pins)						
MODE pin detection current	I_{MODE}		35	40	45	μA
SENSE pin detection current	I_{SENSE}		90	100	110	μA
MODE pin and SENSE pin detection period	t_{MODE} t_{SENSE}			200		μs
MODE pin and SENSE pin detection threshold voltage (15)	V_{MODE} V_{SENSE}	Voltage level 1 range			0.15	V
		Voltage level 2 range	0.25		0.4	V
		Voltage level 3 range	0.55		0.85	V
		Voltage level 4 range	1.1		1.5	V
		Voltage level 5 range	2.2			V
GATE driver signal						
GATE driver impedance (source)	I_{GATE}	I_{GATE} = -20mA		2		Ω
GATE driver impedance (sink)	I_{GATE}	I_{GATE} = 20mA		1.7		Ω
GATE source current capability (12)		V_{CC} = 8.5V, GATE = 10nF, test gate rising speed		2		A

ELECTRICAL CHARACTERISTICS *(continued)*

CONTROLLER

The VDD, CLASS, DET, T2P, and RTN voltages are referred to VSS, and all other pin voltages are referred to GND. GND and RTN are shorted together. VDD - VSS = 48V, VSS = 0V, R_{DET} = 24.9kΩ, R_{CLASS} = 28.7Ω. T_J = -40°C to +125°C (10), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
GATE sink current capability (12)		V_{CC} = 8.5V, GATE = 10nF, test gate falling speed		1.7		A
GATE output high voltage	V_{GATE}		V_{CC} - 0.05			V
GATE output low voltage	V_{GATE}				0.05	V
Minimum GATE on time	t_{ON-MIN}			250		ns
GATE maximum duty cycle	D_{MAX}			70		%
SYNC driver signal						
SYNC driver impedance (source)	I_{SYNC}	I_{GATE} = -20mA		5		Ω
SYNC driver impedance (sink)	I_{SYNC}	I_{GATE} = 20mA		2		Ω
SYNC source current capability (12)		V_{CC} = 8.5V, SYNC = 10nF, test SYNC rising speed		0.8		A
SYNC sink current capability (12)		V_{CC} = 8.5V, SYNC = 10nF, test SYNC falling speed		1.2		A
SYNC output high voltage	V_{SYNC}		V_{CC} - 0.05			V
SYNC output low voltage	V_{SYNC}				0.05	V
Protection						
Overload protection hiccup on time (12)				4.8		ms
Overload protection hiccup off time (12)				340		ms
Thermal shutdown temperature (12)	T_{SD}			150		°C
Thermal shutdown hysteresis (12)	T_{HYS}			20		°C

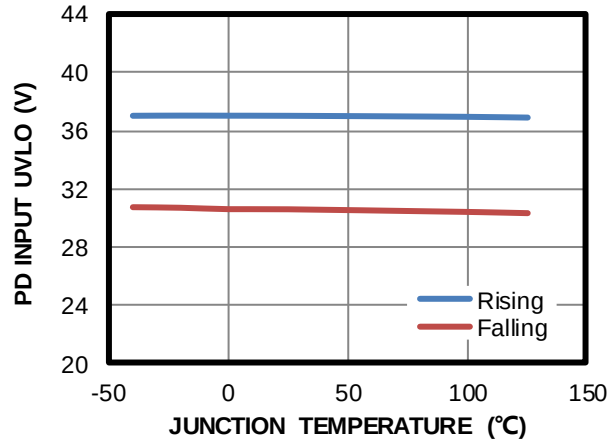
Notes:

10) Guaranteed by over-temperature correlation. Not tested in production.
11) If VDD - AUX > 2.3V, the IC enables adapter input. If VDD - AUX < 0.6V, the IC enable PSE input.
12) Guaranteed by sample characterization. Not tested in production.
13) >0.7µs minimum output-diode conduction time is recommended.
14) $R_{SENSE-GND}$ is the resistance from the SENSE pin to GND. It includes the current-sense resistor from the MOSFET source to GND and the resistor from the MOSFET source to the SENSE pin.
15) See Table 2 on page 22 and Table 3 on page 24 to see different voltage level options.

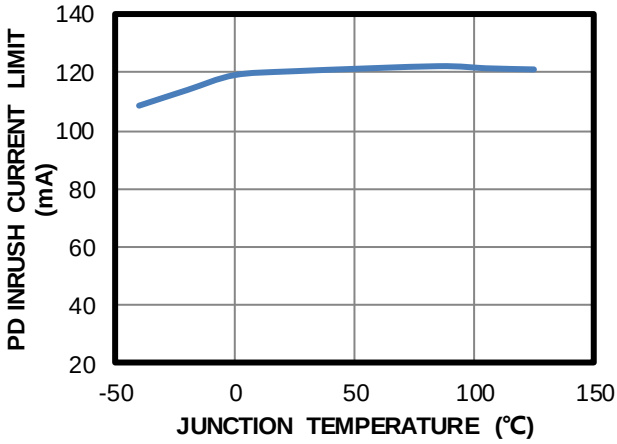
TYPICAL CHARACTERISTICS

V_{DD} - V_{SS} = 48V, T_A = 25°C, unless otherwise noted.

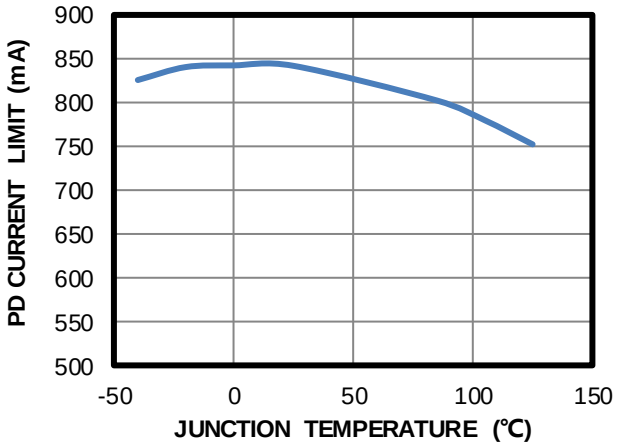
PD Input UVLO vs. Junction Temperature



PD Inrush Current Limit vs. Junction Temperature

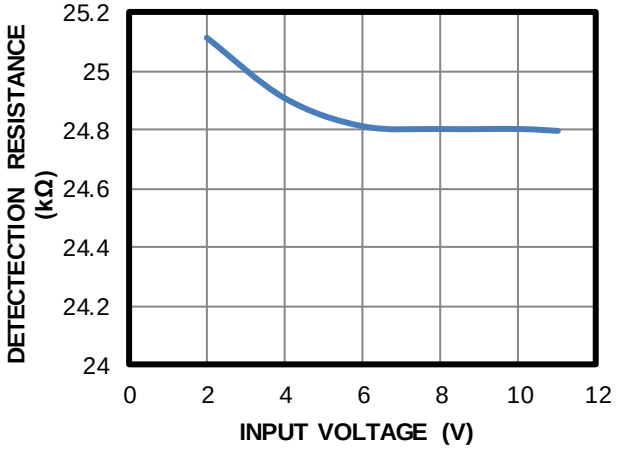


PD Current Limit vs. Junction Temperature

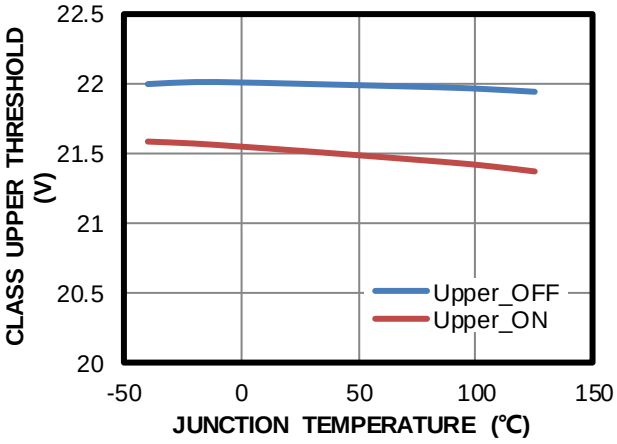


Detection Resistance vs. Input Voltage

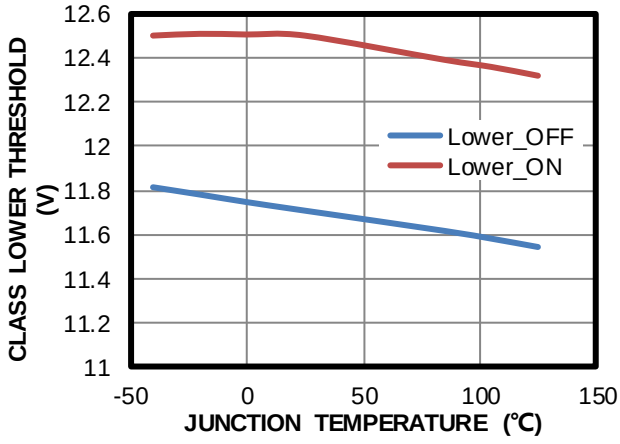
R_{DET} = 24.9kΩ



CLASS Upper Threshold vs. Junction Temperature



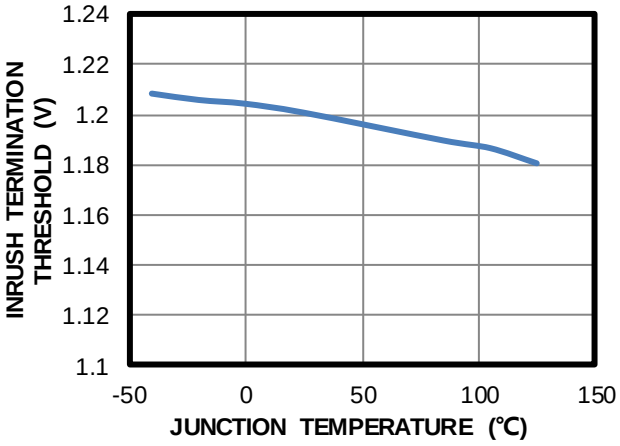
CLASS Lower Threshold vs. Junction Temperature



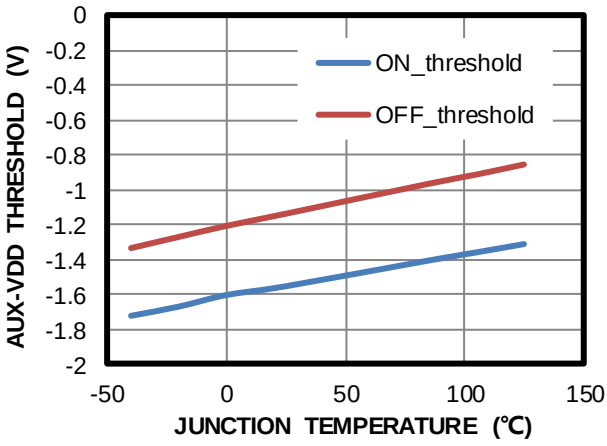
TYPICAL CHARACTERISTICS *(continued)*

V_{DD} - V_{SS} = 48V, T_A = 25°C, unless otherwise noted.

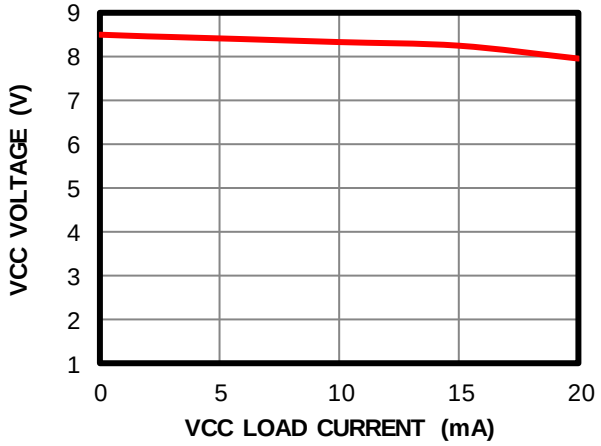
Inrush Current Termination Threshold vs. Junction Temperature



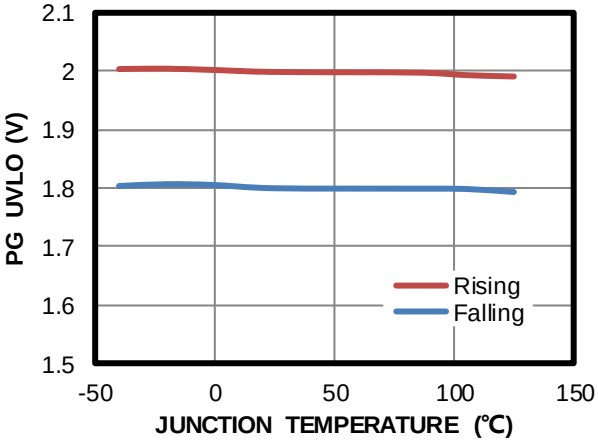
AUX-VDD Threshold vs. Junction Temperature



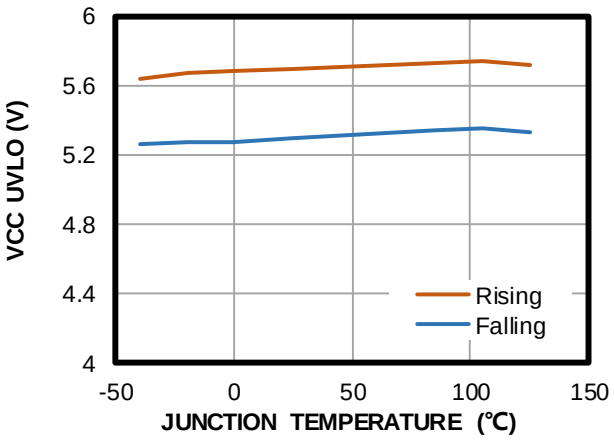
VCC Load Regulation



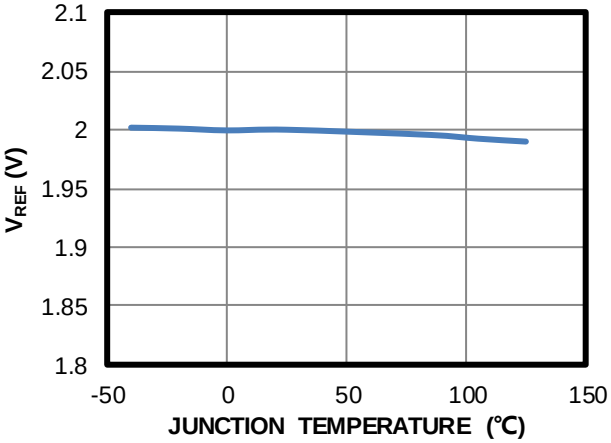
PG UVLO vs. Junction Temperature



VCC UVLO vs. Junction Temperature



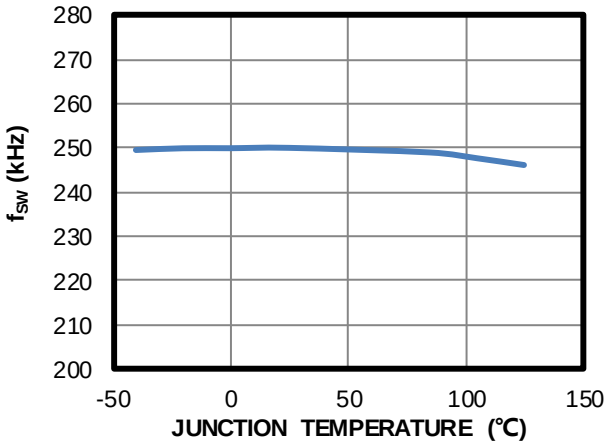
Reference Voltage vs. Junction Temperature



TYPICAL CHARACTERISTICS *(continued)*

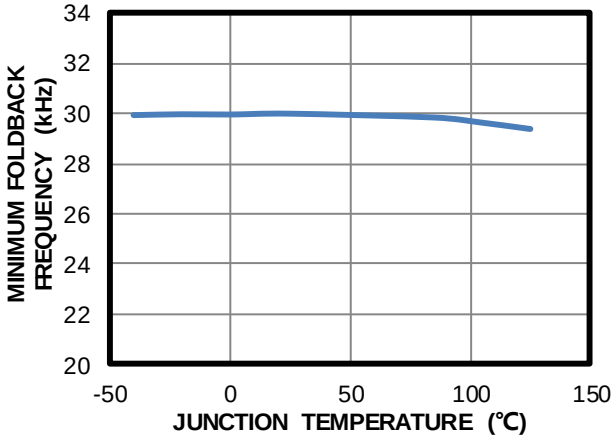
V_{DD} - V_{SS} = 48V, T_A = 25°C, unless otherwise noted.

Frequency vs. Junction Temperature

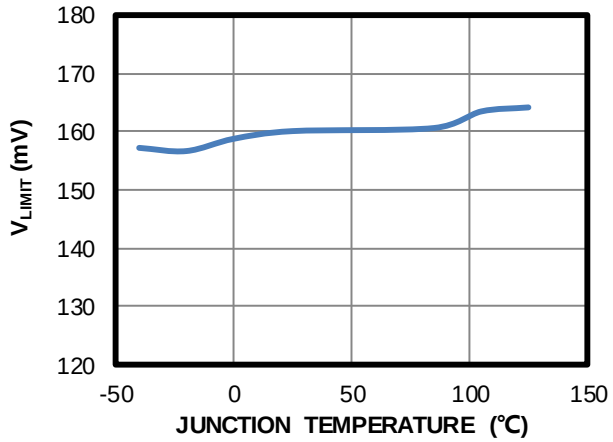


Minimum Foldback Frequency vs. Junction Temperature

PSR mode

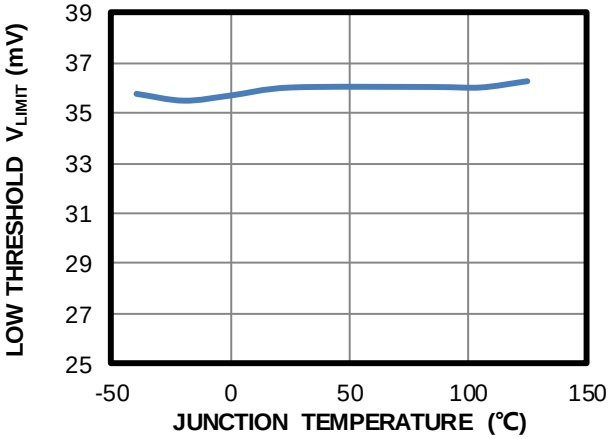


Current Limit vs. Junction Temperature

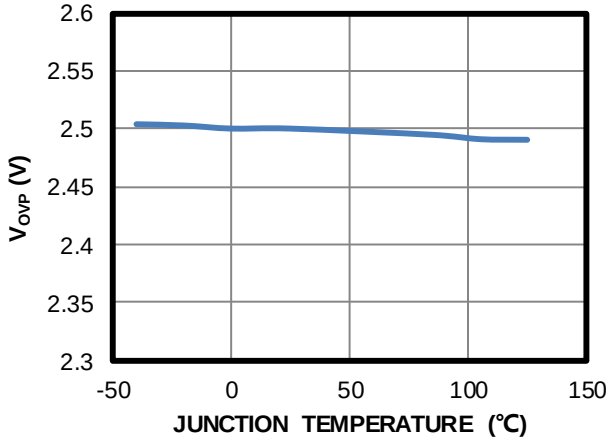


Low Threshold Current Limit vs. Junction Temperature

PSR mode



OVP Threshold vs. Junction Temperature

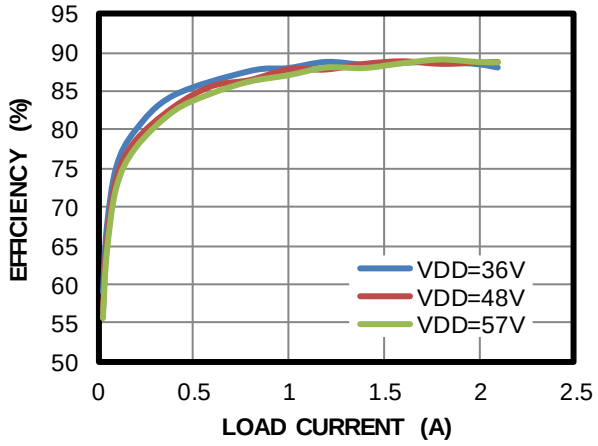


TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} - V_{SS} = 48V, V_{OUT} = 12V, I_{OUT} = 2.1A, T_A = 25°C, unless otherwise noted.

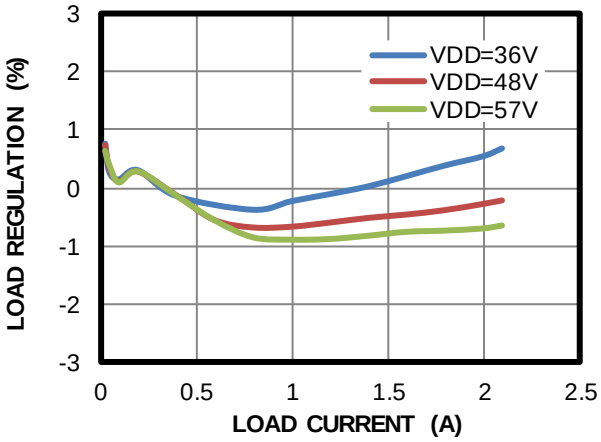
Efficiency

PSR mode, flyback, V_{OUT} = 12V



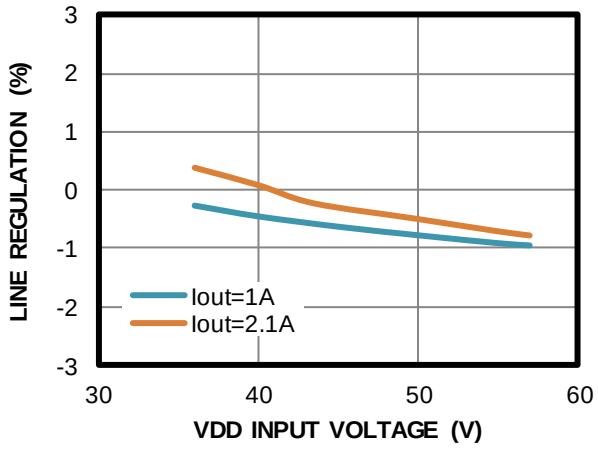
Load Regulation

PSR mode, flyback, V_{OUT} = 12V, R_{FBH} = 100kΩ, $R_{SENSE-GND}$ = 6.8kΩ



Line Regulation

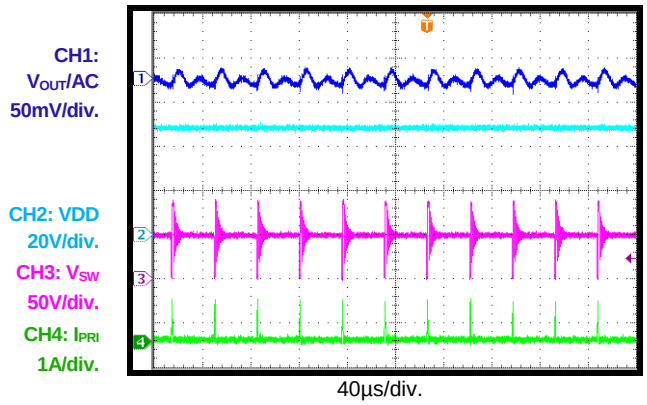
PSR mode, flyback, V_{OUT} = 12V, R_{FBH} = 100kΩ, $R_{SENSE-GND}$ = 6.8kΩ



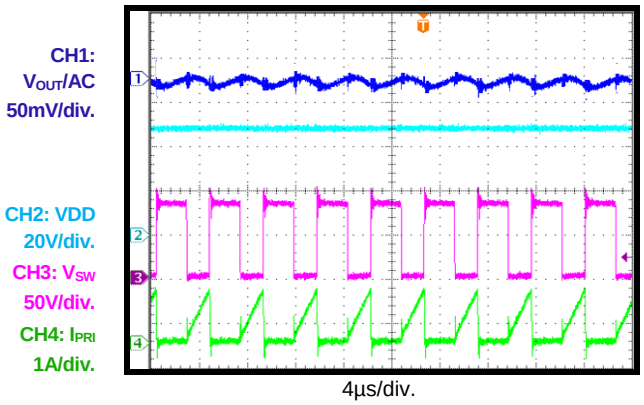
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} - V_{SS} = 48V, V_{OUT} = 12V, I_{OUT} = 2.1A, set in PSR flyback mode, T_A = 25°C, unless otherwise noted.

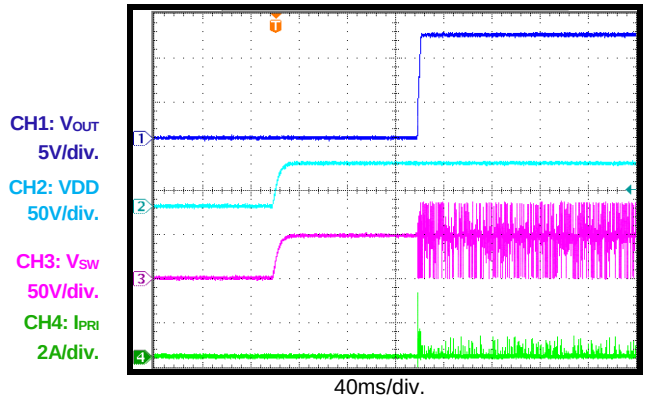
Steady State
I_{OUT} = 30mA



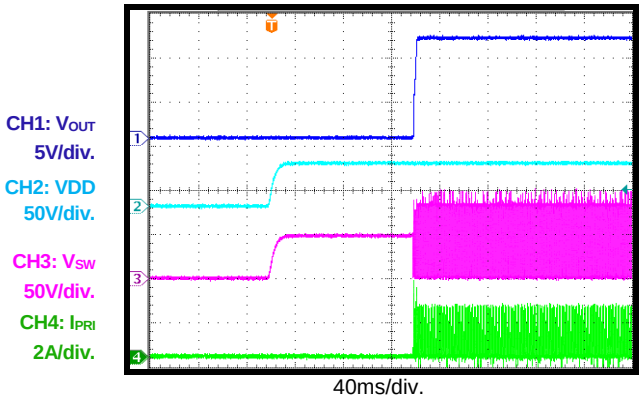
Steady State
I_{OUT} = 2.1A



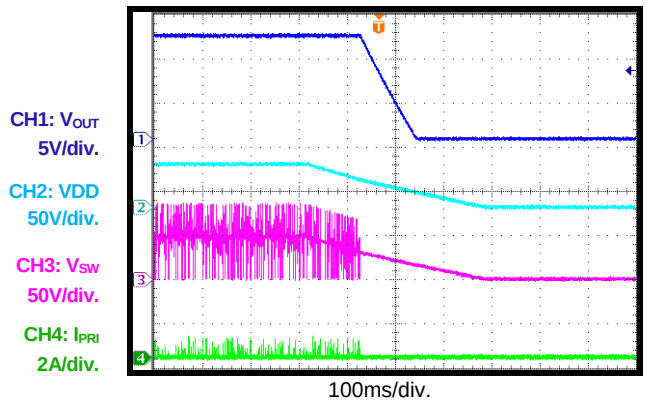
Start-Up through VDD
I_{OUT} = 30mA



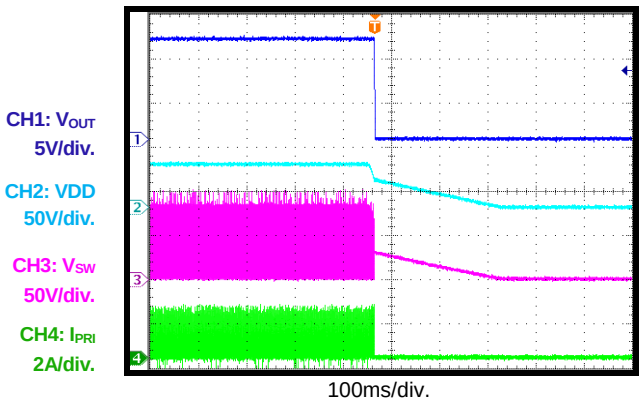
Start-Up through VDD
I_{OUT} = 2.1A



Shutdown through VDD
I_{OUT} = 30mA



Shutdown through VDD
I_{OUT} = 2.1A

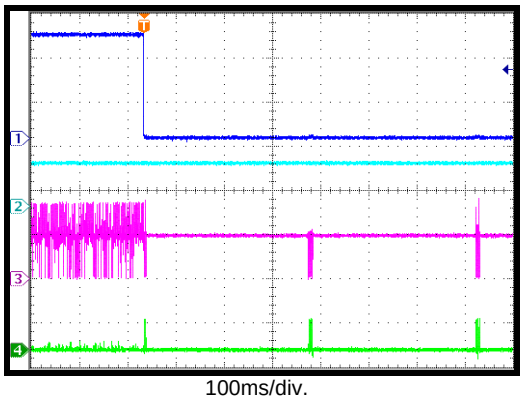


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} - V_{SS}= 48V, V_{OUT} = 12V, I_{OUT} = 2.1A, set in PSR flyback mode, T_A = 25°C, unless otherwise noted.

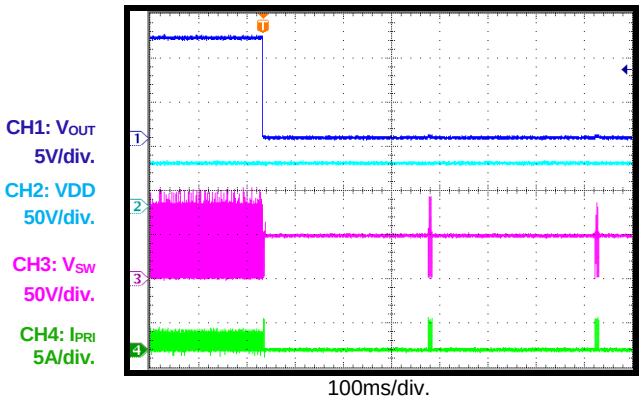
SCP Entry

I_{OUT} = 30mA to short



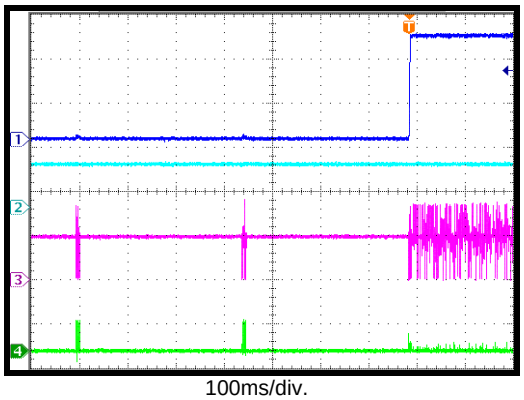
SCP Entry

I_{OUT} = 2.1A to short



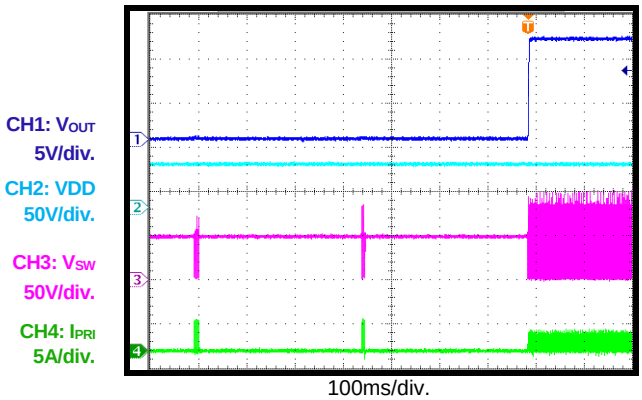
SCP Recovery

I_{OUT} = short to 30mA



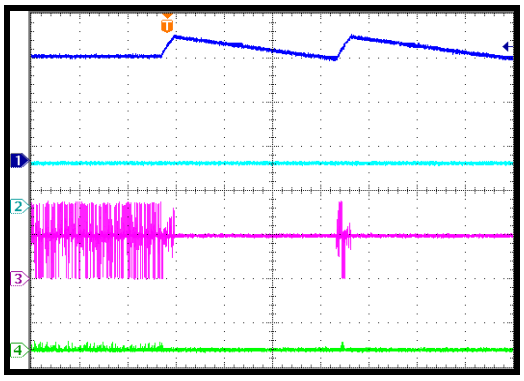
SCP Recovery

I_{OUT} = short to 2.1A



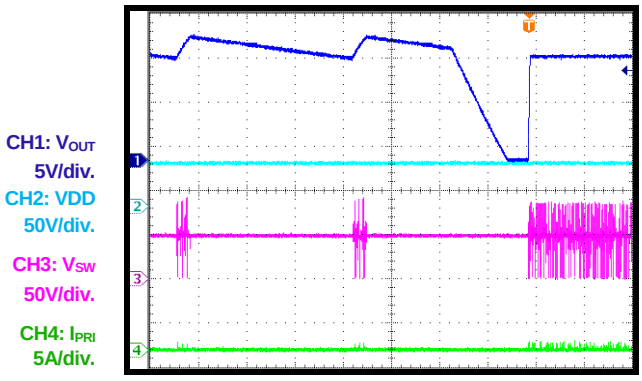
OVP Entry

I_{OUT} = 30mA to 2mA



OVP Recovery

I_{OUT} = 2mA to 30mA

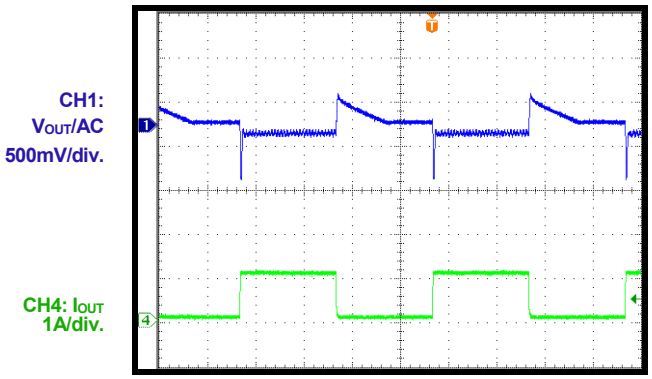


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} - V_{SS}= 48V, V_{OUT} = 12V, I_{OUT} = 2.1A, set in PSR flyback mode, T_A = 25°C, unless otherwise noted.

Load Transient

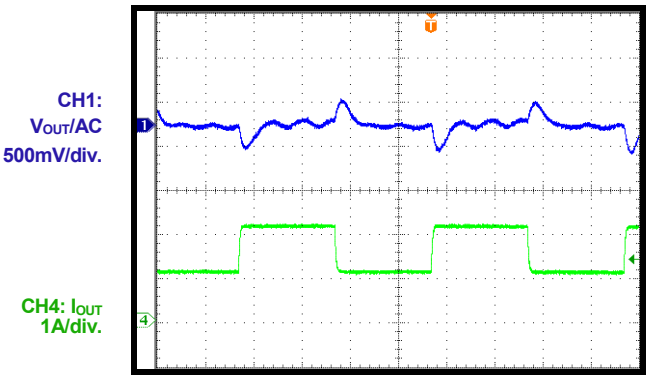
I_{OUT} = 30mA to 1.25A, I_{RAMP} = 50mA/µs,
R_{FBH} = 100kΩ, $R_{SENSE-GND}$ = 6.8kΩ



10ms/div.

Load Transient

I_{OUT} = 1.25A to 2.5A, I_{RAMP} = 50mA/µs,
R_{FBH} = 100kΩ, $R_{SENSE-GND}$ = 6.8kΩ



1ms/div.

FUNCTIONAL BLOCK DIAGRAM

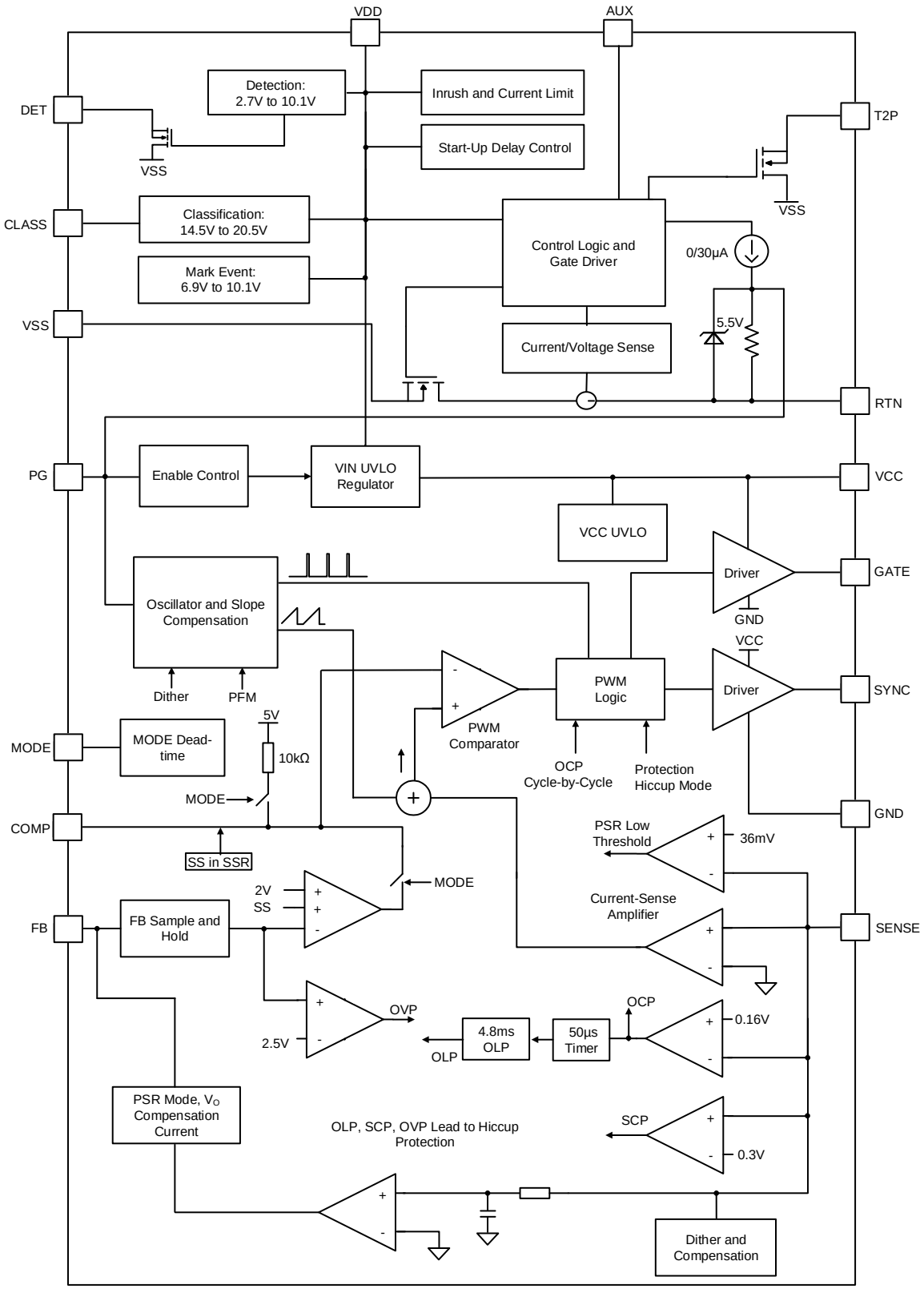


Figure 1: Functional Block Diagram

OPERATION

Compared to IEEE802.3af, the IEE802.3at standard establishes a higher power allocation for Power over Ethernet (PoE) while maintaining backward compatibility with existing IEEE 802.3af systems. Power-sourcing equipment (PSE) and power devices (PD) are distinguished as Type-1 (compliant with IEEE 802.3af power levels) or Type-2 (compliant with IEEE 802.3at power levels). The IEEE 802.3af/at standard establishes a method of communication between PD and PSE with detection, classification, and mark events.

The MP8009 is an integrated PoE solution with an IEEE 802.3af/at PD interface and a peak current mode flyback controller. Along with the PSE, the MP8009 operates as a safety device. The device supplies voltage only when the power-sourcing equipment recognizes a unique and tightly specified resistance at the end of an unknown length of Ethernet cable. Once it is powered from the PSE, the MP8009 regulates the output voltage based on the application circuit setting. Figure 2 shows the typical PD interface power operation sequence.

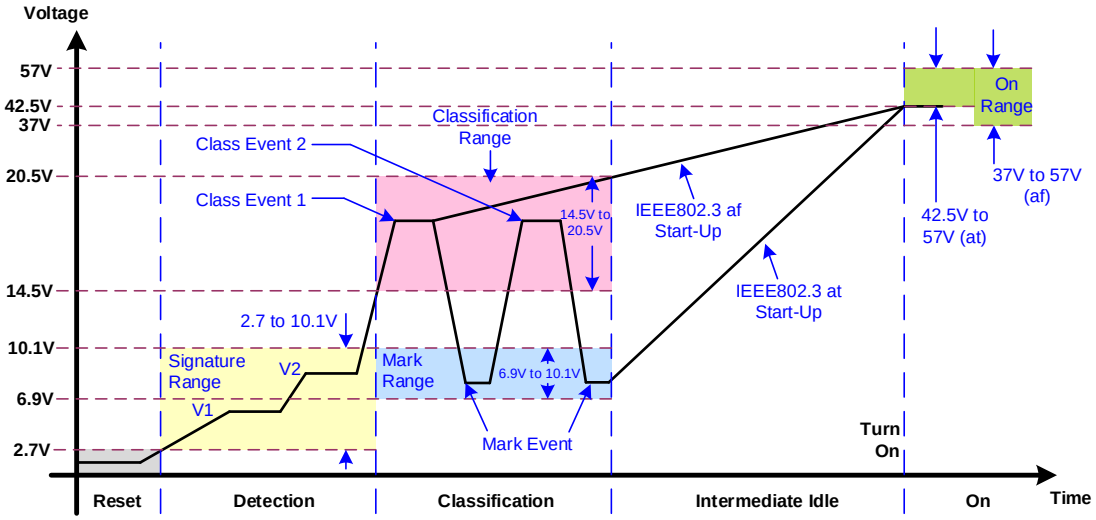


Figure 2: PD Interface Operation Description

Detection

A resistor (R_{DET}) connected between DET and VDD is presented as a load to the PSE in detection mode. The PSE applies two “safe” voltages (between 2.7V and 10.1V) to PD while measuring the change in the drawn current to determine the load resistance. It is recommended to place a 24.9kΩ (±1%) resistor between VDD and DET to present one correct signature resistance. The valid signature resistance detected on the power interface (PI) is between 23.7kΩ and 26.3kΩ.

The detection resistance detected on the PI is the result of the input bridge resistance that is in series with the VDD load. The input bridge resistance is partially cancelled by the MP8009’s effective leakage resistance during detection.

Classification

Classification mode can specify the expected load range of the device being powered by the PSE so that the PSE can distribute power to as many loads as possible within its maximum current capability. Classification mode is active when the voltage is between 14.5V and 20.5V. The MP8009 presents a current in classification mode, which is set by a resistor on the CLASS pin (see Table 1).

Table 1: CLASS Resistor Selection

Class	Max Input Power to PD (W)	Classification Current (mA)	R_{CLASS} (Ω)
0	12.95	2	578
1	3.84	10.55	110
2	6.49	18.7	62
3	12.95	28.15	41.2
4	25.5	40.4	28.7

2-Event Classification

The MP8009 can be used as a Type-1 PD, with classes 0, 1, 2, and 3 (see Table 1). It can also distinguish class 4 with 2-event classification.

In 2-event classification, the Type-2 PSE reads the power classification twice. Figure 2 shows an example of 2-event classification. The first classification event occurs when the PSE provides a voltage between 14.5V and 20.5V to the MP8009, and the MP8009 presents a class-4 load current. The PSE then drops the input voltage into the marked voltage range (between 6.9V and 10.1V) to signal the first mark event. The MP8009 presents a load current between 0.5mA to 2mA in the marked voltage range.

The PSE repeats this sequence, signaling the second classification and second mark event. The PSE then applies power to the MP8009, which charges up the DC/DC input capacitor (C_{BULK}, or C1 in the Typical Application on page 1) with a controlled inrush current. When C_{BULK} is fully charged, T2P presents an active low signal with respect to VSS after t_{DELAY}. The T2P output becomes inactive when the MP8009 input voltage (V_{DD}) falls below the under-voltage lockout (UVLO) threshold (see Figure 3).

PD Interface Under-Voltage Lockout (UVLO) and Current Limit

When the PD is powered by PSE and VDD exceeds the turn-on threshold, the hot-swap MOSFET begins passing a limited current (I_{INRUSH}) to charge the downstream DC/DC converter's input capacitor (C_{BULK}). The start-up charging current is about 120mA.

If RTN drops below 1.2V, the hot-swap current limit changes to 840mA. After UVLO is initiated and t_{DELAY} is complete, the MP8009 asserts the PG signal. The PG signal rises high only after the hot-swap switch turns on completely. Then PG enables the DC/DC controller.

If VDD - VSS drops below the UVLO falling threshold, the hot-swap MOSFET is disabled.

If the output current overloads, the internal pass MOSFET current limit function is enabled, and the voltage difference between RTN and VSS rises. If V_{RTN} exceeds 10V for longer than 1ms (or exceeds 20V), the current limit reverts to the inrush value, and PG drops low simultaneously.

Figure 3 shows the current limit function, and PG and T2P work logic during start-up when the power supply is PSE.

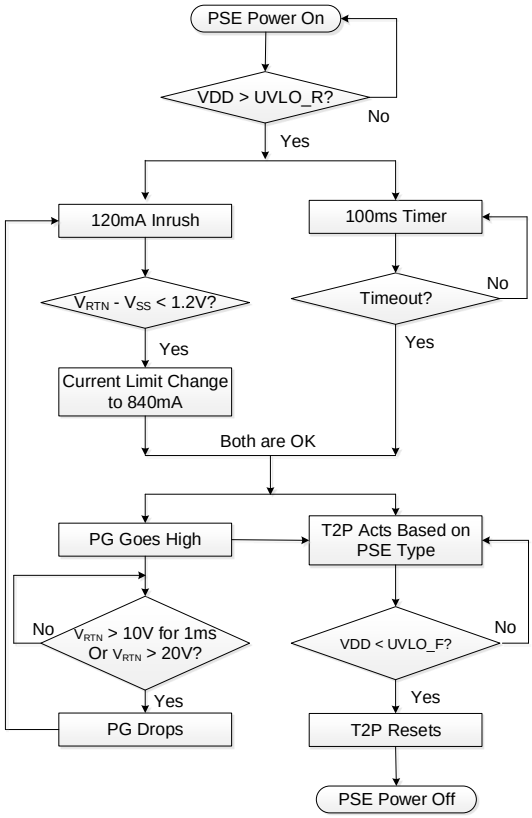


Figure 3: Start-Up Sequence

Wall Power Adapter Detection and Operation

The MP8009 uses wall power adapter detection for applications where an auxiliary power source (e.g. a wall adapter) powers the device (see Figure 4). Once the input voltage (V_{DD} - V_{SS}) exceeds 8.5V, the MP8009 enables wall adapter detection. The wall power adapter detection resistor divider is connected from VDD to the negative terminal of the adapter. A Zener diode (D_{ADP3}) is added for a more accurate hysteresis. There is a -2.3V reference voltage from AUX to VDD for adapter detection. The adapter is detected when the AUX voltage is triggered, calculated with Equation (1):

$$V_{DD} - V_{AUX} = (V_{ADP} - V_{DADP3}) \times \frac{R_{ADPUP}}{R_{ADPUP} + R_{ADPDOWN}} > 2.3V \quad (1)$$

Where V_{ADP} is the adapter voltage, V_{DADP3} is the Zener diode voltage, and R_{ADPUP} and $R_{ADPDOWN}$ are the AUX resistor dividers from the adapter power.

If the applied adapter voltage exceeds the designed adapter voltage, the VDD - VAUX voltage is high. If the applied voltage between VDD and AUX exceeds 6.5V, some current may flow out through the AUX pin. Design the external resistor (R_{ADPUP} / $R_{ADPDOWN}$, or an RT resistor connected from the resistor divider to AUX) to limit the AUX pin's current. The external resistor limits the current by assuming the VDD - AUX voltage is 6.5V (the AUX pin voltage rating) for the calculation. The current flowing out of the AUX pin should be 3mA below the external resistor limit.

To ensure that the MP8009 is stable when working with adapter power, place a Schottky diode (D_{APD1}) between the negative terminal of the adapter and VSS. D_{APD2} can be added to block the reverse current between the adapter and the PSE power source. When a wall adapter is detected, the internal MOSFET between RTN and VSS turns off, classification current is disabled, and T2P becomes active. The PG signal is active when the adapter power is detected, so that it can enable the downstream DC/DC controller, even if the input hot-swap MOSFET is disabled (see Figure 4).

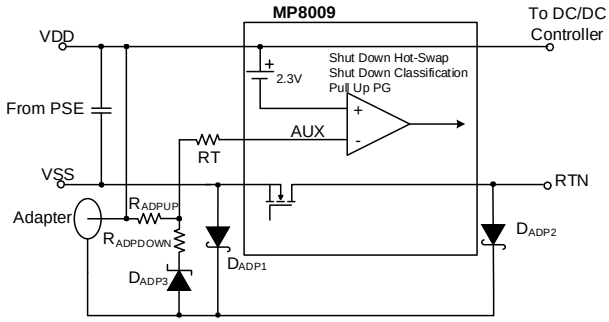


Figure 4: Adapter Power Detection

Power Good (PG) Control

The PG signal is driven by the internal current source. After t_{DELAY} starts counting when UVLO is triggered, and RTN drops to 1.2V (or a wall power adapter is detected), the PG signal is pulled high to indicate the power condition. Then the DC/DC controller is enabled. Figure 3 shows the PG logic when the device is powered from the PSE. PG goes high if the adapter is detected under any condition.

PG can be pulled up through external resistor, but the pull-up resistor should be carefully considered to limit the current flowing into the PG pin. Place one internal Zener diode on the PG pin to clamp the PG voltage. Ensure that the diode limits the current flowing into PG below 0.4mA.

DC/DC CONTROLLER OPERATION

Start-Up and Power Supply

The MP8009's DC/DC controller features a high-voltage, internal start-up circuit. When VDD - GND exceeds 5.5V, the capacitor at VCC is charged through the internal LDO. Generally, V_{CC} is regulated to 8.5V (if VDD is sufficiently high), and the VCC UVLO threshold is typically 5.7V. With the exception of the VCC UVLO threshold, the DC/DC controller has an EN UVLO threshold that is typically 2V. When VCC is charged above its 5.7V threshold, and the EN pin is high, the DC/DC controller begins to operate.

VCC can be powered from the transformer auxiliary winding to reduce IC power loss after the DC/DC controller starts switching. The auxiliary power must exceed the VCC regulation voltage to override the internal LDO. There is one internal reverse blocking circuit that allows V_{CC} to exceed V_{DD} if VCC has biased power. Due to the pin ratings, the VCC power should stay below 16V.

If V_{DD} is below 8.5V and V_{CC} cannot be regulated to 8.5V, the internal high-voltage VCC LDO has a 1.5V voltage drop. This means that the DC/DC controller can work when the input is as low as 8V.

Work Mode Detection

After the DC/DC controller is enabled, it outputs a 40μA current to the MODE pin to detect the resistor setting. If the MODE pin's voltage exceeds 2.2V, the controller works in primary-side regulation (PSR) mode, and the internal error amplifier (EA) is enabled. If the MODE pin is connected to GND through a resistor, the controller works in secondary-side regulation (SSR) mode (see Table 2 on page 22). In SSR mode, the internal EA is disabled while COMP is pulled up to the internal 5V power source through a 10kΩ resistor.

In PSR mode, the V_{OUT} feedback signal is detected by auxiliary winding from the FB pin, and the DC/DC controller reduces the frequency while keeping it above 30kHz under

light load. In SSR mode, the V_{OUT} feedback signal is detected through the COMP pin, and the controller maintains a fixed frequency. Meanwhile, the peak current can be regulated by the COMP voltage until it triggers power-save mode (PSM).

After the controller is enabled, there is a 500µs period before it starts switching. The work mode, dead time, dither, and V_{OUT} compensation settings can be detected by the DC/DC controller during this period (see Table 2).

Table 2: MODE Pin Configurations

MODE to GND Resistance (kΩ)			Work Mode	Dead Time (ns)
Min	Typ (1%)	Max		
0	0	3.3	SSR	100
7.32	7.5	8.2	SSR	150
16	16.9	18.7	SSR	200
32.4	32.4	33	SSR	300
64.9	Float	Float	PSR	150

The MODE pin can set the device to PSR or SSR mode. It can also configure the dead time between the GATE and SYNC pins.

The MODE pin detection current lasts about 200µs. Generally, it is sufficient to connect one resistor between MODE and GND. In a noisy environment, connect a capacitor from the MODE pin to GND to provide filtering. Use a maximum 100pF capacitor so that the MODE pin voltage can rise to a steady state before the DC/DC controller detects it.

PWM Operation

The MP8009 DC/DC controller can be set to a flyback or forward topology. In flyback topology, the external N-channel MOSFET is turned on at the beginning of each cycle, forcing the current in the transformer to increase.

The current through the MOSFET can be sensed. When the sum of the SENSE signal and slope compensation signal exceeds the voltage set by the COMP pin, the external MOSFET turns off.

The transformer current then transmits energy from the primary-side winding to the secondary-side winding, and charges the output capacitor through the Schottky diode.

The transformer's primary-side current is controlled by the COMP voltage, which is controlled by the output feedback voltage. This means that the output voltage controls the transformer current to satisfy the load.

In forward topology, the energy is transferred from the primary-side to secondary-side winding when the primary-side N-channel MOSFET turns on. The primary-side peak current is controlled by the COMP voltage. The COMP voltage is controlled by the external shunt voltage regulator integrated circuit (TL431) and optocoupler feedback. See the Voltage Control section below to set the output voltage feedback.

Voltage Control

Primary-Side Regulation (PSR) Mode

Unlike traditional flyback applications with optoisolator feedback, the MP8009's DC/DC controller can detect the auxiliary winding voltage from the FB pin during the secondary-side output diode conduction period.

Assume that the secondary-side winding acts as the master, and the auxiliary winding acts as the slave. When the secondary-side diode is conducting, the FB voltage can be calculated with Equation (2):

$$V_{FB} = \frac{N_A}{N_S} \times (V_{OUT} + V_{DOF}) \times \frac{R_{FBL}}{R_{FBH} + R_{FBL}} \quad (2)$$

Where V_{DOF} is the output diode forward drop voltage, V_{OUT} is the output voltage, N_A and N_S are the turns of the auxiliary winding and the secondary-side output winding, respectively, and R_{FBH} and R_{FBL} are the resistor dividers for FB sampling.

Figure 5 shows the FB sample control in discontinuous conduction mode (DCM).

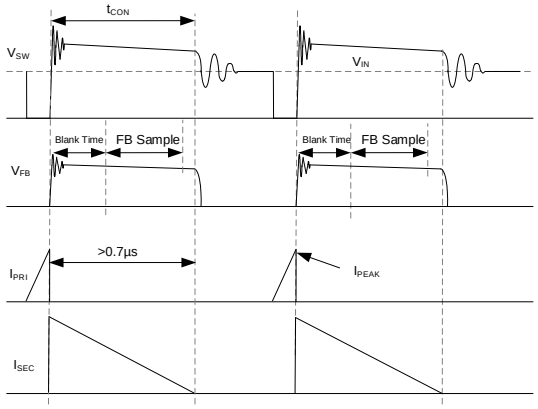


Figure 5: DCM FB Sample

Figure 6 shows the FB sample control in continuous conduction mode (CCM).

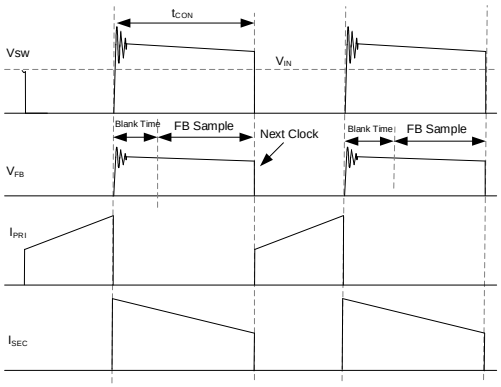


Figure 6: CCM FB Sample

The DC/DC controller regulates the primary-side MOSFET switching to ensure that the V_{SENSE} current signal exceeds 36mV (typical value), and then starts sampling the auxiliary winding voltage after the power MOSFET turns off. A 300ns blanking time is inserted to avoid spike ringing due to the inductance leakage.

To guarantee a sufficient FB sample period, the output diode current conduction time (t_{CON}) under light loads (before the diode current drops to 0A in each cycle) should be longer than 600ns. Generally, it is recommended to design the transformer to ensure that t_{CON} is longer than 700ns, and that V_{SENSE_PK} = 33mV. The DC/DC controller GATE signal also provides a 1.2µs minimum off time. To guarantee a sufficient FB sample time when the DC/DC controller works with a high duty cycle, a 70% maximum duty limits this time.

During the FB sense period, the FB signal is sent into the negative input of the error amplifier (EA), and the FB signal is held after the sense window elapses. The EA output is generated on the COMP pin. This output controls the transformer peak current to match it to the output regulation requirement.

Secondary-Side Regulation (SSR) Mode

The MP8009's DC/DC controller can also be set to secondary-side regulation (SSR) mode. In SSR mode, the V_{OUT} signal is the feedback to COMP pin through one optocoupler. The primary-side regulation (PSR) FB voltage detection function is disabled, so FB should be connected to GND.

Under light-load conditions, the controller maintains a fixed frequency in SSR mode. If the COMP voltage drops, then the peak current drops low until it reaches the power-save mode (PSM) threshold. The 36mV minimum current limit does not work in SSR mode.

In SSR mode, the DC/DC controller can support both flyback and forward topologies. In PSR mode, it can only support flyback topology.

Output Voltage Compensation

In PSR mode, the auxiliary winding waveform reflects the secondary-side winding voltage. However, the output voltage differs from the output winding voltage due to the output diode voltage drop, as well as the power winding resistance. The dropout voltage varies when the conducted current changes.

The resistor connected from the SENSE pin to GND can set the dropout voltage's compensation gain when the current varies. The current-sense signal is filtered internally, and controls the current sinking the FB pin based on the average voltage from the SENSE pin.

There are three types of current gains based on the average SENSE voltage or FB sinking current (see Table 3). A sinking current on FB leads to a voltage drop on FB's high-side feedback resistor, which compensates V_{OUT} (see Figure 7).

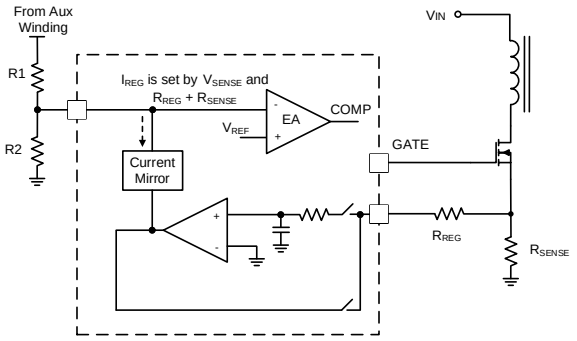


Figure 7: Output Voltage Compensation

In SSR mode, this voltage compensation function is disabled.

Frequency Dithering

The DC/DC controller integrates one frequency dithering circuit to minimize EMI emissions. During steady state, the frequency is fixed internally, but the frequency dithering circuit is added to the configured frequency with 1.5kHz modulation.

In PSR mode, the frequency dithering is fixed at ±6% of the switching frequency. In SSR mode, the frequency dithering can be configured to be ±3%, ±6%, or ±9%, based on the resistor connected from the SENSE pin to GND.

Table 3 shows the dither and V_{OUT} compensation options.

Table 3: SENSE Pin Configurations

SENSE to GND Resistance (kΩ) (14)			PSR Mode		SSR Mode
Min	Typ (1%)	Max	Dither Range (kHz)	I_{FB} / V_{SENSE} Ratio (μA/mV)	Dither Range (kHz)
0	0	1.3	0	0	0
3	3.3	3.6	±15	0.054	±7.5
6.2	6.8	7.5	±15	0.108	±15
12.7	12.7	13	±15	0.216	±22.5
24.9	25.5	28	±15	0	±22.5

The SENSE pin detection current lasts about 200μs after start-up. Generally, it is sufficient to connect one resistor between SENSE and GND. In a noisy environment, connect a capacitor from the SENSE pin to GND to provide filtering.

Current-Sense and Over-Current Protection (OCP)

The MP8009's DC/DC controller is a peak current mode flyback/forward controller. The current through the external MOSFET can be sensed through a sensing resistor that is connected in series with the MOSFET source. The voltage sensed on the SENSE pin is then amplified and fed to the high-speed current comparator for current mode control. The current comparator takes this sensed voltage (plus the slope compensation) as one of its inputs, then compares it to the COMP voltage. If the amplified current signal is above the COMP voltage (V_{COMP}), the comparator outputs low, turning off the power MOSFET.

If the voltage on the SENSE pin exceeds the current-limit threshold voltage (typically 160mV), the controller turns off the GATE output for that cycle. This output stays off until the internal oscillator starts the next cycle and senses the current again. Cycle-by-cycle current limiting limits the MOSFET's current.

Error Amplifier (EA)

In PSR mode, the DC/DC controller senses the FB voltage during the flyback period with a pulsed FB signal. Then the FB signal is held and fed into the error amplifier (EA). The EA regulates V_{COMP} based on the FB signal. Then V_{COMP} controls the peak transformer current to regulate the output voltage.

In SSR mode, the internal EA is disabled and the COMP pin is pulled up by an internal resistor. An external optocoupler can be connected to the COMP pin for output voltage signal feedback.

Light-Load Control

Under light-load conditions in PSR mode, the COMP voltage decreases to regulate the lower peak transformer current. If the sensed peak current signal is below 36mV, the controller does not reduce the transformer current, and instead reduces the frequency. As a result, the transferred energy decreases and the output voltage is regulated.

The DC/DC controller limits the minimum frequency above 30kHz in light-load PSR mode. This helps the MP8009 detect the output voltage with a 30kHz frequency and avoid audible noise. This minimum frequency requires some load to maintain the output voltage, or else V_{OUT} rises and triggers over-voltage-protection (OVP).

Under light-load conditions in SSR mode, the DC/DC controller maintains a fixed frequency. COMP continues to drop until it reaches the power-save mode (PSM) threshold.

Over-Voltage Protection (OVP)

The DC/DC controller provides over-voltage protection (OVP). If the voltage at FB exceeds 125% of V_{REF}, the controller shuts off the gate driving signal and immediately enters hiccup mode. The controller restarts after 340ms, and resumes normal operation if the fault is removed. Connect FB to GND if not using the OVP function.

To avoid mistriggering due to the oscillation of the inductance leakage and parasitic capacitance, OVP sampling has a blanking time.

Overload Protection (OLP)

The DC/DC controller limits the peak current cycle by cycle under over-current protection (OCP) conditions. If the load continues increasing after triggering switching OCP, then the output voltage decreases and the peak current triggers OCP every cycle.

The DC/DC controller sets overload detection by monitoring the SENSE pin voltage. Once the internal soft start finishes, overload protection (OLP) is enabled. If an OCP signal is detected, and lasts more than 4.8ms, the controller turns off the GATE driver. After 340ms delay, the controller restarts with a new start-up cycle.

During OLP, one 50μs one-shot timer is activated, and it remains active for 50μs after one OCP pulse. That means if there is one OCP pulse in a 50μs period, the controller registers this as OCP. If the condition disappears before 4.75ms, the DC/DC controller resumes normal operation.

Short-Circuit Protection (SCP)

When the output is shorted to ground, the MP8009 works in OCP mode. The current is limited cycle by cycle, and OLP may be triggered.

If the peak current cannot be limited by a 160mV SENSE voltage in every cycle due to the minimum gate on time, the current may become unstable and the transformer may saturate. If the monitored SENSE voltage reaches 300mV, the GATE pin turns off and runs hiccup mode immediately with a 340ms off time.

If the short circuit is removed, the output voltage recovers after the next restart cycle with a 340ms delay.

Soft Start (SS)

The DC/DC controller provides soft start (SS) by charging an internal capacitor with a current source. During the soft-start period, the SS signal ramps up slowly. If a commanded shutdown, thermal shutdown, or protection condition occurs, then the soft-start capacitor is discharged completely.

In PSR mode, the SS signal clamps the FB reference voltage. The FB reference soft-start time is typically 4.7ms (between 0V and 2V).

In SSR mode, the SS signal clamps the COMP voltage until COMP reaches the switching current. The soft-start signal continuously ramps up at the same rate. The COMP ramp time is about 4.7ms (between 1.5V and 3.5V).

Minimum On Time

The transformer parasitic capacitance and the gate driver signal induce a current spike on the sense resistor when the power MOSFET turns on. The controller uses a 250ns leading-edge blanking period to avoid falsely terminating the switching pulse. During this blanking period, the current-sense comparator is disabled, and the gate driver cannot switch off.

Gate Driver

The DC/DC controller integrates one high-current gate driver for the primary-side N-channel MOSFET. The high-current gate driver provides strong driving capability and benefits from MOSFET selection. If the external MOSFET (Q_G) is low, the switching speed should be low to improve EMI. It is recommended to use a series resistance of 5Ω or greater.

The controller also integrates one SYNC driver pin. It can be used to turn the synchronous switch off when it is high, and to turn the synchronous switch on when it is low. Figure 8 shows the phase and dead time relationship between GATE and SYNC.

After the IC turns off due to UVLO or a protection, both the GATE and SYNC pins keep a low voltage level.

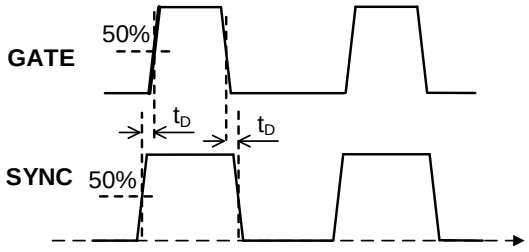


Figure 8: GATE and SYNC Driver

Transformer Inductance Considerations

In primary-side regulation (PSR) mode, the DC/DC controller samples V_{OUT} during the flyback time, so the secondary diode conduction time (with a minimum peak current controlled by the 33mV minimum current-sense limit) should be longer than 0.7μs. The transformer inductance should satisfy the relationship estimated with Equation (3):

$$L_{PRI} \geq (V_{OUT} + V_{DOF}) \times \frac{N_P}{N_S} \times 0.7\mu s \times \frac{R_{SENSE}}{33mV} \quad (3)$$

Where L_{PRI} is the transformer's primary inductance, and V_{DOF} is the output rectifier diode's forward voltage drop.

In SSR mode, there is no inductance limit, but it is recommended to set the peak current high enough to avoid triggering PSM logic. If the system is designed for CCM, PSM may cause a higher V_{OUT} ripple, especially in sync mode forward topology.

Over-Temperature Protection (OTP)

Thermal shutdown is implemented to prevent the chip from thermal runaway. The MP8009 has a separate temperature monitor circuit for the PD and DC/DC power controller.

The controller's thermal protection does not affect the PD interface, but the PD temperature protection turns off both the PD and controller. When the temperature drops below the recovery threshold, the MP8009 starts up again and resumes normal operation.

APPLICATION INFORMATION

Selecting the Detection Resistor

In detection mode, a resistor should be connected between the DET and VDD pins to act as a load for the PSE. The resistance is calculated as ΔV / ΔI, and should range between 23.7kΩ and 26.3kΩ. Use a typical value of 24.9kΩ for the detection resistor.

Selecting the Classification Resistor

To distribute power to as many loads as possible from the PSE, place a resistor between the CLASS and VSS pins to classify the PD power level, which draws a fixed current set by the classification resistor. Table 1 on page 19 shows how to select a classification resistor to supply power to PD. The typical voltage on the CLASS pin is 1.16V in the classification range, and produces 47mW of power loss on the CLASS resistor, even under class 4 conditions.

Protection TVS Setting

To limit the input transient voltage within the absolute maximum ratings, a transient voltage suppressor (TVS) diode must be placed across the rectified voltage (V_{DD} - V_{SS}). An SMAJ58A (or equivalent) diode is recommended for general indoor applications. Outdoor transient levels or special applications require additional protection.

Selecting the PD Input Capacitor

A 0.05μF to 0.12μF input bypass capacitor (from VDD to VSS) is required to meet IEEE 802.3at/af standard specifications. Generally, it is recommended to use a 0.1μF, 100V ceramic capacitor.

Wall Power Adapter Detection Circuit

When an auxiliary power source (e.g. a wall power adapter) powers the device, the resistor dividers (R_{ADPUP} and $R_{ADPDOWN}$) and diode (D_{ADP3}) should be selected to satisfy Equation (1) on page 20 for optimal wall power adapter detection (see Figure 9).

R_{ADPUP} should be about 3kΩ to balance the power loss and the D_{ADP1} / D_{ADP2} leakage current discharge. The R_T resistor limits the AUX current below 3mA when V_{ADP} is high. The minimum R_T value can be estimated with Equation (4):

$$R_T = \frac{\frac{(V_{ADP} - V_{DADP3}) \times R_{ADPUP}}{R_{ADPUP} + R_{ADPDOWN}} - 6.5}{3} \quad (4)$$

Where R_T is in kΩ.

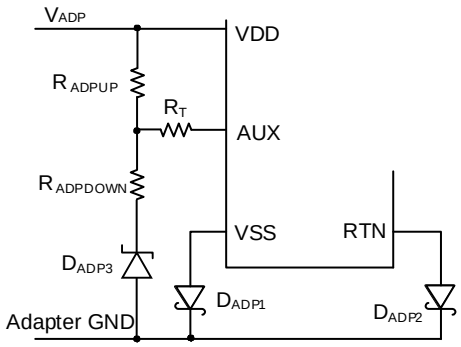


Figure 9: Wall Adapter Detection Circuit

It is recommended to make D_{ADP1} a small package Schottky diode with a 100V voltage rating (e.g. BAT46W). The voltage rating of D_{ADP2} must also be at least 100V, and the current rating must exceed the load current. A low voltage drop Schottky diode (e.g. STPS2H100) is recommended to reduce conduction power loss.

Power Good (PG) Indicator Signal Setting

The MP8009 integrates one power good (PG) indicator. PG is pulled high through an internal pull-up current source when the logic is high; therefore, PG enables the DC/DC controller without any external pull-up circuit. When PG is in a logic low state, the internal pull-up current is disabled and PG is pulled low through an internal resistor.

T2P Indicator Connection

The T2P pin is an active low, open-drain output that indicates the presence of a Type-2 PSE or a wall adapter. An optocoupler can interface the T2P pin to the circuitry on the secondary side of the converter (see Figure 10). It is recommended to use a high-gain optocoupler and a high-impedance (e.g. CMOS) receiver.

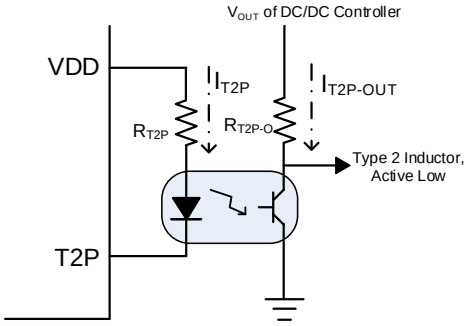


Figure 10: T2P Indicator Circuit

Consider the T2P sinking current (typically 2mA), T2P output low voltage (0.1V), and diode forward voltage drop. Choose R_{T2P} = 23.7kΩ to match the typical 48V input. Assume the DC/DC controller's V_{OUT} is 12V. In this example, choose R_{T2P-O} = 20kΩ based on the CRT, even if it varies with temperature, LED biased current, and aging.

If an LED can light up from VDD to T2P to indicate whether a Type-2 PSE is available, then R_{T2P} can have a higher resistance to match the LED's maximum current and reduce power loss.

Output Voltage Setting

In the MP8009's DC/DC controller, there are two feedback modes: primary-side regulation (PSR) and secondary-side regulation (SSR).

In PSR mode, the converter detects the auxiliary winding voltage from the FB pin. R_{FBH} and R_{FBL} are the resistor dividers for feedback sampling (see Figure 11).

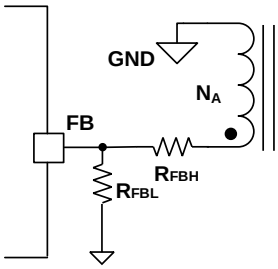


Figure 11: Feedback Sampling in PSR Mode

When the primary-side power MOSFET turns off, the auxiliary winding voltage is proportional to the output winding. The output voltage is then estimated with Equation (5):

$$V_{OUT} = \frac{V_{REF} \times (R_{FBH} + R_{FBL})}{R_{FBL}} \times \frac{N_S}{N_A} - V_{DOF} \quad (5)$$

Where N_S is the transformer's number of secondary-side winding turns, N_A is the transformer's number of auxiliary winding turns, V_{DOF} is the output rectifier diode forward drop, and V_{REF} is the reference voltage on the FB pin.

When the main power MOSFET turns on, the auxiliary winding voltage is negative and the FB voltage is limited by the internal circuit. Then the current flowing out of the FB pin can be calculated with Equation (6):

$$I_{FB} = \frac{1}{R_{FBH}} \times (\frac{V_{IN} \times N_A}{N_P}) \quad (6)$$

R_{FBH} should high enough to limit the FB negative current below 1mA. Due to FB's parasitic capacitance, R_{FBH} should be lower than 100kΩ.

In SSR mode, the output voltage is set by TL431. If TL431's reference voltage is 2.5V, and the expected output voltage is 12V, then the upper and lower divider resistor ratio is 3.8. Then TL431 generates an amplified signal and controls the DC/DC controller's COMP pin through an optocoupler (e.g. PC357). COMP controls the current, and then V_{OUT} is regulated based on the feedback signal.

Work Mode Setting

Once enabled, the DC/DC controller outputs a 40μA current to the MODE pin to detect the MODE resistance. If the MODE pin voltage exceeds 2.2V, the controller works in PSR or SSR mode. The MODE pin can configure the dead time between the GATE and SYNC pins (see Table 2 on page 22).

VCC Power Supply Setting

The VCC voltage (V_{CC}) is regulated by the internal LDO from VDD. V_{CC} is typically regulated at 8.5V. It is recommended to place a decoupling capacitor between VCC and GND.

In flyback mode, the VCC capacitor is recommend to be at minimum 1μF. VCC can also be powered by the transformer auxiliary winding to reduce high-voltage LDO power loss (see Figure 12).

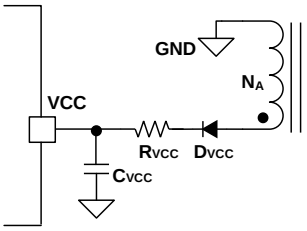


Figure 12: Flyback VCC from N_A Winding

The auxiliary winding supply voltage can be estimated with Equation (7):

$$V_{CC} = \frac{N_A}{N_S} \times (V_{OUT} + V_{DOF}) - V_{DVCCF} \quad (7)$$

Where V_{DVCCF} is the D_{VCC} voltage drop from the auxiliary winding.

In forward mode, the VCC capacitor should be 4.7µF at minimum. VCC can also be powered by the transformer auxiliary winding (see Figure 13).

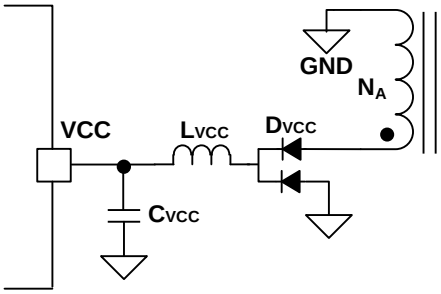


Figure 13: Forward V_{CC} from N_A Winding

The auxiliary winding supply voltage can be calculated with Equation (8):

$$V_{CC} = \frac{N_A}{N_S} \times V_{OUT} \quad (8)$$

V_{CC} should be below 16V.

V_{OUT} Compensation and Frequency Dithering Setting

The SENSE pin can set the output voltage compensation and frequency dithering function. Once enabled, the MP8009 DC/DC controller outputs a 100µA current to the SENSE pin to detect the SENSE resistance. Based on the resistance, the controller determines the compensation type and the frequency dithering type (see Table 3 on page 24).

V_{OUT} compensation is only enabled in PSR mode.

Current-Sense Resistor Setting

The MP8009's DC/DC controller is a peak current mode flyback/forward controller. The current through the external MOSFET can be sensed through a sensing resistor. If the voltage sensed on the SENSE pin exceeds the current-limit threshold voltage (typically 160mV), the controller turns off the GATE output for that cycle.

To avoid reaching the current limit, the voltage on the sensing resistor (R_{SENSE}) should be below 80% of the current limit voltage (160mV). R_{SENSE} can be estimated with Equation (9):

$$R_{SENSE} = \frac{0.8 \times 160mV}{I_{PEAK}} \quad (9)$$

Where I_{PEAK} is the primary-side peak current.

Selecting the Power MOSFET

The controller can drive a wide variety of N-channel power MOSFETs. The critical parameters to select the MOSFET are the maximum drain-to-source voltage ($V_{DS(MAX)}$), the maximum current ($I_{D(MAX)}$), the on resistance ($R_{DS(ON)}$), the total gate charge (Q_G), and the turn-on threshold (V_{TH}).

In flyback applications, the off-state voltage across the MOSFET can be calculated with Equation (10):

$$V_{MOSFET} = V_{IN} + N \times V_{OUT} \quad (10)$$

Consider the voltage spike when the MOSFET turns off. $V_{DS(MAX)}$ should be greater than 1.5 times the calculated voltage.

In forward mode, the off-state voltage across the MOSFET is calculated with Equation (11):

$$V_{MOSFET} = \frac{D \times V_{IN}}{1 - D} + V_{IN} \quad (11)$$

Where D is the duty cycle, and the maximum duty cycle is limited at about 70%.

The maximum current through the power MOSFET occurs when the input voltage is at its minimum and the output power is at its maximum. The current rating of the MOSFET should be greater than 1.5 times I_{RMS}.

The on resistance of the MOSFET determines the conduction loss.

Q_G is important for MOSFET selection since it determines the commutation time. A high Q_G leads to high switching loss, while a low Q_G may cause fast turn-on/off speed, which determines the voltage spike on the MOSFET.

The turn-on threshold voltage (V_{TH}) is also important. GATE is powered by VCC, so V_{TH} must be below V_{CC}.

Selecting a Flyback Transformer

A transformer is an important component in a flyback converter since it determines the duty cycle, peak current, efficiency, MOSFET, and output diode rating. A good transformer should consider the winding ratio, primary-side inductance, saturation current, inductance leakage, current rating, and core selection.

The transformer winding ratio is important since it determines the duty cycle. Calculate the duty cycle with Equation (12):

$$D = \frac{N \times V_{OUT}}{N \times V_{OUT} + V_{IN}} \quad (12)$$

Where N is the transformer's primary-side winding to output winding ratio, and D is the duty cycle. A duty cycle of about 45% is recommended for most applications.

The primary-side inductance affects the input current ripple ratio factor. A higher-value inductor results in a larger transformer size and higher cost. A lower-value inductor results in a high switching peak current and RMS current, which causes a reduction in efficiency. Choose a primary-side inductor to set the current ripple ratio factor between 30% and 50%. Estimate the primary-side inductance with Equation (13):

$$L_P = \frac{V_{IN} \times D^2}{2 \times n \times I_{IN} \times f_{SW}} \quad (13)$$

Where *n* is the current ripple ratio, I_{IN} is the input current, and L_P is the primary inductance. Calculate L_P based on the minimum input voltage condition.

The transformer should have a high saturation current to support the switching peak current. Otherwise, the transformer inductance decreases sharply. The SENSE resistor can limit the switching peak current.

The energy stored in the inductance leakage cannot couple to the secondary side. This causes a high voltage spike when the MOSFET turns off. This decreases efficiency and increases stress on the MOSFET. Generally, the transformer inductance leakage should be limited below 3% of the transformer inductance.

The current rating counts the maximum RMS current, which allows current to flow through each winding. The current density should be controlled; otherwise, it can lead to high resistor power loss.

Diode Conduction Time Setting (Only for PSR Flyback Applications)

In PSR mode, the controller starts sampling the auxiliary-winding voltage after the primary-side power MOSFET turns off. A 300ns blanking time avoids spike ringing due to inductance leakage. To guarantee a sufficient FB sample period, the output diode current conduction time (t_{CON}) under light-load conditions should be longer than 600ns. Design the transformer to ensure that t_{CON} is longer than 700ns, and that V_{SENSE_PK} = 33mV, calculated with Equation (14):

$$\frac{33mV \times L_P \times N_S}{R_{SENSE} \times N_P \times (V_{OUT} + V_{DOF})} \geq 700ns \quad (14)$$

Where V_{DOF} is the output diode's forward drop voltage.

Selecting an RCD Snubber for Flyback Applications

The transformer's inductance leakage can cause spikes and excessive ringing on the MOSFET drain voltage waveform. An RCD snubber circuit limits the MOSFET voltage spike (see Figure 14).

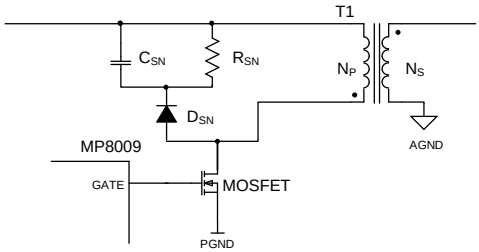


Figure 14: RCD Snubber

The power dissipation in the snubber circuit can be estimated with Equation (15):

$$P_{SN} = \frac{1}{2} \times L_K \times I_{PEAK}^2 \times f_{SW} \quad (15)$$

Where L_K is the inductance leakage, and I_{PEAK} is the peak switching current.

Since R_{SN} consumes the leakage inductance power loss, R_{SN} can be calculated with Equation (16):

$$R_{SN} = \frac{V_{SN}^2}{P_{SN}} \quad (16)$$

Where V_{SN} is the expected snubber voltage on C_{SN}.

The snubber capacitor (C_{SN}) can be designed to achieve an appropriate voltage ripple on the snubber, estimated with Equation (17):

$$\Delta V_{SN} = \frac{V_{SN}}{R_{SN} \times C_{SN} \times f_{SW}} \quad (17)$$

Generally, a 15% ripple is acceptable.

Selecting an Output Diode for Flyback Applications

The flyback output rectifier diode supplies current to the output capacitor when the primary-side MOSFET is off. Use a Schottky diode to reduce losses due to the diode forward voltage and recovery time. The diode should be rated for a reverse voltage 1.5 times greater than the calculated value, which is estimated with Equation (18):

$$V_{DIODE} = \frac{V_{IN}}{N} + V_{OUT} \quad (18)$$

The average current rating must exceed the maximum expected load current, and the peak current rating must exceed the output winding peak current. It is recommended to add an RC snubber circuit for the output diode.

Selecting a Transformer for Forward Applications

The forward transformer transfers energy to the output when the power MOSFET turns on. Its key parameters are the winding ratio, primary-side winding turns, current rating, and core selection. The transformer winding ratio determines the duty cycle, and is calculated with Equation (19):

$$D = \frac{V_{OUT} \times N}{V_{IN}} \quad (19)$$

Where N is the transformer's primary-side winding to output winding ratio. Generally, a duty cycle of about 45% is recommended for most applications.

When the power MOSFET turns on, the transformer transfers energy to the output. Meanwhile, the input voltage generates an exciting current in the transformer. There should be sufficient primary-side winding to prevent the transformer from saturating. The peak exciting current can be estimated with Equation (20):

$$I_{EXC} = \frac{V_{OUT} \times N}{2 \times L_P \times f_{SW}} \quad (20)$$

Where I_{EXC} is the peak exciting current, and L_P is the primary inductance.

When using I_{EXC} to calculate the primary winding, ensure that there are sufficient margins from extreme condition (e.g. load transient and OCP). The current rating depends on the maximum RMS current, which flows through each winding. The current density should be controlled; otherwise, it can lead to high resistive power loss.

Selecting a SYNC MOSFET for Forward Applications

The MP8009's DC/DC controller supports active clamp forward. The active clamp P-channel MOSFET should have the same maximum voltage as the main power MOSFET. Its maximum current should exceed the exciting peak current and RMS current.

Selecting the Output MOSFET for Forward Applications

The forward output needs two diodes to conduct the current. If higher efficiency is required, the diodes can be replaced by MOSFETs (see Figure 15).

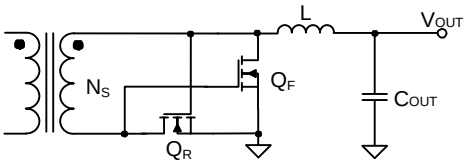


Figure 15: Forward Output MOSFET

The MOSFET voltage rating should be greater than its max V_{DS} voltage. Q_R's maximum V_{DS} can be calculated with Equation (21):

$$V_R = \frac{D \times V_{IN}}{N \times (1 - D)} \quad (21)$$

Q_F's maximum V_{DS} voltage can be calculated with Equation (22):

$$V_F = \frac{V_{IN}}{N} \quad (22)$$

Where N is the transformer primary winding to output winding ratio, and D is the primary MOSFET duty cycle. Ensure that there is some margin.

The MOSFET current rating should be greater than its maximum RMS current and peak current. Q_R's RMS current can be estimated with Equation (23):

$$I_R = I_{OUT} \times \sqrt{D} \times \sqrt{1 + \frac{1}{3} \times (\frac{I_{PP}}{I_{OUT}})^2} \quad (23)$$

Q_F's RMS current can be calculated with Equation (24):

$$I_F = I_{OUT} \times \sqrt{1 - D} \times \sqrt{1 + \frac{1}{3} \times (\frac{I_{PP}}{I_{OUT}})^2} \quad (24)$$

Where I_{PP} is the inductor's peak-to-peak current.

The Q_R MOSFET's gate-driving voltage is equal to V_F, and the Q_F MOSFET's gate-driving voltage is equal to V_R. If the driving voltage exceeds each MOSFET's maximum gate voltage, a clamp circuit is required. The MOSFET turn-on resistance determines the conduction loss, while Q_G determines the driver circuit loss. These values should be low enough to obtain higher efficiency and lower rising temperatures.

Selecting an Output Inductor for Forward Applications

The output inductor used for forward applications must supply constant current to the output load while the main power MOSFET turns on. A larger-value inductor results in less ripple current and lower output voltage ripple. However, a larger-value inductor also has a larger physical size, higher series resistance, and lower saturation current. A good rule to determine the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 30% to 50% of the maximum output current. The inductance value can be calculated by with Equation (25):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT} \times N}{V_{IN}}) \quad (25)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_{SW} is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that does not saturate under the maximum inductor peak current.

Selecting the Input Capacitor

An input capacitor is required to supply the AC ripple current to the inductor while limiting noise at the input source. A low-ESR capacitor is required to keep the noise on the IC at a minimum. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors can also be used. For ceramic capacitors, the capacitance dominates the input ripple at the switching frequency.

In flyback mode, the input ripple can be estimated with Equation (26):

$$\Delta V_{IN} = I_{IN} \times \frac{V_{IN}}{f_{SW} \times C_{IN} \times (N \times V_{OUT} + V_{IN})} \quad (26)$$

Where ΔV_{IN} is the input voltage ripple, I_{IN} is the input current, and C_{IN} is the input capacitor.

In forward mode, the input ripple can be estimated with Equation (27):

$$\Delta V_{IN} = \frac{I_{IN}}{f_{SW} \times C_{IN}} \times (1 - \frac{V_{OUT} \times N}{V_{IN}}) \quad (27)$$

Output Capacitor Selecting

The output capacitor maintains the DC output voltage. For the best results, use ceramic capacitors or low-ESR capacitors to minimize

the output voltage ripple. For ceramic capacitors, the capacitance dominates the output ripple at the switching frequency.

In flyback mode, the output ripple can be estimated with Equation (28):

$$\Delta V_{OUT} = \frac{N \times V_{OUT}}{(V_{IN} + N \times V_{OUT}) \times f_{SW}} \times \frac{I_{OUT}}{C_{OUT}} \quad (28)$$

If the voltage ripple is too high, a π filter is required. Choose the inductor to be between 0.1μH an 0.47μH to achieve an ideal output voltage ripple, as well as system stability.

In forward mode, the output ripple can be estimated with Equation (29):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT} \times N}{V_{IN}}) \quad (29)$$

Design Examples

Table 4 shows a PSR topology flyback design example following the application guidelines for the specifications below.

Table 4: PSR Flyback Design Example

PoE Input	36V to 57V
V_{OUT}	12V
I_{OUT}	2.1A

For the detailed application schematic, see Figure 19 on page 36. For the typical performance and circuit waveforms, see the Typical Performance Characteristics section on page 14. For more device applications, refer to the related evaluation board datasheet.

Table 5 lists a design example for forward applications.

Table 5: SSR Forward Design Example

PoE Input	36V to 57V
Adapter Input	48V
V_{OUT}	5V
I_{OUT}	4.8A

For the detailed application schematic, see Figure 20 on page 36. For more detailed device applications, refer to the related evaluation board datasheet.

PCB Layout Guidelines

Efficient layout of the PoE front-end and high-frequency switching power supply is critical for stable operation. Poor layout may result in reduced performance, excessive EMI, resistive loss, and system instability. For the best results, refer to Figure 16, Figure 17, and Figure 18, and follow the guidelines below:

PD Interface Circuit

All component placements must follow the power flowing from RJ-45, the Ethernet transformer, the diode bridges, the TVS to 0.1μF capacitor, and the DC/DC converter input bulk capacitor. The spacing between VDD and VSS must comply with safety standards, such as IEC60950.

1. Make all leads as short as possible with wide power traces.
2. Place the PD interface circuit ground planes so that they are referenced to VSS.
3. Place the switching converter ground planes so that they are referenced to RTN/GND.
4. Connect the exposed pad to GND. It cannot be connected to VSS.
5. Place the AUX resistor divider close to AUX if adapter power detection is enabled.

Flyback Topology

1. For minimal noise and ringing, keep the input loop as short as possible between the input bulk capacitor, transformer, MOSFET, sense resistor, and GND plane.
2. Keep the output loop between the rectifier diode, output capacitor, and transformer as short as possible.
3. Keep the clamp loop circuit between D3, C6, and the transformer as small as possible.
4. Place the VCC capacitor close to the VCC and GND pin for the best decoupling.
5. Route the feedback trace far away from noise sources, such as the switching node.
6. Place the COMP components close to the COMP pin.
7. Use a single-point connection between power GND and signal GND.

Figure 16 shows a recommended flyback layout for primary-side regulation. See the Typical Application on page 1 for more details.

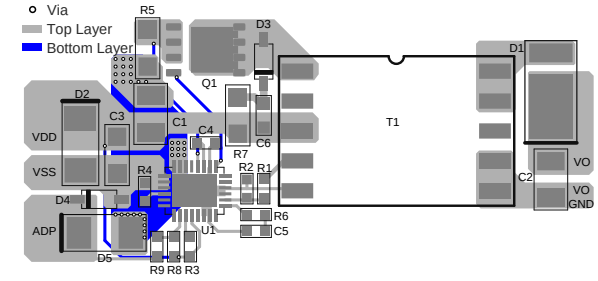


Figure 16: Recommended Flyback Topology PCB Layout

Forward Topology

1. For minimal noise and ringing, keep the input loop as short as possible between the input capacitor, transformer, Q1, and sense resistor.
2. For minimal noise and ringing, keep the active clamp loop as short as possible between the input capacitor, transformer, C6, and Q2.
3. Keep the output high-frequency current loop as short as possible between the transformers, D1, and D2.
4. Place the VCC capacitor close to the VCC and GND pin for the best decoupling.
5. Route the COMP feedback trace far away from noise sources, such as the switching node.
6. Use a single-point connection between power GND and signal GND.

Figure 17 shows a recommended forward layout. For more details, refer to the related evaluation board datasheet.

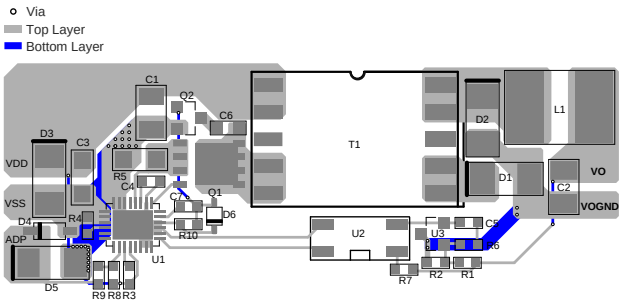


Figure 17: Recommended Forward Topology PCB Layout

Figure 18 shows the recommended schematic for a forward layout.

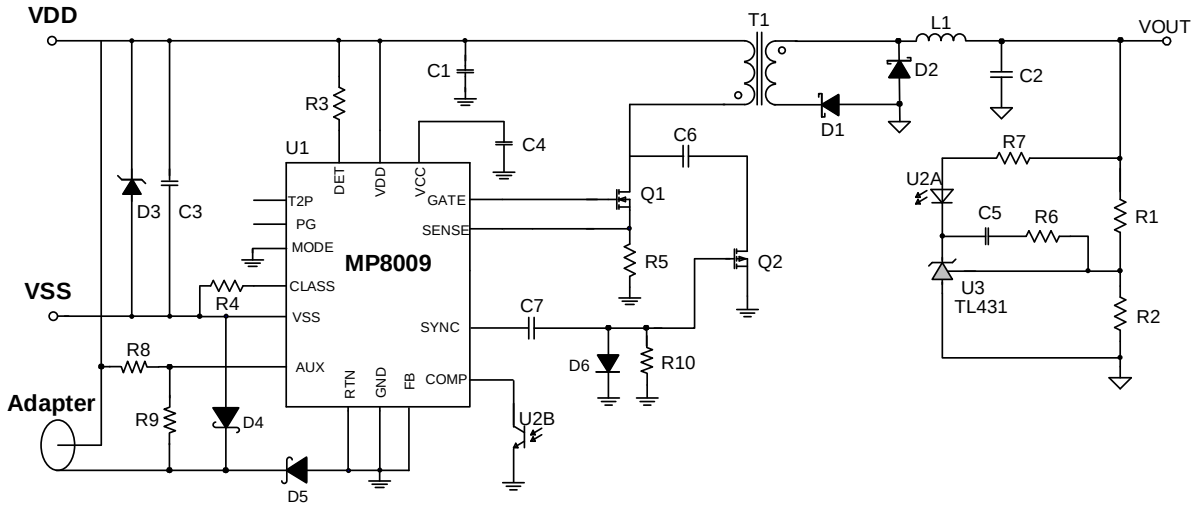


Figure 18: Forward Layout Schematic

TYPICAL APPLICATION CIRCUITS

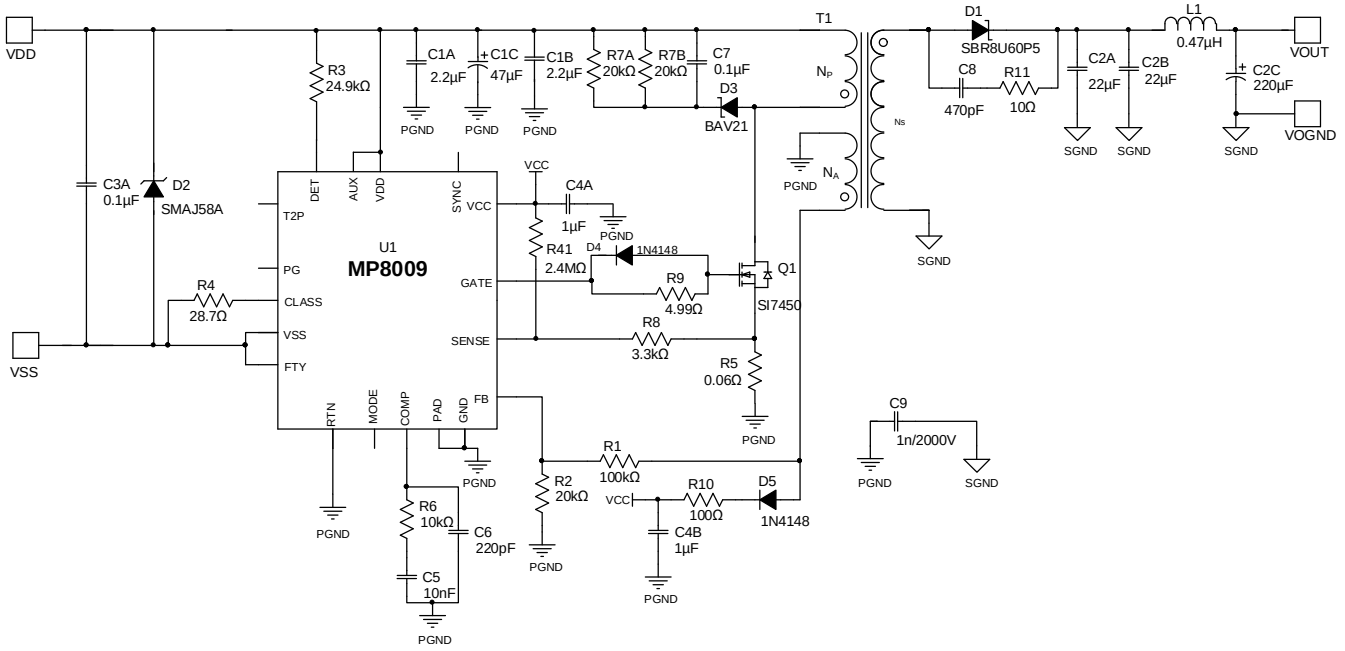


Figure 19: Typical Application Circuit (VDD - VSS = 36V to 57V PoE Input, V_{OUT} = 12V/2.1A)

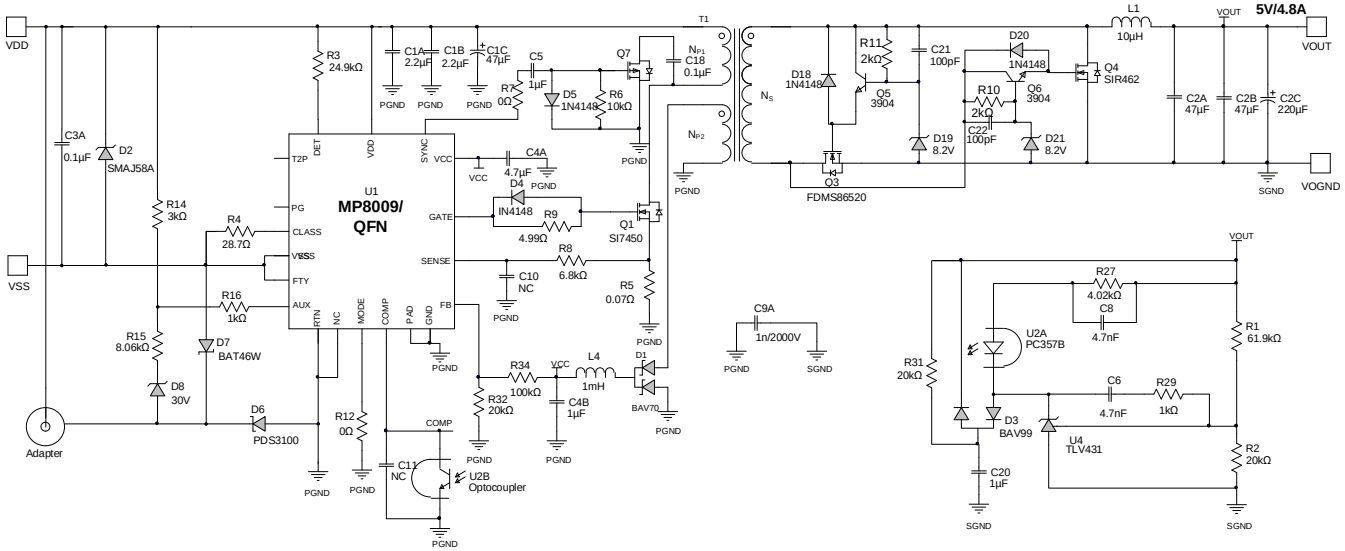
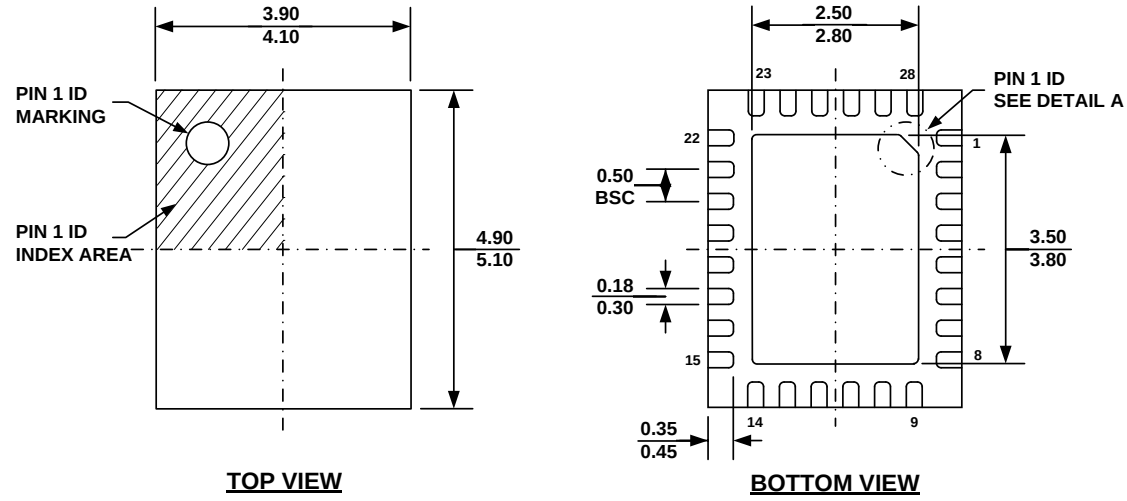


Figure 20: Typical Application Circuit (VDD - VSS = 36V to 57V PoE Input or 48V Adapter, V_{OUT} = 5V/4.8A)

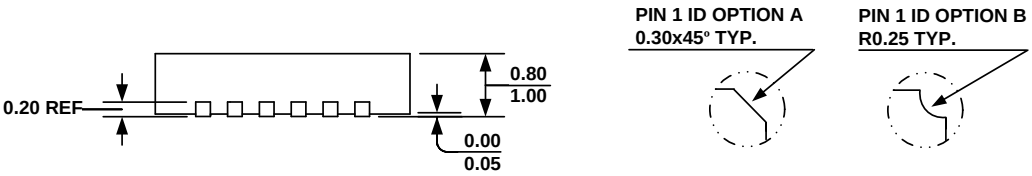
PACKAGE INFORMATION

QFN-28 (4mmx5mm)



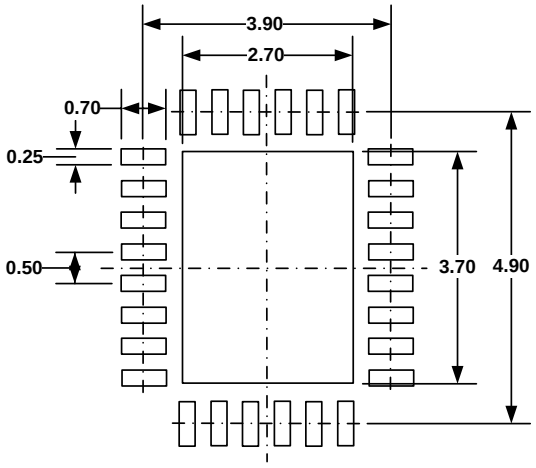
TOP VIEW

BOTTOM VIEW



SIDE VIEW

DETAIL A

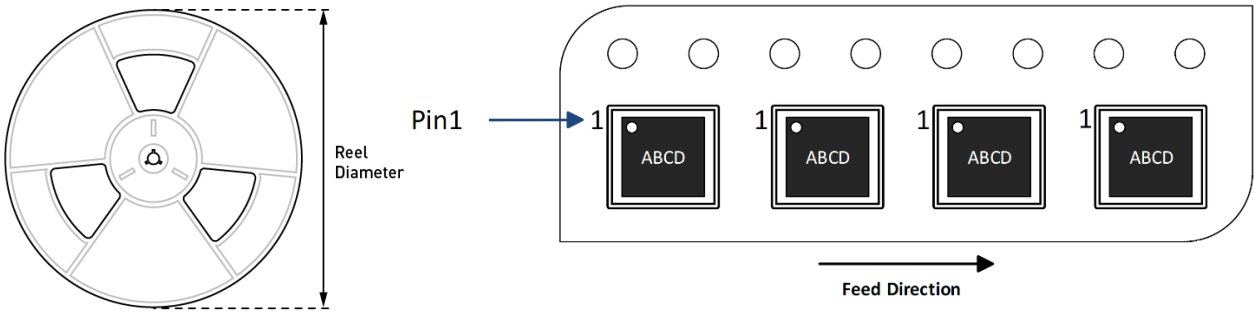


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VGHD-3.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8009GV–Z	QFN-28 (4mmx5mm)	5000	N/A	13in	12mm	8mm

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	12/9/2020	Initial Release	-

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