MP8620

25A, 16V,
Fully Integrated Synchronous Buck

The Future of Analog IC Technology

DESCRIPTION

The MP8620 is a fully integrated step-down converter with internal power MOSFETs. It achieves 25A continuous output current over a wide input supply range with excellent load and line regulation. The MP8620 can be configured and optimized as a single phase or a multi-phase solution to support high current (50A-100A) applications. This provides the flexibility and at the same time meets the efficiency requirement with less components.

Average current mode control scheme is employed in the MP8620. The device operates reliably even with low duty cycle and noisy environment.

Fault condition protection include cycle-by-cycle current limit, thermal shutdown, output short-circuit, output under voltage and output over voltage protection.

The MP8620 requires a minimum number of readily available standard external components and is available in a 6x6mm QFN package.

The MP8620 is suitable for a wide range of space-constraint applications, including point of load regulation for FPGAs, ASICs, DDR memory power, and power systems for networking and data centers.

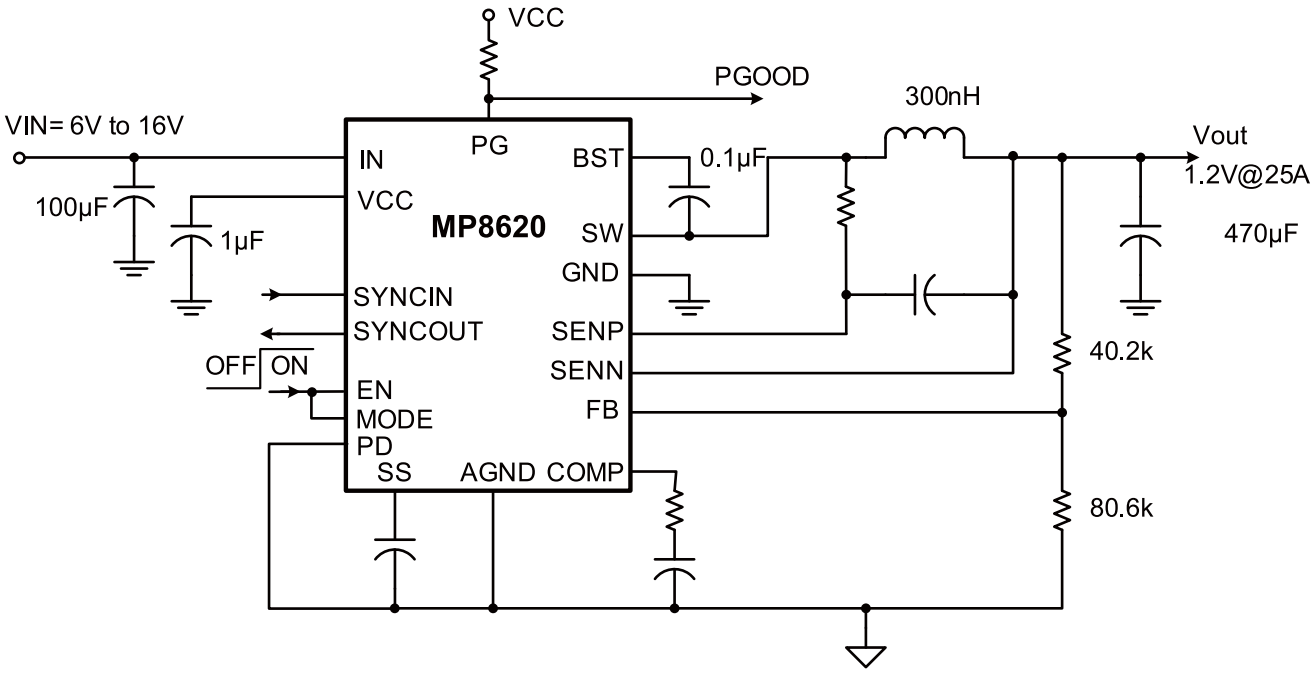
FEATURES

- Supports Multi-phase Configuration up to 100A
- Wide 6V to 16V Operating Input Range
- 25A Output Current
- 3mΩ/12mΩ Internal Power MOSFET Switches Deliver up to 95% Efficiency
- Synch Output to Drive Another Regulator in 90o, 120o,180o Phase-Shift Operation
- Synch from 300kHz to 900kHz External Clock
- Default 600kHz Frequency, Programmable from 300kHz to 1.5MHz.
- Feedback Voltage Accuracy: 1.0%
- Programmable Soft-Start
- Startup Tracking
- EN and Power Good for Power Sequencing
- Cycle-by-Cycle Over Current Protection, SCP, OCP, OVP, UVP and Thermal Shutdown
- Output Adjustable from 0.8V
- Stable with Low ESR Output Ceramic Capacitors
- Available in a 6x6mm QFN Package

APPLICATIONS

- Distributed Power Systems
- Pre-Regulator for Linear Regulators
- Networking and Data Centers
- DDR Memory Power

TYPICAL APPLICATION (AVERAGE CURRENT MODE)

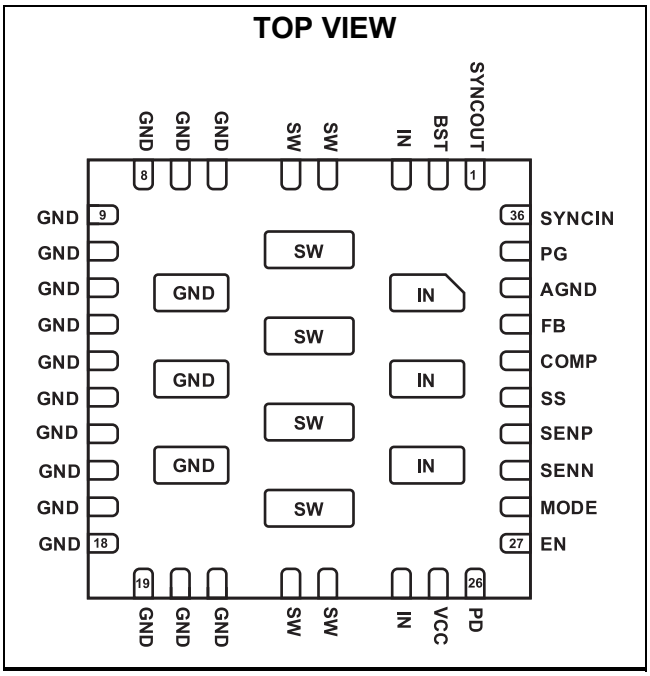


ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP8620DQK	QFN (6x6mm)	MP8620	-40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP8620DQK–Z).
For RoHS Compliant packaging, add suffix –LF (e.g. MP8620DQK–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 20V
V_{SW} ..... -0.3V to V_{IN} + 0.3V
V_{BST} ..... V_{SW} + 6V
All Other Pins ..... -0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2)
..... 4.16W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 6V to 16V
Output Voltage V_{OUT} ..... 0.8V to VCC-1.5V
Operating Junct. Temp (T_J) ..... +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN (6x6mm)	30	6	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	6V ≤ V_{IN} ≤ 16V	0.792	0.800	0.808	V
Feedback Current	I_{FB}	V_{FB} = 0.8V		10		nA
Switch Leakage		V_{EN} = 0V, V_{SW} = 0V		0.1	0.7	μA
Current Sense Voltage Limit	V_{SENP}-V_{SENN}			18.5		mV
Default Oscillator Frequency	f_{SW}	V_{FB} = 0.6V		600		kHz
Maximum Duty Cycle		V_{FB} = 0.6V		90		%
Minimum On Time	t_{ON}			50		ns
Soft-Start Charging Current	I_{SS}			4		μA
COMP Threshold for Switching	V_{COMP_THRESH}			1.5		V
Maximum COMP Level	V_{COMP_MAX}			3.2		V
Gain of Error Amplifier	G_{EA}			1.2		mA/V
Gain of Error Sink		V_{COMP} = 1.5V		-130		μA
Gain of Error Source		V_{COMP} = 1.5V		130		μA
Gain of Internal Current Sense	A_{CS}			30		V/V
Slope Compensation	V_{SLOPE}			1.1		V
Power Good Ramp Up Threshold				90		%
Power Good Ramp Down Threshold				85		%
Power Good Rising Delay		From 90% REF to PG high		500		μs
Power Good Falling Delay		From 85% REF to PG low		50		μs
Power Good Sink Current Capability	V_{PG}	Sink 4mA			0.4	V
Power Good Leakage Current	I_{PG_LEAK}	V_{PG} = 3.3V			1	μA
V_{CC} Tolerance	V_{CC}	I_{CC} = 0mA	4.5	5	5.5	V
V_{CC} Regulation		I_{CC} = 0~20mA		5		%
Sync Frequency	F_{SYNC}		0.3		0.9	MHz
SYNCIN Bias Current	I_{SYNCIN}			10		nA
SYNCIN Logic High Voltage(5)			1.3			V
SYNCIN Logic Low Voltage(5)					0.4	V
SYNCOUT High Level		V_{CC} = 5V,Source 5mA		4.6		V
SYNCOUT Low Level		V_{CC} = 5V, Source 5mA		0.4		V
Under Voltage Lockout Threshold Rising			4.4	4.8	5.2	V
Under Voltage Lockout Threshold Hysteresis				415		mV
EN Input Low Voltage					0.4	V
En Input High Voltage			1.3			V
EN Input Current		V_{EN} = 2V		2		μA
		V_{EN} = 0V		0.1		

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)		V_{EN} = 0V		0.1		μA
Supply Current (Quiescent)		V_{EN} = 2V, V_{FB} = 1V		2		mA
Thermal Shutdown				150		°C
SENP Bias Current	I_{SENP}			100		nA
SENN Bias Current	I_{SENN}			100		nA
Slave Mode Threshold				3		V
Negtive current limit	V_{SENP}-V_{SENN}			3		mV
Phase shift for SYNCOUT		V_{PD}<1V @1MHz		180°		
		1V<V_{PD}<3V @1MHz		120°		
		V_{PD}>3V @1MHz		90°		
MODE Input High Voltage			1.3			
MODE Input Low Voltage					0.4	V
EN High To Switching Delay		C_{SS}=10nF		750		μs

Notes:

5) Guaranteed by design.

PIN FUNCTIONS

Pin #	Name	Description
1	SYNCOUT	Timing output to drive another MP8620 (or similar device) SYNCIN for phase-shift operation.
2	BST	Bootstrap. A capacitor is connected between SW and BST pins to form a floating supply across the high-side power switch driver, so that the high-side power switch's gate can be pulled above the input voltage.
3, 24 Exposed Pad	IN	Input Voltage. The MP8620 operates from a +6V to +16V input rail. A decoupling capacitor is needed to suppress the large spikes from the input rail. Use wide PCB traces and multiple vias to make the connection.
4, 5, 22, 23 Exposed Pad	SW	Switch Output. These pins are fused together on package.
6-21 Exposed Pad	GND	Power Ground. These pins are fused together on package.
25	VCC	Bias Supply. Decouple with a 1µF ceramic capacitor.
26	PD	Connect this pin to different voltage level to program phase delay on SYNCOUT. Connect it to AGND, VCC or any point in middle of 0 to VCC to generate 180°C, 90°C or 120°C phase shifted clock on SYNCOUT correspondingly.
27	EN	Enable/Disable the part. EN and MODE pins will work together to determine the working status of MP8620.
28	MODE	Test pin. To ensure proper operation, this pin should be shorted with EN pin.
29	SENN	Current Sensing Amplifier Inverting Input. Connect the filtering cap very close to SENP and SENN. Keep SENP, SENN away from noisy nodes like IN, SW, GND,BST
30	SENP	Current Sensing Amplifier Non-Inverting Input.
31	SS	Soft-Start. Connect a capacitor to ground. A 4µA current source charges the capacitor during start-up. An 8µA current source discharges the capacitor during soft shut-down.
32	COMP	Compensation. Connect a R/C network to FB.
33	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. Pull FB to VCC will force the chip into slave mode.
34	AGND	Analog Ground.
35	PG	Power Good Indicator. The output of this pin is an open drain of a MOSFET.
36	SYNCIN	External Frequency Synchronization Input. Short this pin to ground will force the chip to use internal default clock frequency. The switching frequency also can be programmed by connecting an external resistor between this pin and AGND.

BLOCK DIAGRAM

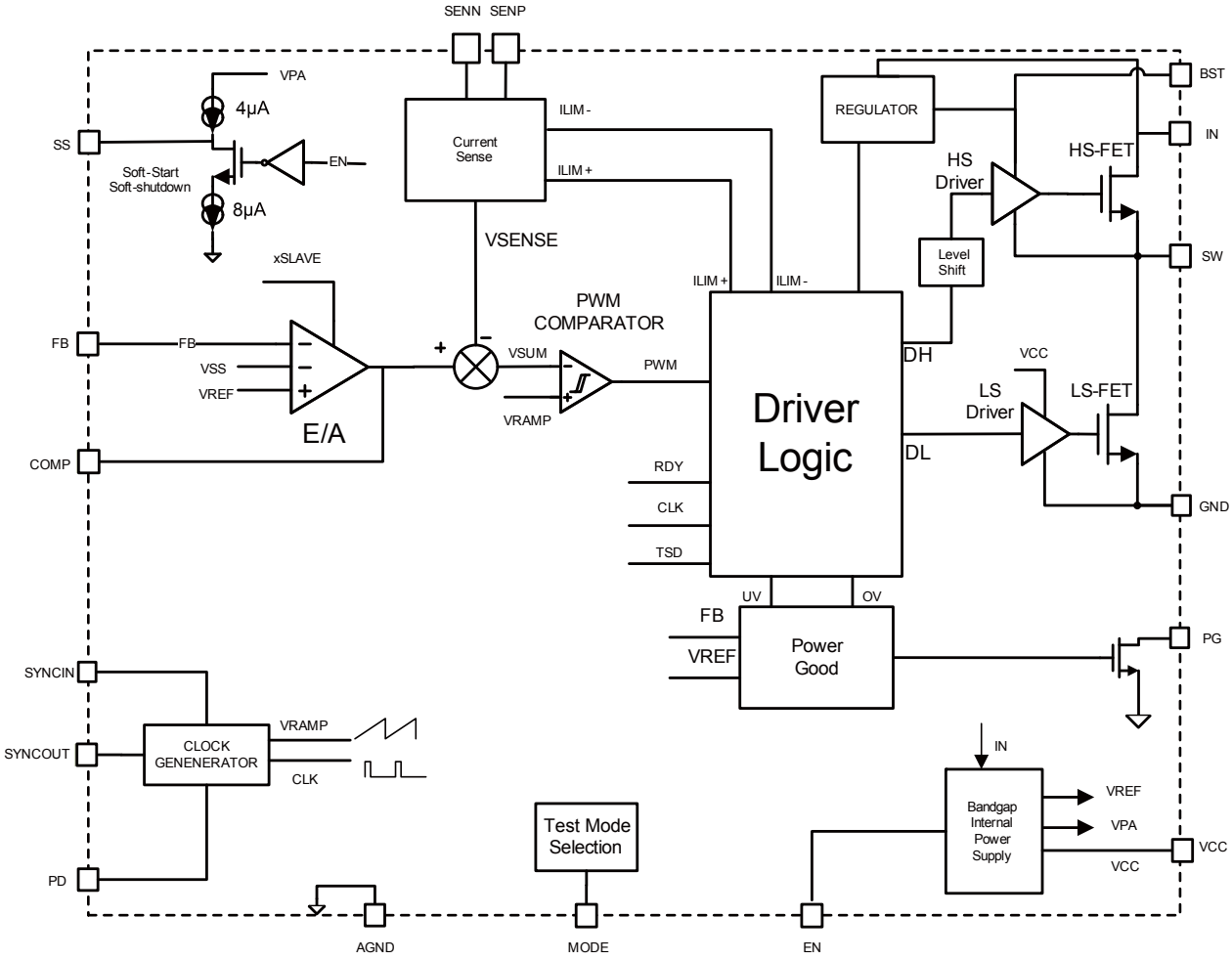


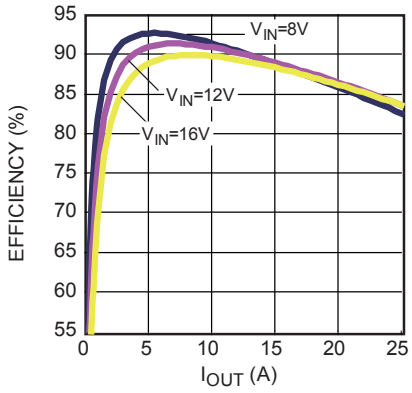
Figure 1—Function Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, V_{OUT}=1.2V, L=0.82µH, T_A=+25°C, unless otherwise noted.

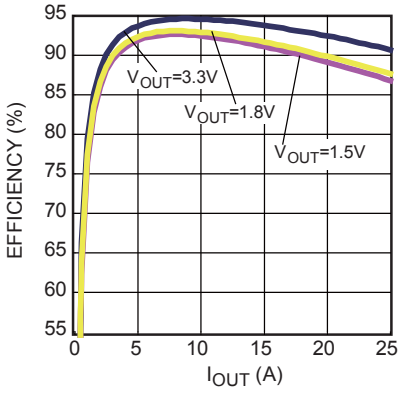
Efficiency

V_{OUT}=1.2V, f_{sw}=300kHz, L=0.82µH



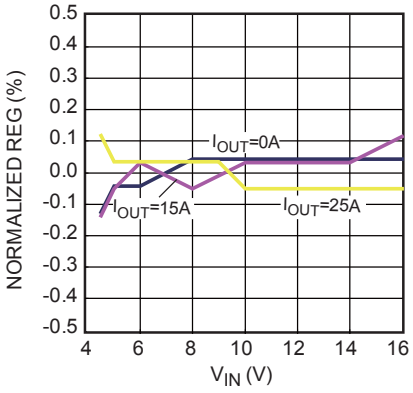
Efficiency

V_{IN}=12V, f_{sw}=300kHz

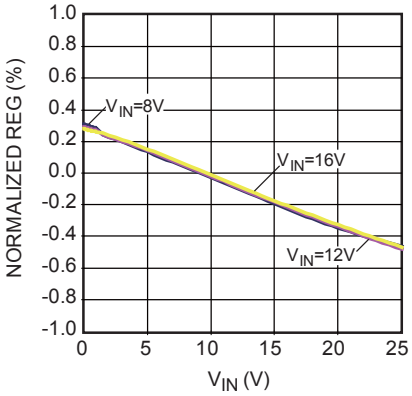


Line Regulation

V_{OUT}=1.2V

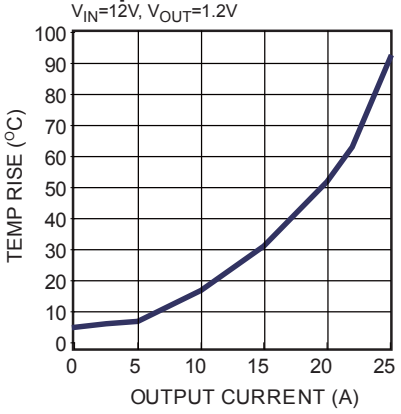


Load Regulation

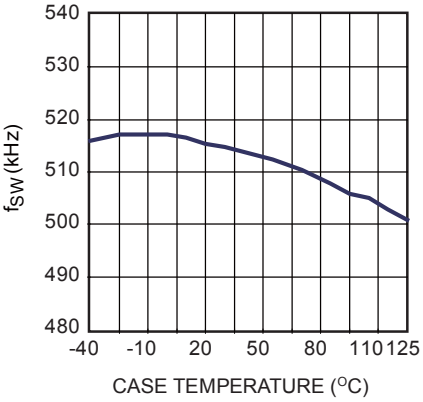


Case Temp Rise vs. Output Current

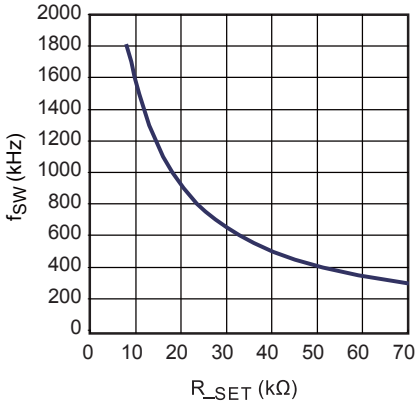
V_{IN}=12V, V_{OUT}=1.2V



Frequency vs. Temperature



Frequency vs. Setting Resistor

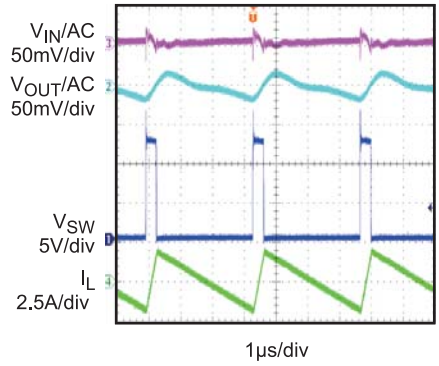


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT}=1.2V, L=0.82µH, T_A=+25°C, unless otherwise noted.

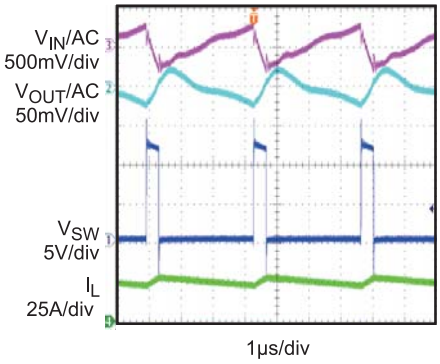
Input/Output Voltage Ripple

I_{OUT}=0A, f_{SW}=300kHz



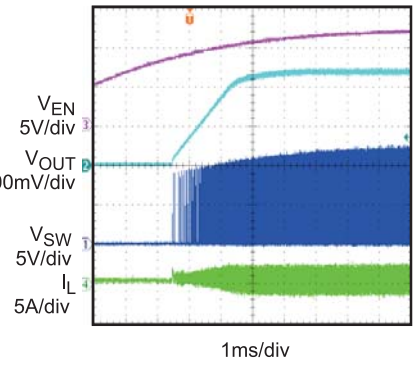
Input/Output Voltage Ripple

I_{OUT}=25A, f_{SW}=300kHz



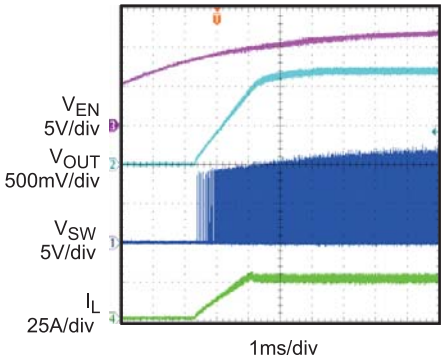
Start up through IN

I_{OUT}=0A



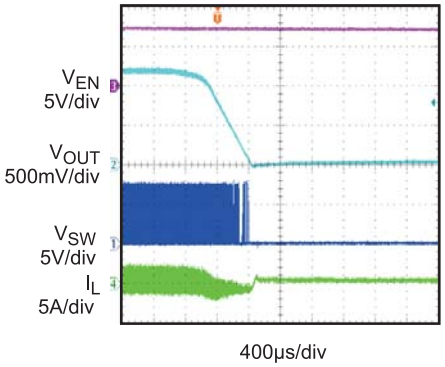
Start up through IN

I_{OUT}=25A



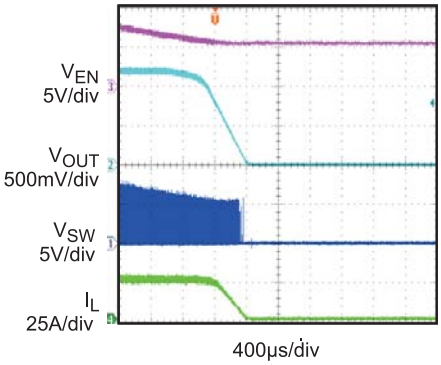
Power down through IN

I_{OUT}=0A



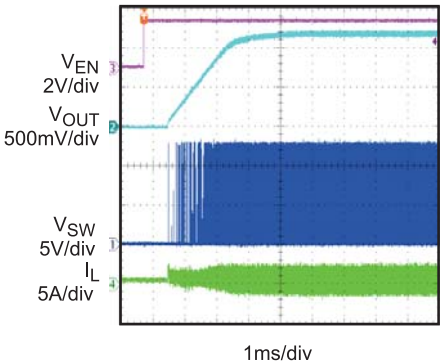
Power down through IN

I_{OUT}=25A



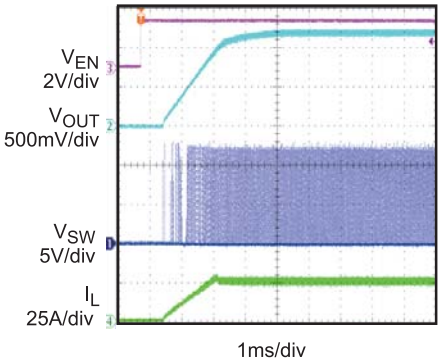
Start up through EN

I_{OUT}=0A



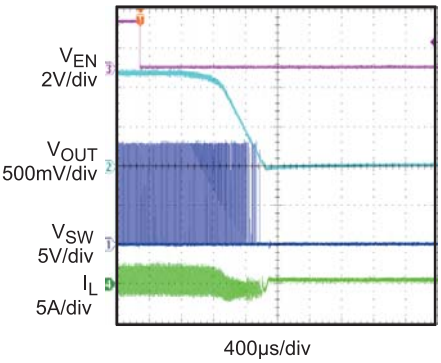
Start up through EN

I_{OUT}=25A



Power down through EN

I_{OUT}=0A

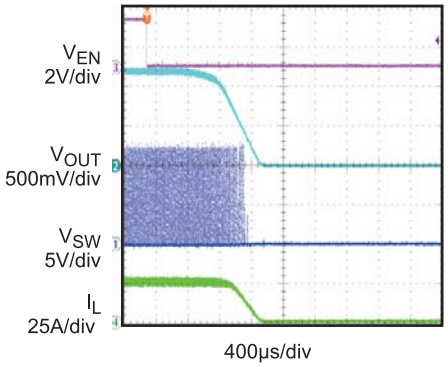


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

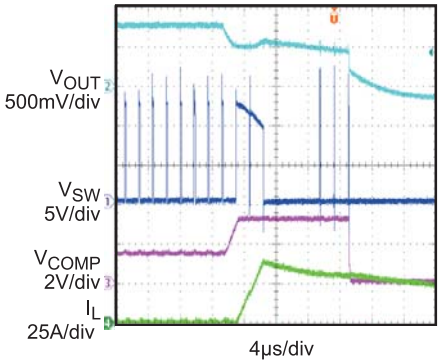
V_{IN}=12V, V_{OUT}=1.2V, L=0.82µH, T_A=+25°C, unless otherwise noted.

Power down through EN

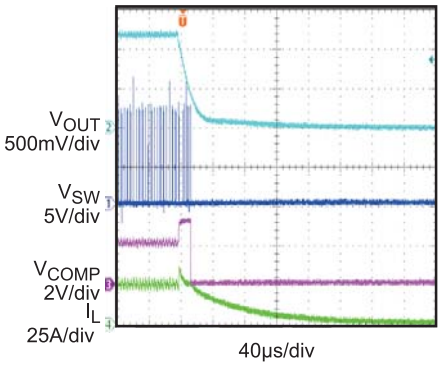
I_{OUT}=25A



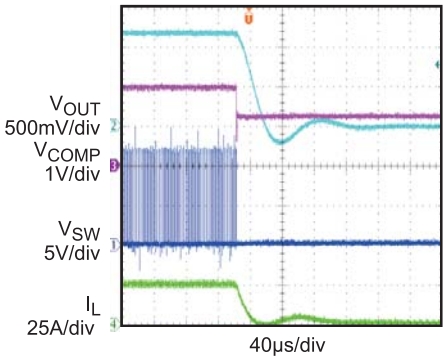
Short-circuit Protection



Over-current Protection

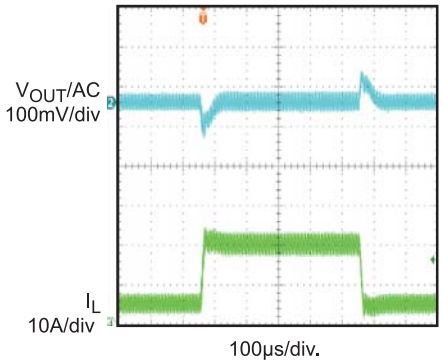


Over-voltage Protection



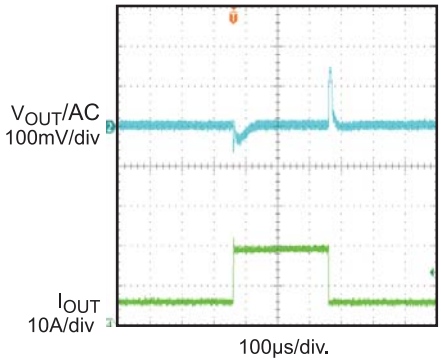
Transient Response

I_{OUT}=5A-20A @ 2.5A/µs



Transient Response

I_{OUT}=5A-20A@ 7.5A/µs



OPERATION

Basic PWM Scheme

The MP8620 utilizes average current mode control scheme. The EA output voltage is proportional to the average inductor current.

At the beginning of a cycle, high side switch HS-FET is off. The EA output voltage is higher than the sum of current sense amplifier output and ramp signal, and the PWM comparator's output is low. The falling edge of the CLK signal sets the RS Flip-Flop, which turns on the HS-FET. The inductor is charged by the input supply.

The ramp signal will rise up after HS-FET is turned on, as well as the current sense voltage signal. When the sum of the Current Sense Amplifier output and the ramp signal exceeds the EA output voltage, the RS Flip-Flop is reset and the MP8620 reverts to its initial HS-FET off state

If the sum of the Current Sense Amplifier and the ramp signal does not exceed the COMP voltage, then the rising edge of the CLK resets the Flip-Flop. There is a maximum duty cycle limitation on MP8620.

The output of the Error Amplifier integrates the voltage difference between the feedback and the 0.8V bandgap reference, and it converts the voltage difference into a current source to charge up the Error Amplifier output. The EA output voltage is proportional to the average inductor current, the higher EA output voltage, the higher inductor current delivered to the output.

The MP8620 employs a synchronous low side switch (LS-FET). Whenever the HS-FET is off, the LS-FET is turned on to minimize the conduction loss.

Enable Control

EN pin and MODE pin together will determine the working status of MP8620. In all operation conditions, EN pin and MODE pin should be connected together to ensure proper operation. When EN/MODE are pulled high, MP8620 are enabled and a SS is initialized. When EN/MODE are pulled low, MP8620 is disabled, then soft shut-down will begin.

DCR Sensing

The MP8620 adopts a lossless current sensing scheme, commonly referred to as inductor DCR sensing, as shown in Figure 2. As long as the time constant of the power inductor is equal to the time constant of the RC network placed across the power inductor, the voltage across the capacitor is equal to the instantaneous inductor current times the DC resistance of the inductor winding. For example, in Figure 2(a), when

$$R_{DCR} = \frac{L}{R7 \cdot C13}$$

The differential voltage across SENP and SENN pins is

$$V_{CS} = i_L \cdot R_{DCR}$$

In some applications, users may need to program the current sensing gain by choosing inductors with different DCR values. An alternative way to implement it is to add resistor divider, as shown in Figure 2(b). The time-constant-matching equation becomes:

$$R_{DCR} = \frac{L}{C13}\left(\frac{1}{R7} + \frac{1}{R6}\right)$$

And the differential voltage across SENP and SENN pins becomes:

$$V_{CS} = i_L \cdot \left(\frac{R6}{R7 + R6}\right) \cdot R_{DCR}$$

Use the worst-case inductance and R_{DCR} values provided by the inductor manufacturer, adding some margin for the inductance drop over temperature and load.

The internal CS amplifier of MP8620 can also take the input from a 1% high accuracy current sensing resistor for the best current sensing accuracy.

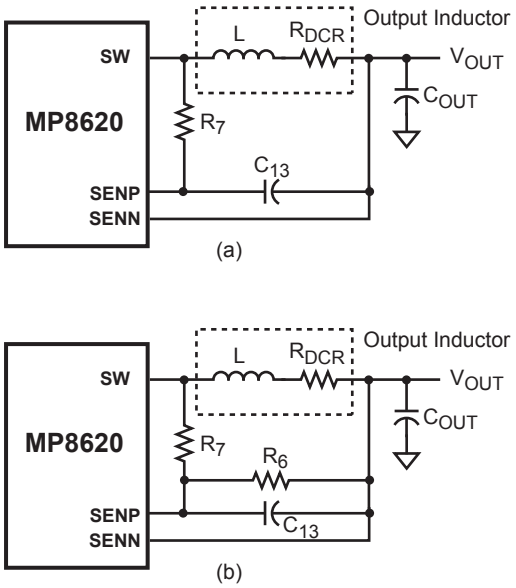


Figure 2—Lossless Inductor DCR Current Sensing

Frequency Setting

The MP8620 oscillating frequency is set by an external resistor from the SYNCIN pin to ground. The value of Rset can be calculated from:

$$R_{SET}(k\Omega) = \frac{14000}{f_{SW}(kHz) - 170}$$

The MP8620 can also be synchronized by an external clock pulse through SYNCIN pin. The frequency of the clock pulse should be in the range of 300kHz-900kHz.

Input UVLO and Startup

The MP8620 remains in shutdown mode until input voltage rises above 4.8V. If EN is brought high, the soft-start begins, the part starts switching when V_{SS} is higher than 300mV. There is a 415mV hysteresis when VCC drops. When the input voltage drops below the UVLO falling edge, the part shuts off. This is non-latch protection. Once the input voltage rises above the UVLO rising edge, it restarts again.

Once the soft-start is initiated, an internal 4μA current source charges the external capacitor connected to SS pin. The internal reference is overridden by the SS voltage to regulate the output voltage. When the SS voltage exceeds the internal reference voltage, the FB pin is regulated by the internal reference. The soft-start time or the output voltage ramp up time is calculated as

$$t_{ss} = \frac{(0.8 + 0.3) \cdot C_{SS}}{4\mu A}$$

Power Good (PG)

MP8620 has power-good (PG) output. The PG pin is the open drain of a MOSFET. It should be connected to VCC or other voltage source through a resistor (e.g. 100k). After the input voltage is applied, the MOSFET is turned on, so that the PG pin is pulled to GND before SS ready. After FB voltage reaches 90% of REF voltage, the PG pin is pulled high after a 500μs delay. When the FB voltage drops to 85% of REF voltage, the PG pin will be pulled low after 50us delay.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

MP8620 has cycle-by-cycle over-current limit control. The peak inductor current is monitored during the ON state of the high side power switch. Once it detects that the inductor current is higher than the current limit, the high side power switch is turned off. If the FB voltage doesn't trigger UV (under-voltage, 70% of reference voltage), the high side power switch is turned on again when next CLK cycle kicks in. If the current limit is hit, together with UV and COMP saturation, it triggers OCP. The MP8620 enters latch mode once OCP is triggered. It needs power cycle to restart. When the output is short-circuited, it triggers OCP as well.

Over/Under-voltage Protection (OVP/UVP)

MP8620 monitors the output voltage through a resistor divided feedback (FB) voltage to detect over and under voltage on the output. When the FB voltage is higher than 130% of the reference voltage, it'll trigger OVP. Once it triggers OVP, the LS-FET is always on, while the HS-FET is off. It needs power cycle to power up again. When the FB voltage is below 70% of the reference voltage, UVP will be triggered. Usually UVP is accompanied with current limit and COMP saturation, hence it results in SCP.

Thermal Shutdown

Thermal shutdown is employed in MP8620. The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (typically 150ºC), the converter latches off. It needs power recycle to power up again.

Output Voltage Tracking and Sequencing

The MP8620 allows the user to program how its output voltage ramps during startup by means of the SS pin. Through this pin, the output voltage can be set to either coincidentally or rationally track another output voltage, as shown below:

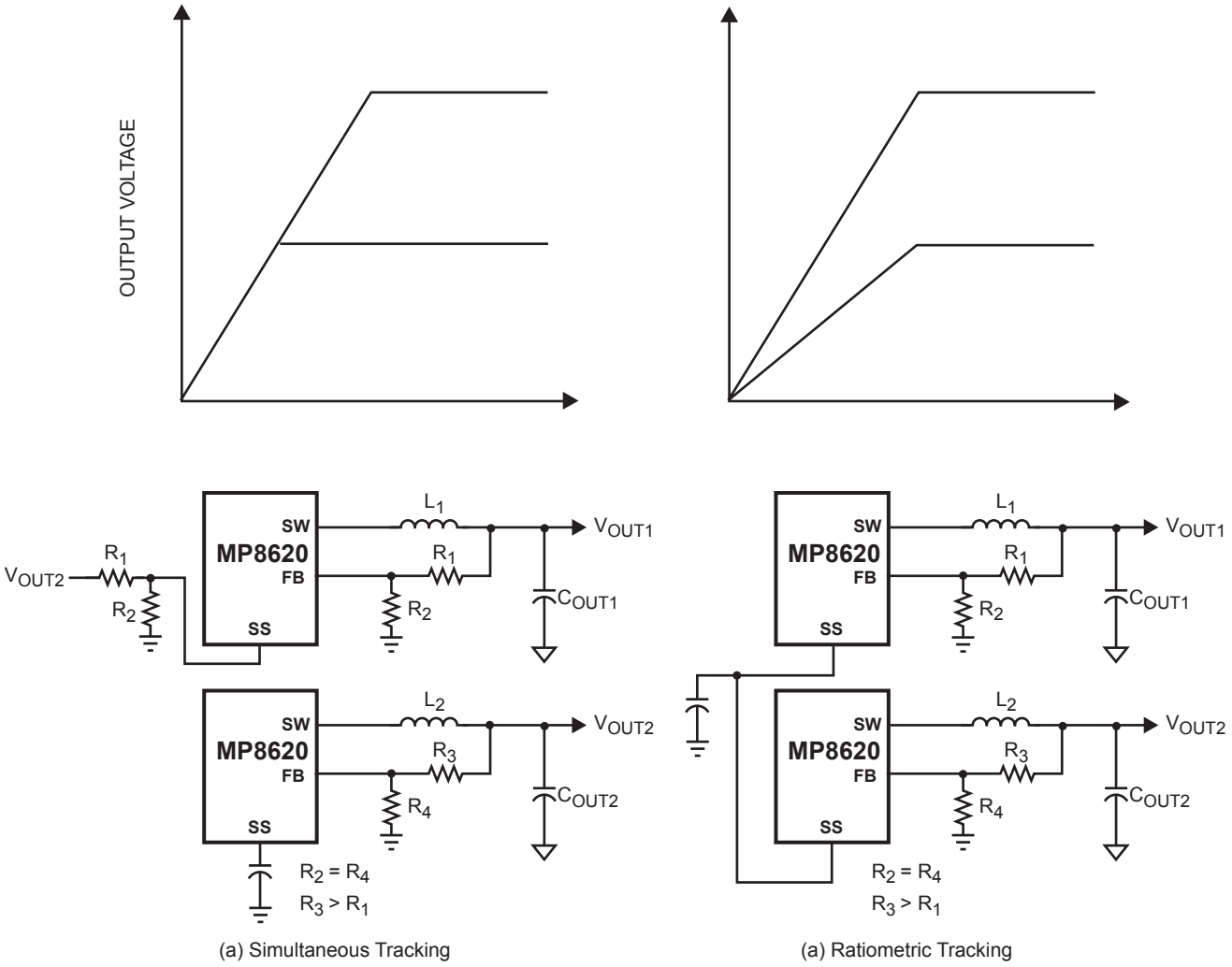


Figure 3—Output Voltage Tracking

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see the schematic on front page). Choose R1 to be around 40.2kΩ. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1}$$

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.8	40.2 (1%)	32.4 (1%)
2.5	40.2 (1%)	19.1 (1%)
3.3	40.2 (1%)	13 (1%)
5	40.2 (1%)	7.68 (1%)

Selecting the Inductor

A 0.2μH to 1μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. Inductors with lower DC resistance is preferred to get higher efficiency. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_{SW}}$$

Where ΔI_L is the inductor ripple current.

Choose inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 200mA, larger inductance is recommended for improved efficiency.

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance. In the layout, it's recommended to put the input capacitors as close as to the VIN pin.

The capacitance varies significantly over temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable over temperature.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2}$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is input voltage ripple requirement in the system design, choose the input capacitor that meets the specification.

The input voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \cdot C_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$\Delta V_{IN} = \frac{1}{4} \cdot \frac{I_{OUT}}{f_{SW} \cdot C_{IN}}$$

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCON capacitors are recommended. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot \left(R_{ESR} + \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}}\right)$$

Where R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \cdot f_{SW}^{\ 2} \cdot L \cdot C_{OUT}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of POSCON capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot R_{ESR}$$

Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30~40% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_{SW} \cdot \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where ΔL is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2f_{SW} \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Loop Compensation (Power Stage)

MP8620 employs average current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP pin is the output of the internal error amplifier. A series capacitor-resistor combination sets a pole-zero combination to compensate the characteristics of the control system. In Fig. 4, it shows a model that gives a good first-order approximation of the system. The control to output gain of the model can be expressed as follows:

$$H_{CO}(s) = \frac{V_{IN} \cdot F_m \cdot K_{LC}(s)}{1 + V_{IN} \cdot F_m \cdot G_{CS}(s)} \quad (1)$$

F_m is the modulation gain, which is

$$\frac{Dmax}{Vslope} = \frac{0.9V}{1.1V} \quad (2)$$

$K_{LC}(s)$ is the output LC filter transfer function, which is:

$$K_{LC}(s) \approx \frac{1 + s \cdot ESR \cdot C_{OUT}}{1 + s \cdot \frac{L + R_o \cdot C_{OUT} \cdot (ESR + DCR)}{R_o} + s^2 \cdot L \cdot C_{OUT}} \quad (3)$$

Where R_O is the equivalent output impedance, which equals to $\frac{V_{OUT}}{I_{OUT}}$ (4)

$G_{CS}(s)$ is the current sensing gain, which is

$$G_{CS}(s) = \frac{1 - K_{LC}(s)}{\frac{L}{DCR} \cdot s + 1} \cdot A_{CS} \cdot \frac{R_7}{R_6 + R_7} \cdot \frac{1}{2\pi \cdot R_{LPS} \cdot C_{LPS}} \quad (5)$$

Where A_{CS}=30

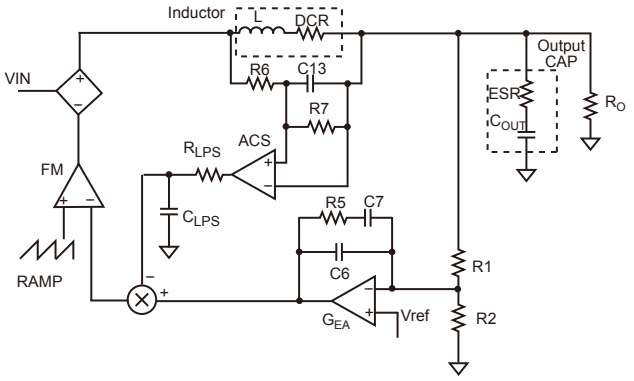


Figure 4

Loop Compensation (Type II Compensator)

1. The first step to compensate a power system is to choose a target cut-off frequency (f_c). If f_c is set too high, the system is easy to be unstable; if it's too low, the transient response performance is poor. It is recommended to keep f_c within the range of 1/10~1/4 of the switching frequency.
2. Choose the compensation resistor (R5) to set the desired f_c. R5 can be determined as:

$$R5 = \frac{R1}{\left|H_{CO}(fc)\right|} \quad (6)$$

   Where R1 is the FB upper resistor. It's recommended to choose R1 value within the range of 20kΩ-50kΩ.

3. Choose the compensation capacitor (C7) to achieve the desired phase margin. It's recommended to put the compensation zero (f_{Z1}) resulted from R5 and C7 around the double pole position caused by L and C_O. So C7 is determined as follow:

$$C7 = \frac{\sqrt{L \cdot C_{OUT}}}{R5} \quad (7)$$

4. Choose the second compensation capacitor (C6) to roll off the gain around the cut-off frequency. The pole resulted from R5 and C6 can be located at the frequency point of twice of fc. So C6 is determined as follows:

$$C6 = \frac{1}{4 \cdot \pi \cdot fc \cdot R5} \quad (8)$$

Loop compensation (Type III Compensator)

If the system loop response can't meet the specification with type II loop compensation, then a pair of zero and pole can be introduced.

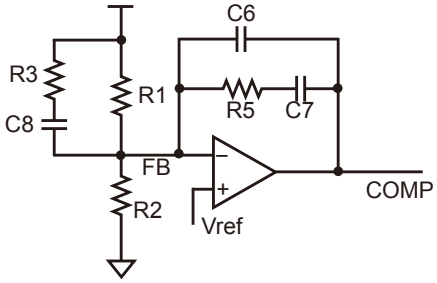


Figure 5

This is type III loop compensation. In Fig2, R3 and C8 form the additional zero (f_{Z2}) and pole (f_{P2}).

It's suggested to place f_{Z2} at half of fc and f_{P2} at twice of f_c. Then R3 and C8 can be determined as follows:

$$C8 = \frac{1}{\pi R1 \cdot fc} \quad (9)$$

$$R3 = \frac{1}{4\pi \cdot C8 \cdot fc} \quad (10)$$

In table 2, it lists the typical values of compensation components for some standard output voltages. The values of the compensation components have been optimized for fast transient responses and good stability at given conditions.

Table 2

Vin (V)	V_{OUT}(V)	f_S(kHz)	C_{OUT}(µF)	R1(kΩ)	R5(kΩ)	C7(pF)	C6(pF)	C8(pF)	R3(kΩ)
12	1.2	300	470	40.2	49.9	220	27	120	0.05
12	3.3	300	470	40.2	64.9	220	27	120	0.05

Layout Recommendation

1) The high current paths (GND, IN and SW) should be placed very close to the device with short, direct and wide traces.
2) Put the input capacitors as close as possible to the IN and GND pins.
3) Put the decoupling capacitor as close as possible to the VCC and GND pins.
4) Keep the switching node SW short and away from the feedback network.
5) The external feedback resistors should be placed next to the FB pin. Make sure to route the FB trace away from the noisy SW node and GND.
6) Keep the BST voltage path (BST, CBST and SW) as short as possible.
7) Four layer layouts are recommended to achieve better thermal performance.
8) SYNCIN pin is very noise sensitive. Be sure to route it away from noisy source, e,g, SW pads, BST pads. It's recommended to pour some GNP pads around the SYNCIN resistor to improve the noise immunity.

Multi-Phase Configuration

MP8620 can be configured into two-phase, three-phase and four-phase operation as follows:

a. Pull FB to V_{CC} to force the IC as slave IC. The EAMP of the slave IC is in high Z state after its FB is pulled high.
b. Connect the COMP pin of slave IC to the COMP pin of the master IC as shown in Figure 6.
c. The SYNCOUT of the master IC provides clock signal to the slave IC. The phase delay between the master IC clock and the slave IC clock can be programmed by adjusting the voltage at PD of the master IC as shown in Table 3:

Table 3

V_{PD} (V)	Phase Delay
V_{PD}<1	180°
1<V_{PD}<3	120°
V_{PD}>3	90°

d. Repeat steps a-c above to configure more phases if needed.

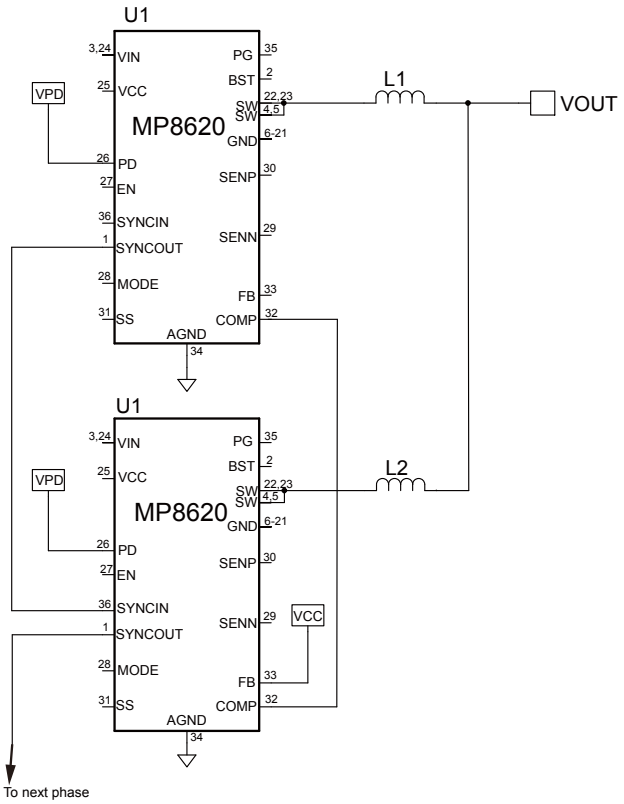


Figure 6

BST Resistor Selection

During operation, high voltage spike may be recorded at the SW node, due to high dv/dt when the HSFET is turned on. A BST resistor (R_BST shown in Figure 7) is recommended to be placed in series with the BST capacitor (C_BST shown in Figure 7) to slow down the switching speed of the HSFET to reduce the voltage spike. The R_BST should be chosen that at any desired input voltage and with any output current, the voltage spike at the SW node should not exceed the absolute maximum value specified in the section of "ABSOLUTE MAXIMUM RATINGS". In typical application conditions, a resistor value of 4.7Ω is enough.

When determining the voltage spike at the SW node, care should be taken on the measurements to ensure accurate results. It's recommended to use a low capacitance oscilloscope probe (e.g. 1.5pF). The measurement loop between SW node and GND pad should be as small as possible. An example of measuring the SW spike in a small measurement loop is shown on figure 8.

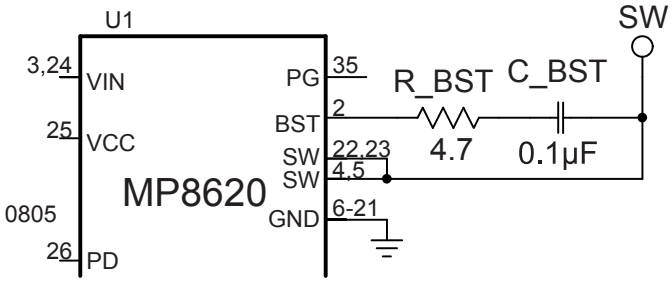
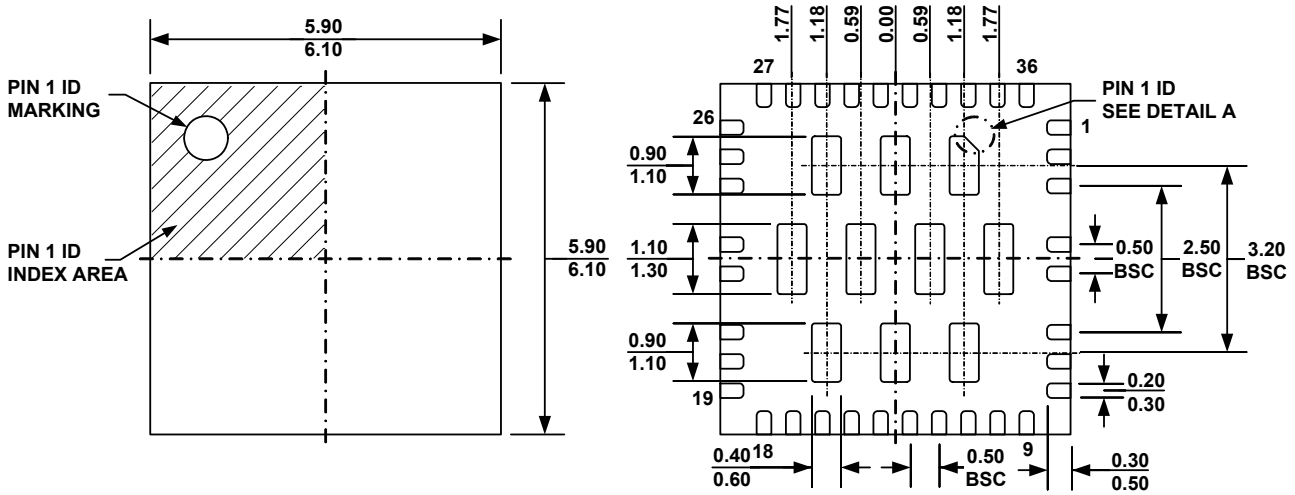


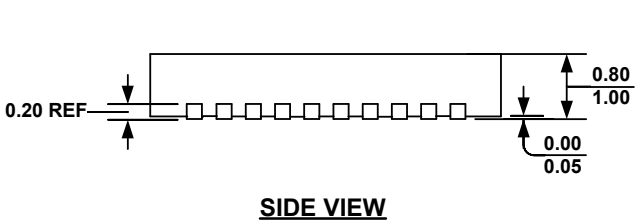
Figure 7

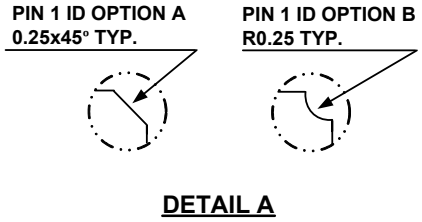
Figure 8

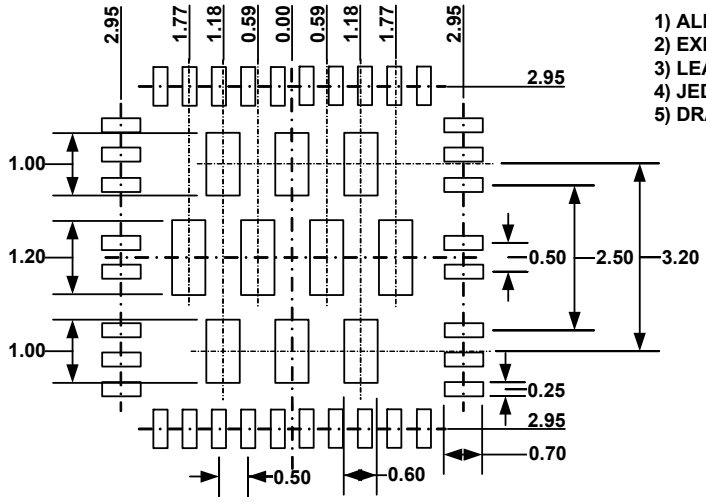
PACKAGE INFORMATION

QFN (6x6mm)









NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-220, VARIATION VJJD-2.
5) DRAWING IS NOT TO SCALE.

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