MPM3860

1.2MHz Synchronous 2.75-7V,6A Ultra-Thin Power Module

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MPM3860 is a fully-integrated high-frequency, synchronous rectified, step-down, power module with internal inductor. It offers a very compact solution to achieve a 6A continuous output current over a wide input range, with excellent load and line regulation. The MPM3860 has synchronous-mode operation for higher efficiency over the output current-load range.

Constant On-Time control operation provides very fast transient response and easy loop design as well as very tight output regulation.

Full protection features include SCP, OCP, UVP, and thermal shutdown.

The MPM3860 requires a minimal number of readily-available, standard external components and it is available in a space-saving QFN24 4mmx6mm package.

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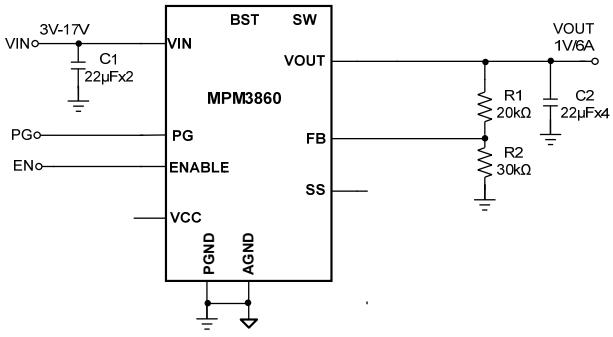
FEATURES

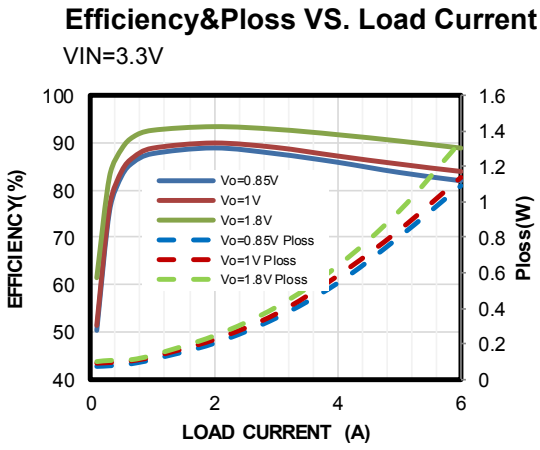
- Wide 2.75V to 7V Operating Input Range
- 6A Output Current
- Internal Power MOSFETs
- Output Adjustable from 0.6V
- High Efficiency Synchronous Mode Operation
- Pre-biased Startup
- Forced CCM Mode for Low VOUT Ripple
- Fixed 1200kHz Switching Frequency
- External Programmable Soft Startup Time
- EN and Power Good for Power Sequencing
- Over-Current Protection and Hiccup
- Thermal Shutdown
- Available in a QFN24 (4mmx6mmx1.6mm) package

APPLICATIONS

- FPGA Power System
- Optical Module
- Telecom
- Networking
- Industrial Equipment

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MPM3860GQW	QFN-24 (4mmX6mmX1.6mm)	*See Below*

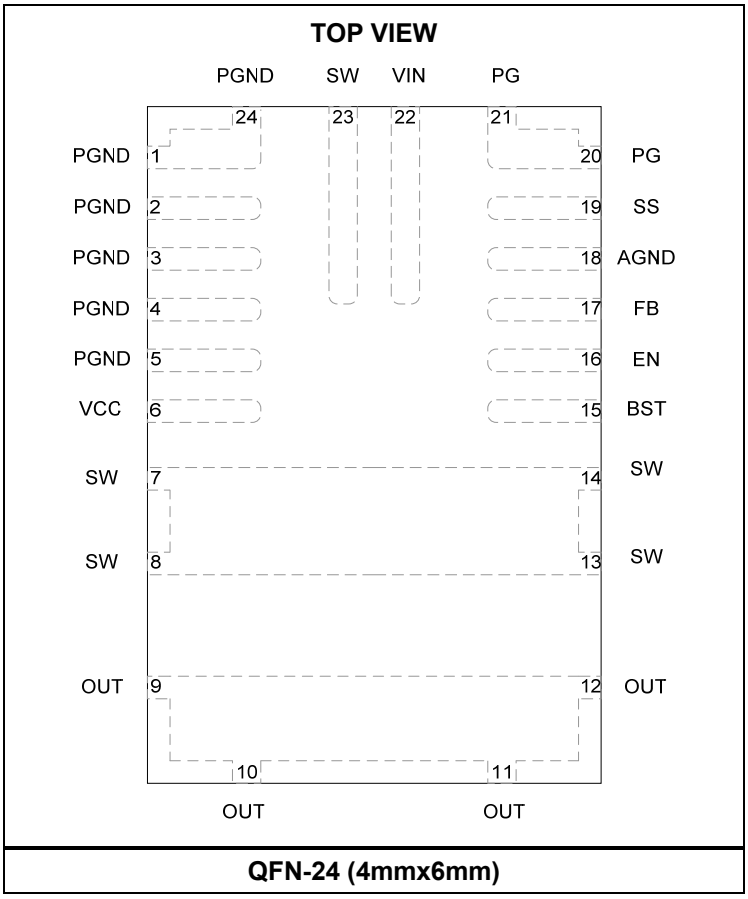
* For Tape & Reel, add suffix –Z (e.g.: MPM3860GQW–Z).

TOP MARKING

MPSYWW
MP3860
LLLLLL
M

MPS: MPS prefix
Y: Year code
W: Week code
MP3860: Part number
LLLLLL: Lot number
M: module

PACKAGE REFERENCE



QFN-24 (4mmx6mm)

PIN FUNCTIONS

QFN 4x6 Pin #	Name	Description
1,2,3,4,5,24	PGND	System Ground. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout. Suggested to be connected to GND with copper and vias.
6	VCC	Internal Bias Supply Output.
7,8,13,14,23	SW	Switch Output. Use wide PCB trace to make the connection.
9,10,11,12,	OUT	Output Pin, connect to COUT.
15	BST	Bootstrap. Internal a capacitor connected between SW and BST pins to form a floating supply across the high-side switch driver.
16	EN	Enable. Pull EN high to enable the part. When floating, EN is pulled down to GND by internal 3.3MΩ resistor so it is disabled.
17	FB	Feedback. Sets the output voltage when connected to the tap of an external resistor divider that is connected between output and GND.
18	AGND	Signal Ground. AGND is not internally connected to System Ground, make sure AGND connected to system Ground in PCB layout.
19	SS	Soft start. Connect a capacitor across SS and GND to set the soft-start time to avoid start up inrush current，An internal 22nF SS capacitor is inside.
20,21	PG	Power-Good Output. The output of this pin is an open drain output. It will change state if UVP, OCP, OTP or OV happens.
22	VIN	Supply Voltage. The part operates from a 2.75V to 7V input rail. C1 is needed to decouple the input rail. Use wide PCB trace to make the connection.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... –0.3V to +8V
V_{SW} –0.3V (-5V<10ns) to + V_{IN} +0.7V(10V<10ns)
V_{BST} ..... V_{SW} +4V
V_{EN} ..... V_{IN}
All Other Pins ..... –0.3V to +4V
Continuous Power Dissipation (TA=+25℃)(2) .....
.....4.8W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature .....-65°C to 125°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 2.75V to 7V
Output Voltage V_{OUT} ..... 0.6V to V_{IN}xD_{MAX}
Operating Junction Temp. .....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

EVM3860-QW-00A .....25.99 .. 7.18.. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation on EVM3860-QW-00A board at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on 4-layer PCB.

ELECTRICAL CHARACTERISTICS (5)

V_{IN} = 5V, T_J=-40°C to +125°C, typical value is tested at T_J=+25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage Range	V_{IN}		2.75		7	V
Supply Current						
Supply Current (Shutdown)	I_{IN}	V_{EN}=0V			5	μA
Supply Current (Quiescent)	I_q	V_{EN}=2V, V_{FB}=0.65V		100	150	μA
MOSFET						
Switch Leakage	SW_{LKG}	V_{EN}=0V, V_{SW}=7V			1	μA
Current Limit						
Valley Current Limit	I_{LIMIT_VY}			7		A
Short Hiccup Duty Cycle(6)	D_{HICCUP}			10		%
Switching Frequency and Minimum On/Off Timer						
Switching frequency	Fs			1.2		MHz
Minimum On Time(6)	$T_{On\ MIN}$			50		ns
Minimum Off Time(6)	$T_{Off\ MIN}$			100		ns
Reference and Soft Start						
Feedback Voltage	V_{FB}	T_J=25°C	594	600	606	mV
		T_J=-40°C to +125°C	591	600	609	
Feedback Current	I_{FB}	V_{FB}=700mV		10	50	nA
Soft Start Current	I_{SS_START}			6		μA
Enable and UVLO						
EN Rising Threshold	$V_{EN\ RISING}$			1.22		V
EN Falling Threshold	$V_{EN\ FALLING}$			1		V
EN Pin Pull-Down Resistor	R_{EN_PD}			3.3		MΩ
VCC						
VCC Under Voltage Lockout Threshold Rising	VCC_{Vth}			2.47		V
VCC Under Voltage Lockout Threshold	VCC_{HYS}			100		mV
VCC Regulator	V_{CC}	VIN=5V		3.5		V
VCC Load Regulation	Reg_{VCC}	I_{CC}=5mA		3		%
Power Good						
Power-Good UV Rising Threshold	$PGUV_{vth\_Hi}$		0.85	0.9	0.95	V_{FB}
Power-Good UV Falling Threshold	$PGUV_{vth\_Lo}$		0.75	0.80	0.85	V_{FB}
Power-Good OV Rising Threshold	$PGOV_{vth\_Hi}$		1.15	1.2	1.25	V_{FB}
Power-Good OV Falling Threshold	$PGOV_{vth\_Lo}$		1.05	1.1	1.15	V_{FB}
Power-Good Delay	PG_{Td}	Both edge		50		μs

ELECTRICAL CHARACTERISTICS (5) *(continued)*

V_{IN} = 5V, T_J=-40°C to +125°C, typical value is tested at T_J=+25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power-Good Sink Current Capability	V_{PG}	Sink 4mA			0.4	V
Power Good Leakage Current	I_{PG_LEAK}	V_{PG}=5V			10	μA
Thermal Protection						
Thermal Shutdown(6)	T_{SD}			150		°C
Thermal Hysteresis(6)	T_{SD-HYS}			20		°C

Notes:

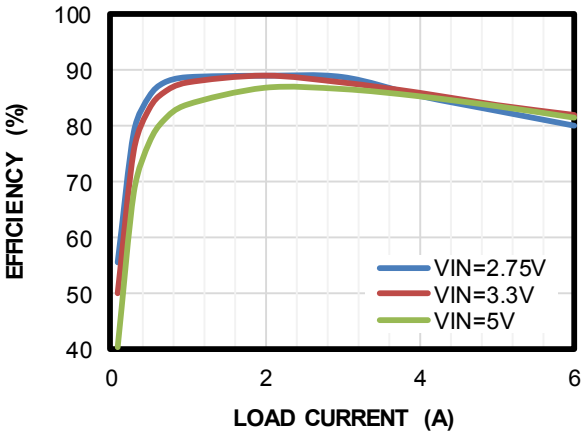
5) Not tested in production and guaranteed by over-temperature correlation.

6) Guaranteed by design and characterization test.

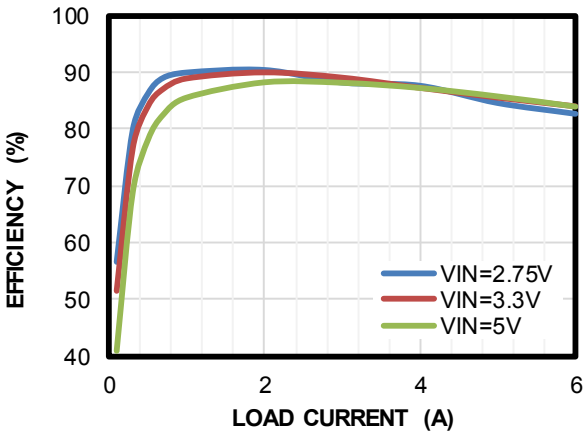
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1V, COUT=4x22uF, f_S=1200kHz, T_A = 25°C, unless otherwise noted.

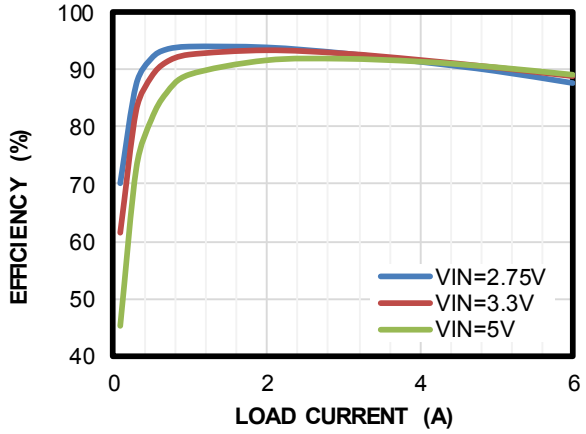
Efficiency vs. Load Current
V_{OUT} = 0.85V



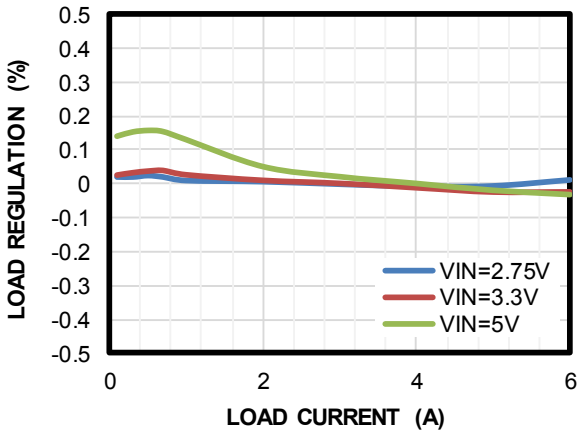
Efficiency vs. Load Current
V_{OUT} = 1V



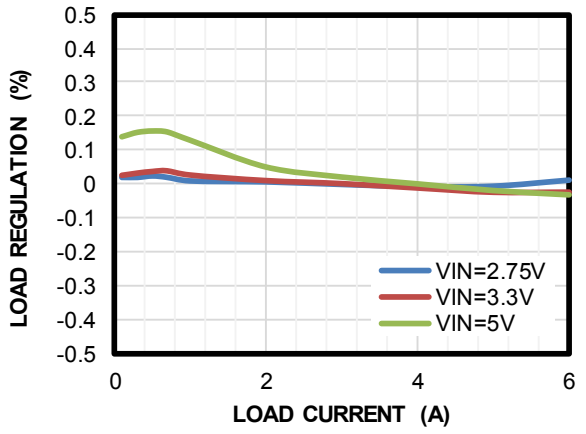
Efficiency vs. Load Current
V_{OUT} = 1.8V



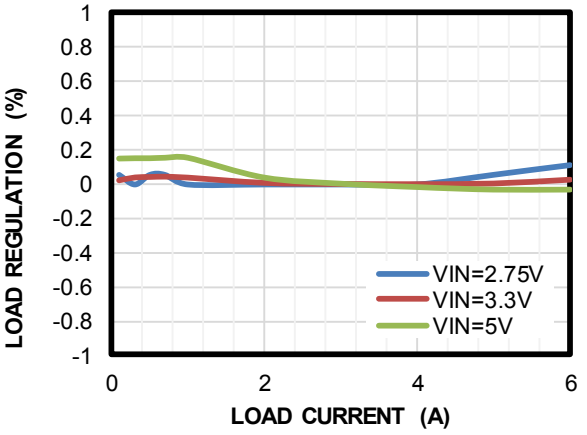
Load regulation vs. Load Current
V_{OUT} = 0.85V



Load regulation vs. Load Current
V_{OUT} = 1V



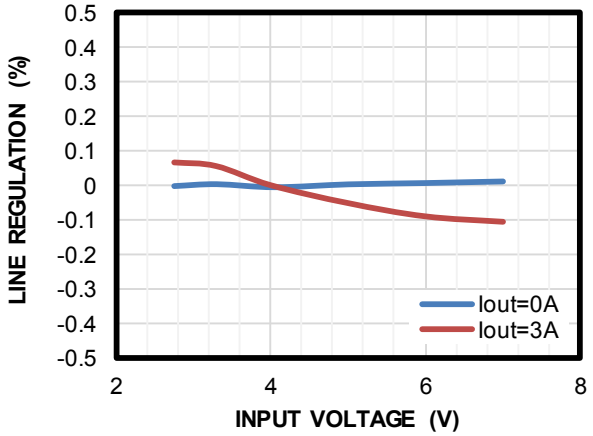
Load regulation vs. Load Current
V_{OUT} = 1.8V



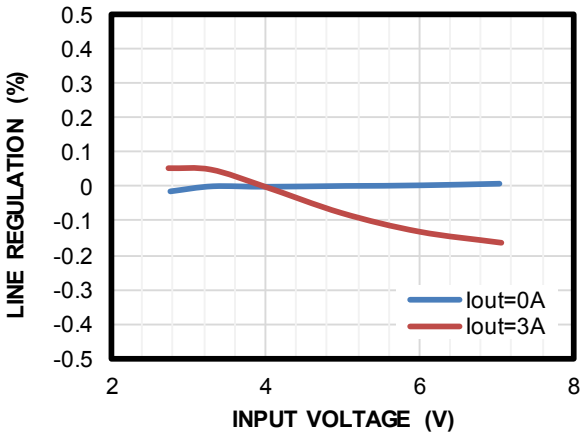
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, COUT=4x22uF, f_S=1200kHz, T_A = 25°C, unless otherwise noted.

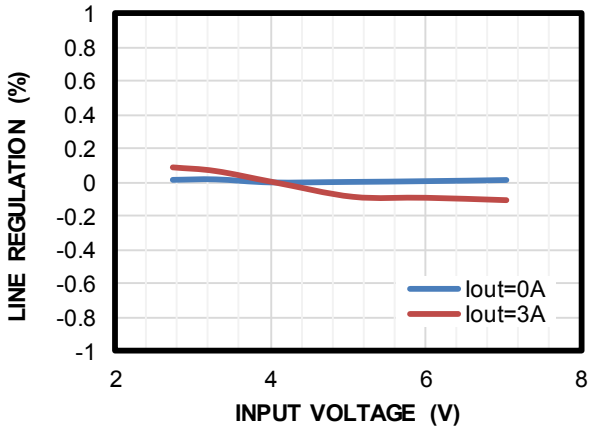
Line regulation vs. Input Voltage
V_{OUT} = 0.85V



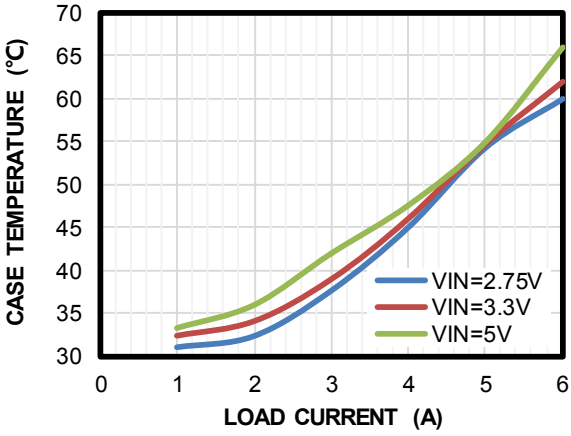
Line regulation vs. Input Voltage
V_{OUT} = 1V



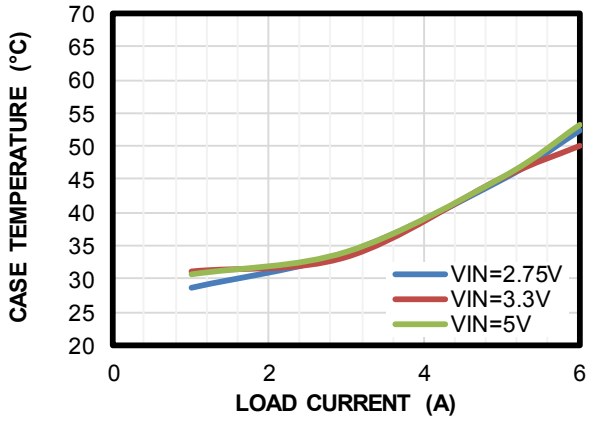
Line regulation vs. Input Voltage
V_{OUT} = 1.8V



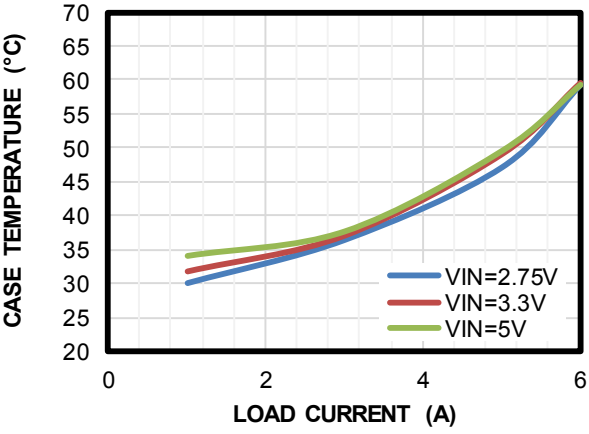
Thermal
V_{OUT} = 0.85V



Thermal
V_{OUT} = 1V



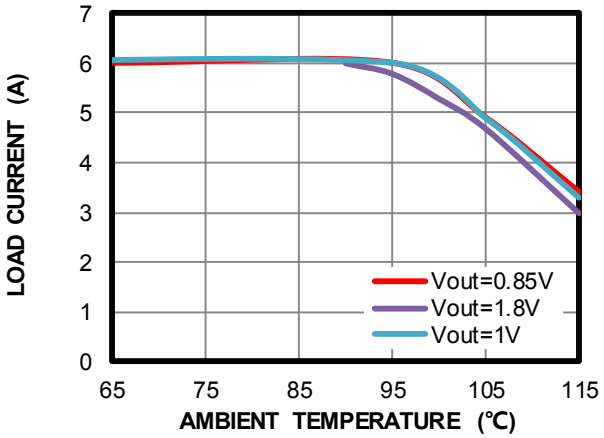
Thermal
V_{OUT} = 1.8V



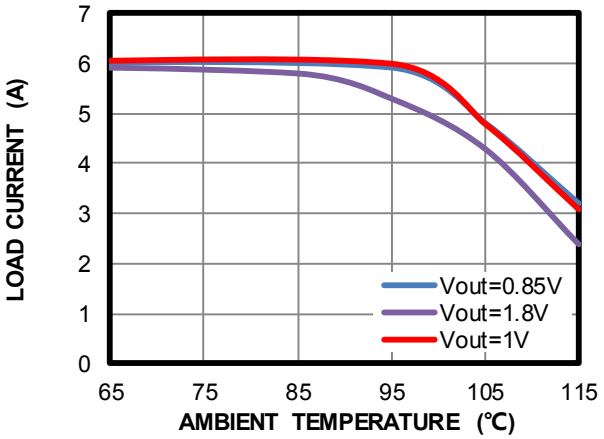
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, COUT=4x22uF, f_S=1200kHz, T_A = 25°C, unless otherwise noted.

Thermal Derating
V_{IN} = 3.3V



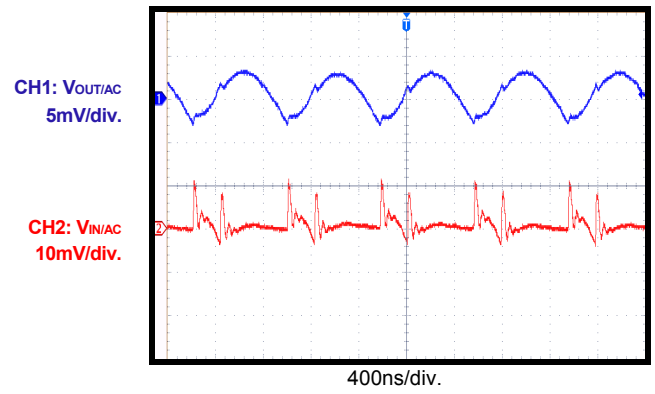
Thermal Derating
V_{IN} = 5V



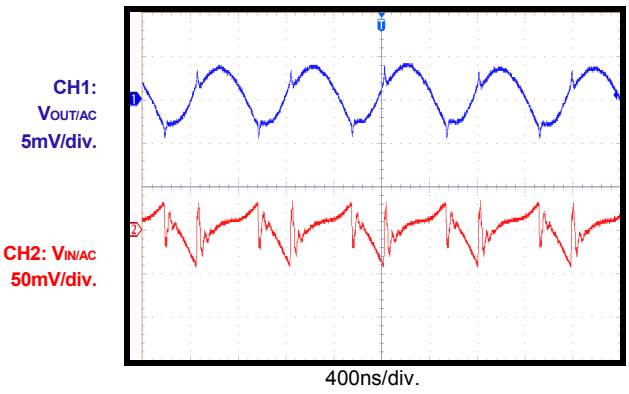
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, COUT=4x22uF, f_S=1200kHz, T_A = 25°C, unless otherwise noted.

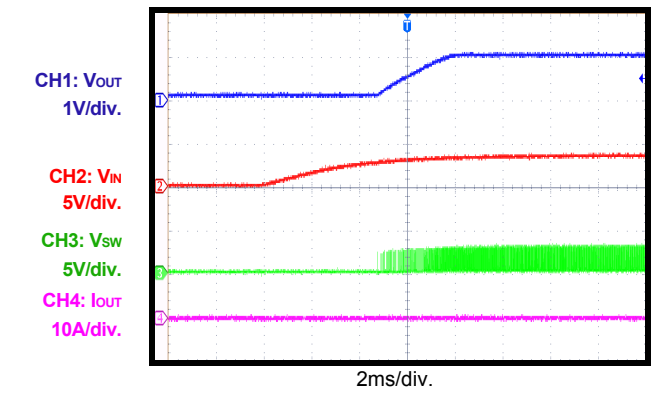
Vo Ripple
I_{OUT} = 0A



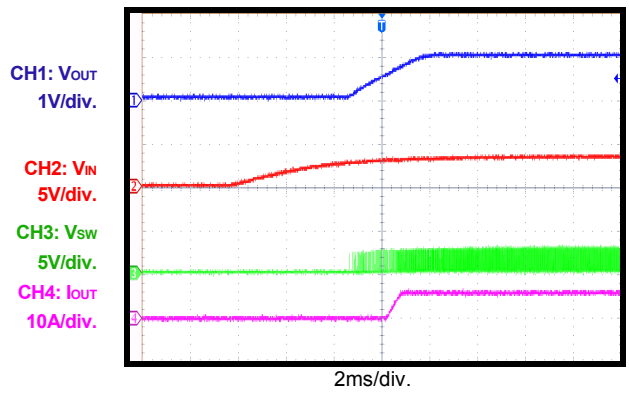
Vo Ripple
I_{OUT} = 6A



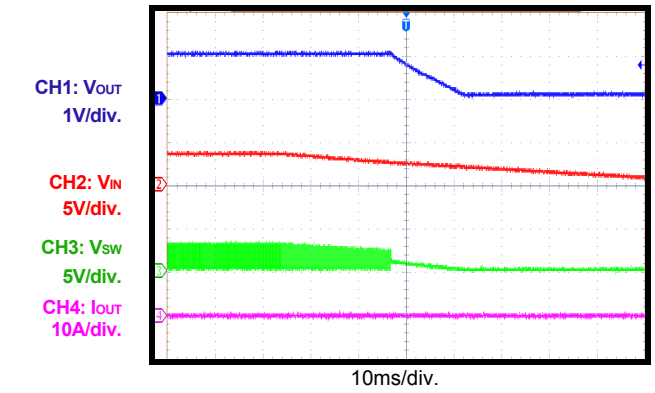
Vin On
I_{OUT} = 0A



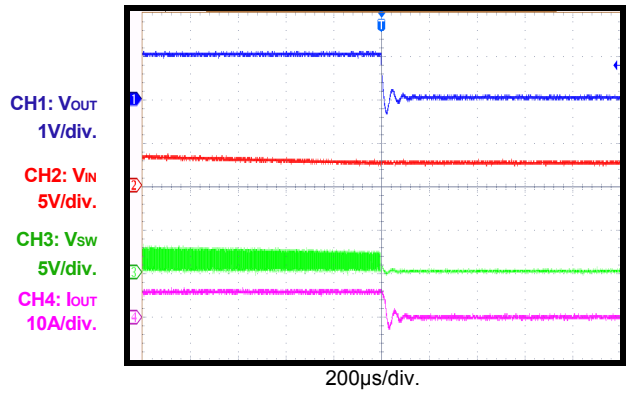
Vin On
I_{OUT} = 6A



Vin off
I_{OUT} = 0A



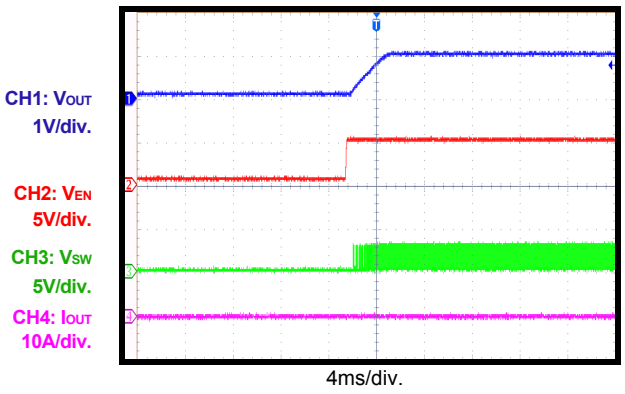
Vin off
I_{OUT} = 6A



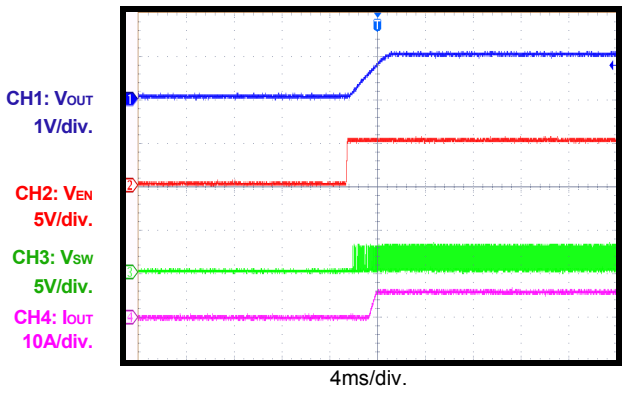
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, COUT=4x22uF, f_S=1200kHz, T_A = 25°C, unless otherwise noted.

EN ON
I_{OUT} = 0A



EN ON
I_{OUT} = 6A



EN OFF
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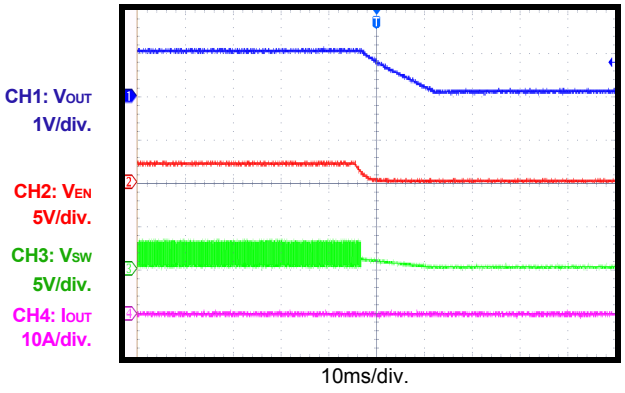
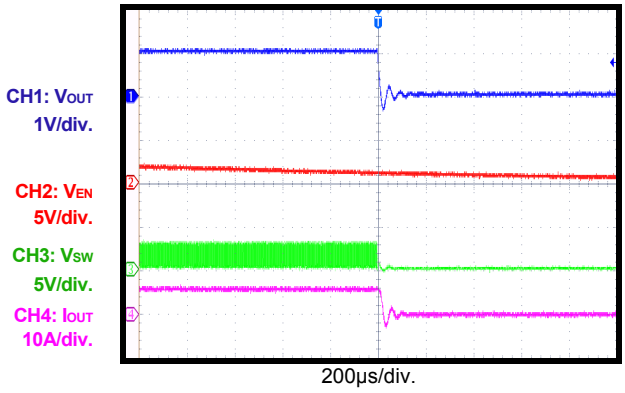
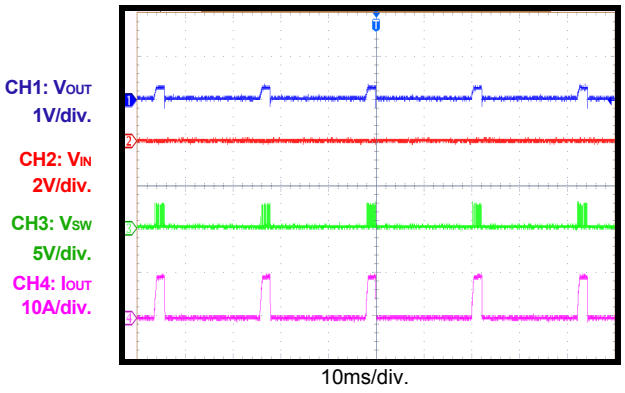


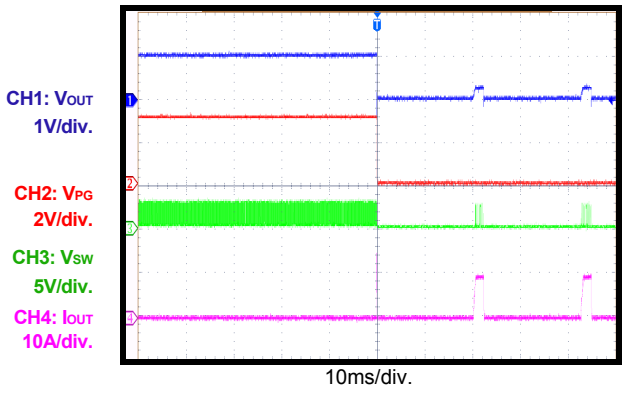
EN OFF
I_{OUT} = 6A



SCP Steady state



SCP entry
I_{OUT} = 0A

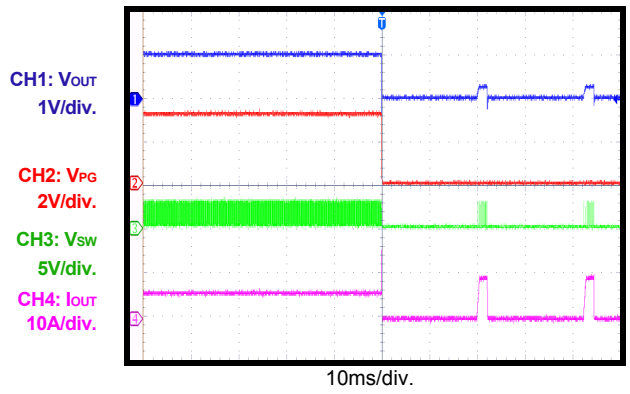


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, COUT=4x22uF, f_S=1200kHz, T_A = 25°C, unless otherwise noted.

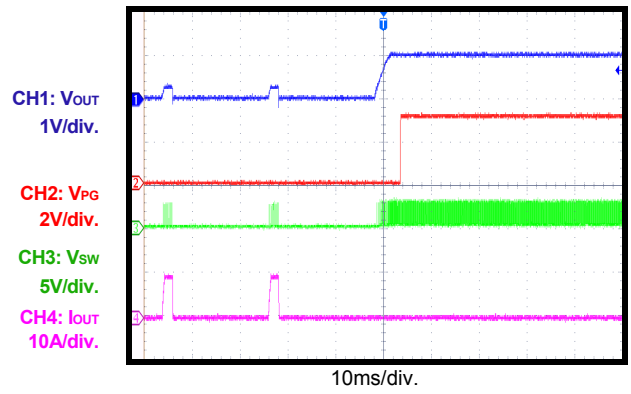
SCP entry

I_{OUT} = 6A



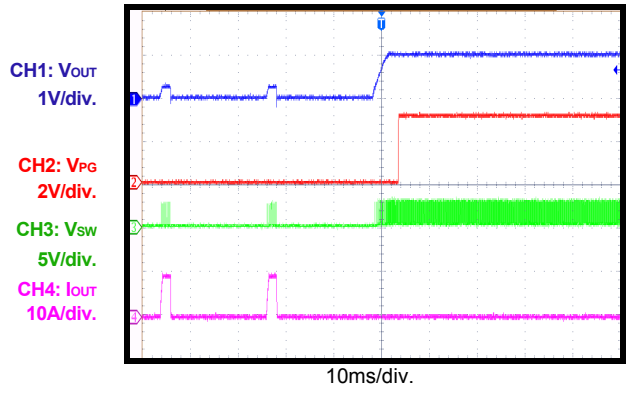
SCP recorvery

I_{OUT} = 0A



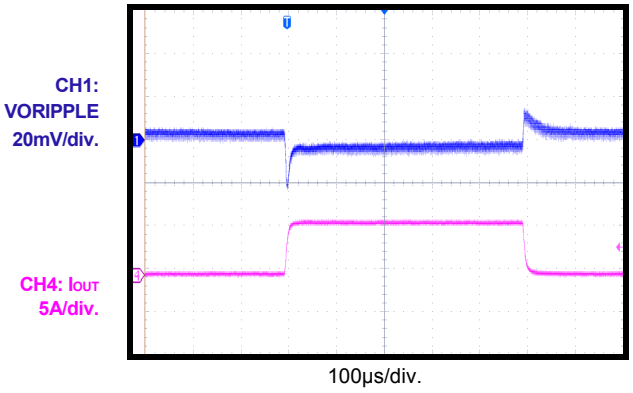
SCP recorvery

I_{OUT} = 6A



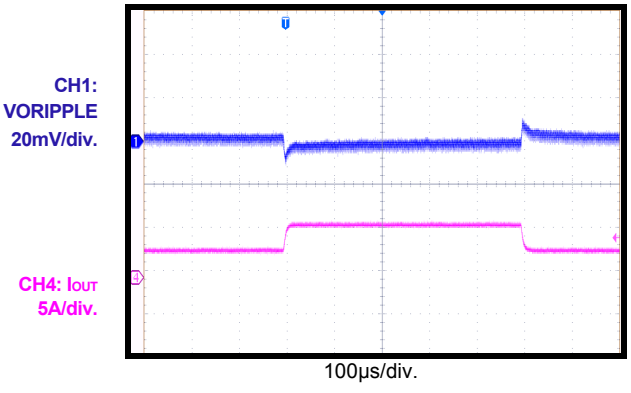
Transient

I_{OUT} = 0-6A



Transient

I_{OUT} = 3-6A



BLOCK DIAGRAM

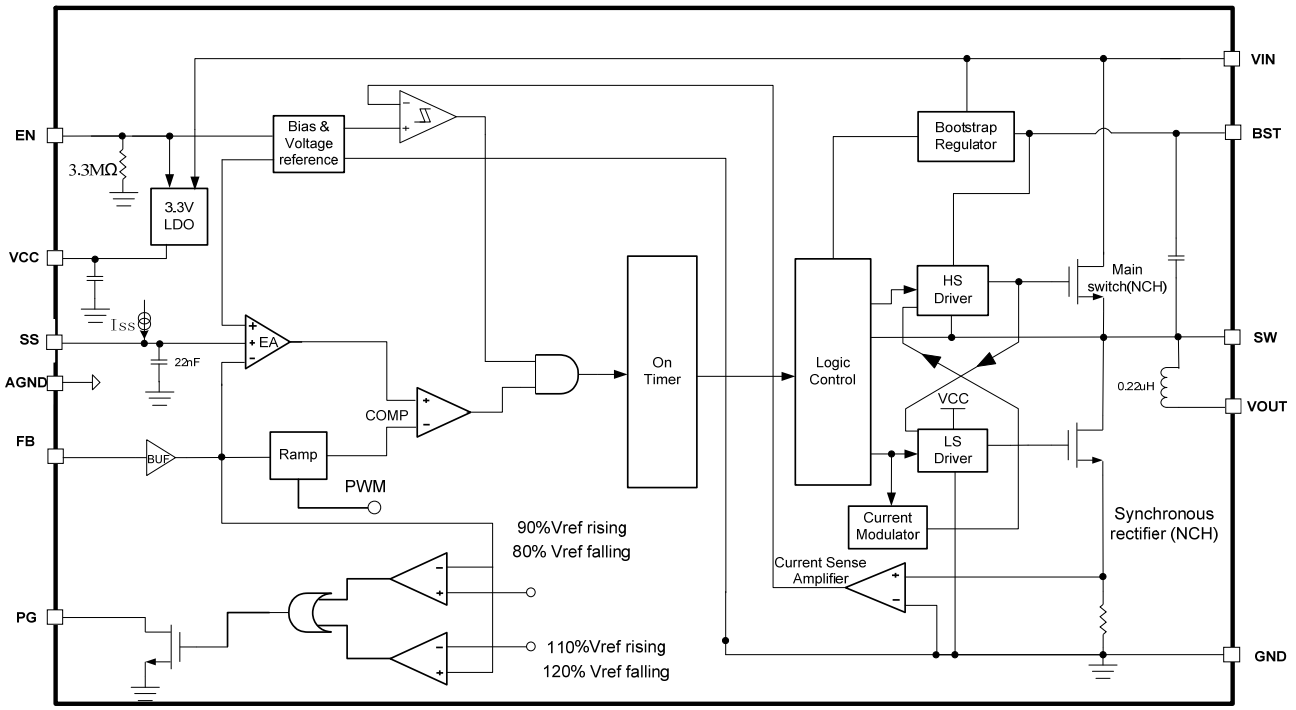


Figure 1: Functional Block Diagram

OPERATION

The MPM3860 is fully integrated synchronous rectified step-down switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. Figure 2 shows the simplified ramp compensation block in MPM3860, at the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON when the feedback voltage (VFB) is below the reference voltage (VREF), which indicates insufficient output voltage. The ON period is determined by both the output voltage and input voltage to make the switching frequency fairy constant over input voltage range.

After the ON period elapses, the HS-FET is turned off, or becomes OFF state. It is turned ON again when VFB drops below VREF. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its OFF state to minimize the conduction loss. There will be a dead short between input and GND if both HS-FET and LS-FET are turned on at the same time. It's called shoot-through. In order to avoid shoot-through, a dead-time (DT) is internally generated between HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

An internal compensation is applied for COT control to make a more stable operation even when ceramic capacitors are used as output capacitors, this internal compensation will then improve the jitter performance without affect the line or load regulation.

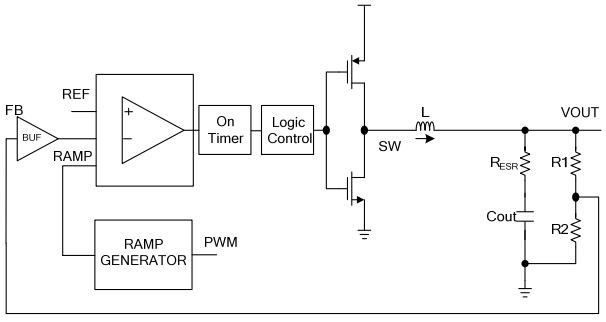


Figure 2: Simplified Ramp Compensation Block

CCM Operation

When the output current is high and the inductor current is always above zero amps, it is called continuous-conduction-mode (CCM). The CCM mode operation is shown in Figure 3 shown. When V_{FB} is below V_{EAO}, HS-MOSFET is turned on for a fixed interval which is determined by one- shot on-timer. When the HS-MOSFET is turned off, the LS-MOSFET is turned on until next period.

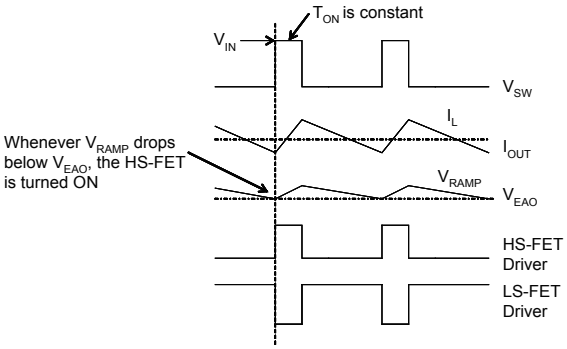


Figure 3: Heavy Load Operation

In CCM mode operation, the switching frequency is fairly constant and it is called PWM mode.

VCC Regulator

The 3.5V internal regulator power most of the internal circuits. This regulator takes the V_{IN} input and operates in the full V_{IN} range: When V_{IN} exceeds 3.5V, the output of the regulator is in full regulation; when V_{IN} falls below 3.5V, the output of the regulator decreases following the V_{IN}. An internal 1μF decoupling ceramic capacitor is inside.

Enable

EN is a digital control pin that turns the regulator on and off: Drive EN higher than 1.22V to turn on the regulator, drive it lower than 1V to turn it off.

When floating, EN is pulled down to GND by an internal 3.3MΩ resistor.

EN can be connected directly to V_{IN}. It support 17V input range.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage.

The MPM3860 UVLO comparator monitors the output voltage of the internal regulator VCC.

VCC UVLO rising threshold is about 2.47V while its falling threshold is 2.37V.

When the input voltage is higher than the UVLO rising threshold voltage, the MPM3860 powers up. It shuts off when the input voltage is lower than the UVLO falling threshold voltage. This is non-latch protection.

Soft Start

MPM3860 employs a soft start (SS) mechanism to ensure smooth output ramping during power up. When the EN pin goes high, an internal current source (6μA) charges up the SS capacitor. The SS capacitor voltage takes over the REF voltage to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. Once SS voltage rises above the V_{REF}, it continues to ramp up REF voltage takes over. At this point, the soft start finishes and it enters steady state operation.

The SS capacitor value can be determined as follows:

$$C_{ss}(nF) = 0.83 \times \frac{T_{ss}(ms) \times I_{ss}(uA)}{V_{REF}(V)} \quad (1)$$

An internal 22nF SS capacitor is inside.

If the output capacitance is large value, it is not recommended to set the SS time too short. Otherwise, it's easy to hit the current limit during SS.

Power Good Indicator

The PG pin is the open drain of a MOSFET that connects to VCC or some other voltage source through a resistor (eg. 100kΩ). The MOSFET turns on with the application of an input voltage so that the PG pin is pulled to GND before SS is ready. After FB voltage reaches 90% of VREF, the PG pin is pulled high after a 50μs delay. When the FB voltage drops to 80% of VREF, the PG pin will be pulled low.

When UVLO or OTP happens, the PG pin will be pulled low immediately; When OC (Over current) happens, the PG pin will be pulled low when VFB drops below 80% of VREF after 0.05ms delay; When OV happens, PG pin will be pulled low when VFB rise above 120% of VREF after 0.05ms delay. If VFB fall back below 110% of VREF, PG pin will be pulled high after 0.05ms delay.

If the input supply fails to power the MPM3860, PG is clamped low, even though PG is tied to an external DC source through a pull-up resistor. The relationship between the PG voltage and the pull-up current is shown in Figure 4.

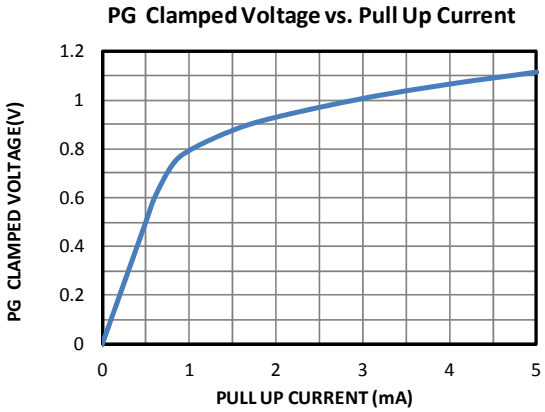


Figure 4: PG Clamped Voltage vs. Pull up Current

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

MPM3860 has valley limit control. LS-FET will monitor the current flow through the LS-FET. HS-FET will wait until valley current limit disappear to turn on again. Meanwhile, the output voltage drops until VFB is below the under-voltage (UV) threshold—typically 50% below the reference. Once UV is triggered, the MPM3860 enters hiccup mode to periodically restart the part.

During over-current protection, the device tries to recover from over-current fault with hiccup mode. That means the chip will disable output power stage, discharge soft-start cap and then automatically try to soft-start again. If the over-current condition still holds after soft-start ends, the device repeats this operation cycle till over-current conditions disappear and then output rises back to regulation level. So the OCP is non-latch protection.

Pre-bias startup

The MPM3860 has been designed for monotonic startup into pre-biased loads.

If the output is pre-biased to a certain voltage during startup, the BST voltage will be refreshed and charged, the voltage on the soft-start capacitor will be charged too. If BST voltage exceeds its rising threshold voltage and Soft-start capacitor voltage exceeds the sensed output voltage at the FB pin, the part starts to work normally.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, it shuts down the whole chip. When the temperature falls below its lower threshold (typically 130°C) the chip is enabled again.

Start-Up and Shutdown Circuit

If both V_{IN} and EN exceed their respective thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. The shutdown procedure starts by initially blocking the signaling path to avoid any fault triggering. The internal supply rail is then pulled down.

APPLICATIONINFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider is used to set the output voltage. First, choose a value for R2. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It is recommended to choose a value within 2kΩ- 100kΩ for R2. Typically, set the current through R2 less than 250uA will make a good balance between system stability and also the no load loss. Then R1 is determined as follow:

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (2)$$

The feedback circuit is shown as Figure 5.

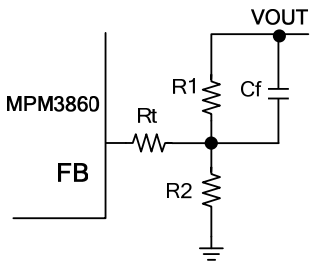


Figure 5: Feedback Network

Table 1: Resistor Selection for Common Output Voltages

V_{OUT}(V)	R1(kΩ)	R2(kΩ)	Cf(pF)	Rt(kΩ)
1.0	20	30	39	0
1.2	20	20	39	0
1.5	20	13	39	0
1.8	20	10	39	0
2.5	20	6.34	39	0
3.3	20	4.42	39	0

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (4)$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Under worst-case conditions where $V_{IN} = 2V_{OUT}$:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (6)$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (7)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (9)$$

Besides considering the output ripple, chose larger output capacitor also can get better load transient response, but maximum output capacitor limitation should be also considered in design application. If the output capacitor value is too high, the output voltage can't reach the design value during the soft-start time, and then it will fail to regulate. The maximum output capacitor value C_{o_max} can be limited approximately by:

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (10)$$

Where, I_{LIM_AVG} is the average start-up current during soft-start period. T_{ss} is the soft-start time.

PC Board Layout (7)

PCB layout is critical for stable operation. For best results, refer to recommended layout showed in Figure 6 and follow the guidelines below:

1. Keep the power loop as small as possible.
2. Use a large ground plane to connect directly to PGND. If the bottom layer is a ground plane, add vias near PGND.
3. Ensure the high-current paths at GND and VIN have short, direct, and wide traces.
4. Place the ceramic input capacitor, especially the small package size (0402) input bypass capacitor as close to VIN and PGND pins as possible to minimize high frequency noise. Keep the input capacitor and IN as short and wide as possible.
5. Place the VCC capacitor to VCC pin and GND pin as close as possible.
6. Connect VIN, VOUT and GND to a large copper area to cool the chip to improve thermal performance and long-term reliability.
7. Separate input GND are from other GND area at top layer, and connect them together at internal layers and bottom layer through multiple vias.
8. Ensure an integrate GND are at internal layer or bottom layer.
9. A four-layer layout is recommended to achieve better thermal performance. Use multiple vias to connect the power planes to internal layers.

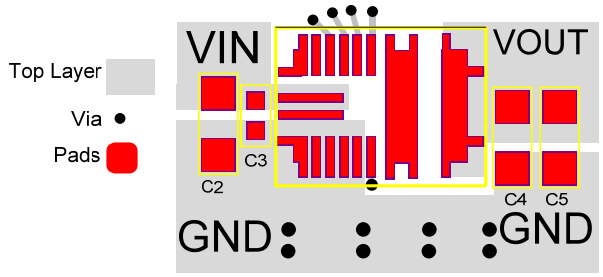


Figure 6: PC Board Layout

Note:

7) The recommended layout is based on the Typical Application circuit on the next page.

TYPICAL APPLICATION CIRCUITS

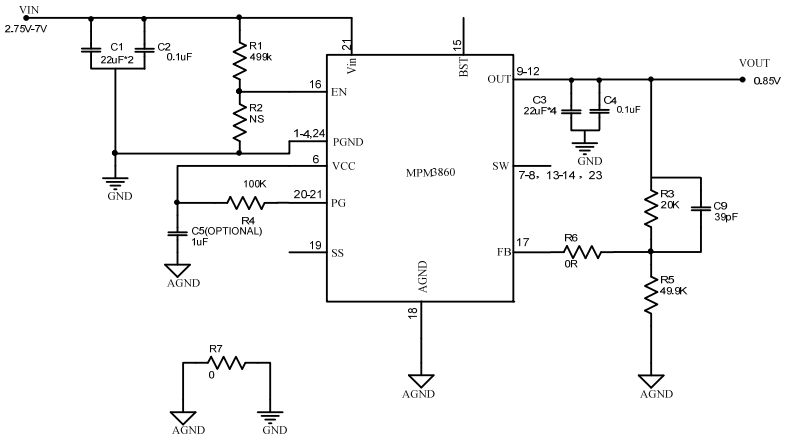


Figure 7: Typical application circuits with 0.85V output

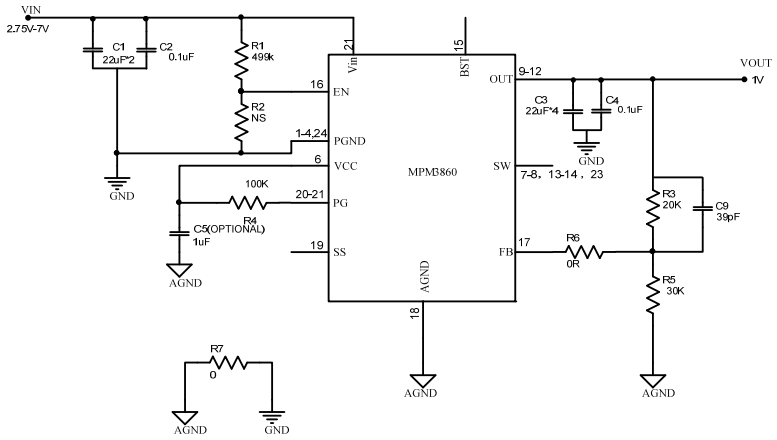


Figure 8: Typical application circuits with 1V output

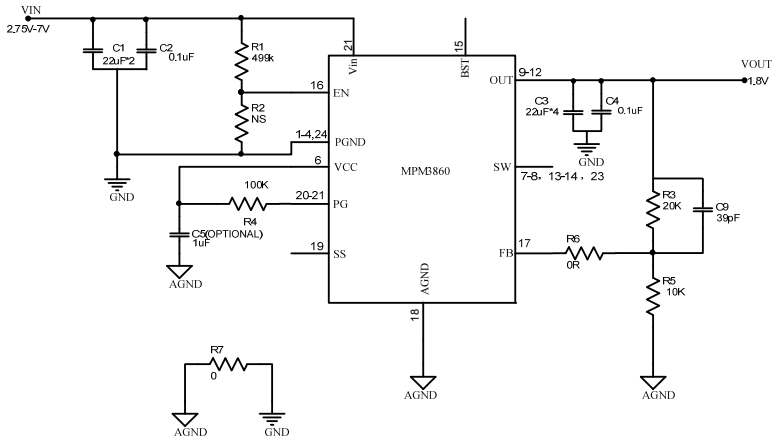
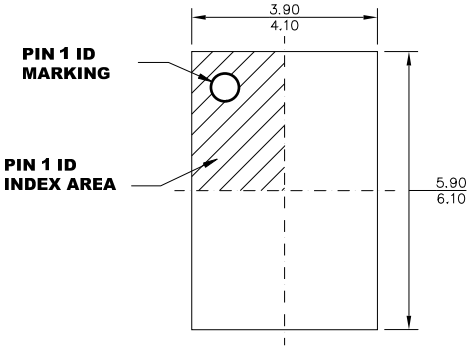


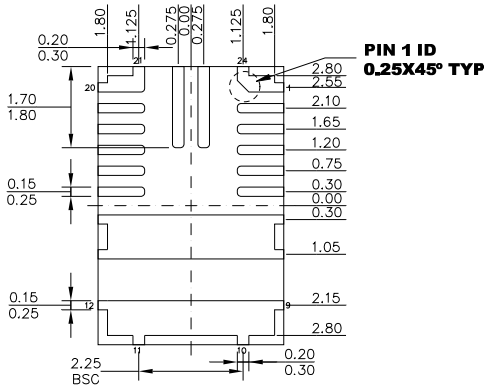
Figure 9: Typical application circuits with 1.8V output

PACKAGE INFORMATION

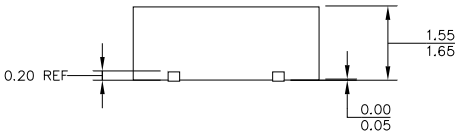
QFN-24 (4mmx6mm)



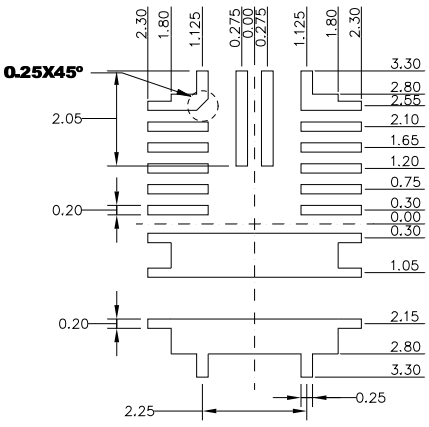
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

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