MPQ18021HN-A



100V, 2.5A, High-Frequency, Half-Bridge Gate Driver AEC-Q100 Qualified

DESCRIPTION

The MPQ18021HN-A is a high-frequency, 100V, half-bridge, N-channel power MOSFET driver. Its low-side and high-side driver channels are controlled independently and matched with a time delay of less than 5ns. Under-voltage lockout (UVLO) on both the high-side and lowside supplies force their outputs low in the case of an insufficient supply. The integrated bootstrap diode reduces the external component count.

The MPQ18021HN-A is available in a costeffective SOIC-8E package.

FEATURES

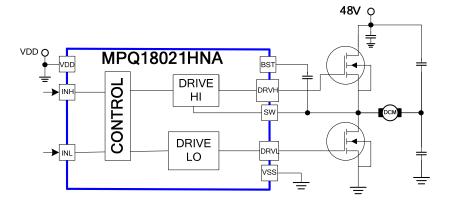
- Guaranteed Industrial Automotive **Temperature Range Limits**
- Drives N-Channel MOSFET Half-Bridge
- 100V V_{BST} Voltage Range
- On-Chip Bootstrap Diode
- Typical 16ns Propagation Delay Time
- Less than 5ns Gate Drive Matching
- Drives 1nf Load with 12ns/9ns Rise/Fall Times with 12V VDD
- TTL-Compatible Input
- Less than 160µA Quiescent Current
- UVLO for both High-Side and Low-Side
- Available in a SOIC-8E Package
- Available in AEC-Q100 Qualified Grade 1

APPLICATIONS

- Car DC/DC Power Systems
- Half Bridge Motor Drivers

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TYPICAL APPLICATION





ORDERING INFORMATION

Part Number	Package	Top Marking
MPQ18021HN-A-AEC1	SOIC-8E	See Below

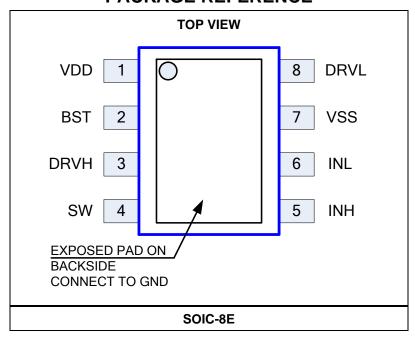
^{*} For Tape & Reel, add suffix –Z (e.g. MPQ18021HN-A-AEC1–Z).

TOP MARKING

MP18021A LLLLLLLL MPSYWW

MP18021A: Part number LLLLLLL: Lot number MPS: MPS prefix Y: Year code WW: Week code

PACKAGE REFERENCE





PIN FUNCTIONS

Pin#	Name	Description		
1	VDD	Supply input. VDD supplies power to all of the internal circuitries. Place a decoupling capacitor to ground close to VDD to ensure a stable and clean supply.		
2	BST	Bootstrap. BST is the positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between BST and SW.		
3	DRVH	Floating high-side driver output.		
4	SW	Switching node.		
5	INH	Control signal input for the floating driver.		
6	INL	Control signal input for the low-side driver.		
7	VSS	Chin ground Connect the expected and to VSS for proper thermal energies		
Exposed Pad		Chip ground. Connect the exposed pad to VSS for proper thermal operation.		
8	DRVL	Low-side driver output.		

ADSOLUTE MAXIM	
Supply voltage (V _{DD})	0.3V to +18V
SW voltage (V _{HS})	5.0V to +110V
BST voltage (V _{HB})	0.3V to +110V
BST to SW	0.3V to +18V
DRVH to SW0.3\	√ to (BST - SW) + 0.3V
DRVL to VSS	0.3V to (VDD + 0.3V)
All other pins	0.3V to $(V_{DD} + 0.3V)$
CDM rating (AEC-Q100-0	
All pins	Class C6
HBM rating (AEC-Q100-0	002)
BST, DRVH	Class H1B
SW	Class H1C
Other pins	Class H2
Continuous power dissipa	ation (T ₄ = 25°C) (2)

ARSOLUTE MAXIMUM RATINGS (1)

Recommended Operating Conditions (3)					
Supply voltage (V _{DD})	9.0V to 16V				
SW voltage (V _{HS})	1.0V to +100V - VDD				
SW slew rate	<50V/ns				
Operation junction temp.	(T _J)40°C to +125°C				

Junction temperature 150°C Lead temperature.......260°C Storage temperature-65°C to +150°C

Thermal Resistance (4)	$oldsymbol{ heta}_{JA}$	$\boldsymbol{\theta}_{JC}$	
SOIC-8E	50	12	.°C/W

NOTES:

- 1) Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-toambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX) T_A$)/ θ_{JA} . Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.



ELECTRICAL CHARACTERISTICS

 $V_{DD}=V_{BST}$ - $V_{SW}=12V$, $V_{SS}=V_{SW}=0V$, no load at DRVH and DRVL, $T_J=-40^{\circ}C$ to +125°C, typical values tested at $T_J=+25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Тур	Max	Units
Supply Currents						
VDD quiescent current	I_{DDQ}	INH = INL= 0		120	160	μA
VDD operating current	I _{DDO}	f _{sw} = 500kHz		2.8	3.5	mA
Floating driver quiescent current	I _{BSTQ}	INH = INL = 0		70	100	μA
Floating driver operating current	I _{BSTO}	f _{sw} = 500kHz		2.1	3	mA
Leakage current	ILK	HB = SW = 100V		0.05	2.5	μΑ
Inputs	ILN			0.00	2.0	μΛ
INL/INH high				2.2	2.6	V
INL/INH low			1	1.5	2.0	V
INL/INH internal pull-down			•			
resistance	R _{IN}			185		kΩ
Under-Voltage Protection (UVF	P)		<u> </u>			ı
VDD rising threshold	V_{DDR}		7.4	8.1	8.9	V
VDD hysteresis	V _{DDH}			0.5		V
(BST-SW) rising threshold	V _{BSTR}		6.5	7.1	7.7	V
(BST-SW) hysteresis	V _{BSTH}			0.55		V
Bootstrap Diode		1	l		I	
Bootstrap diode VF @ 100μA	V _{F1}			0.5		V
Bootstrap diode VF @ 100mA	V _{F2}			1		V
Bootstrap diode dynamic R	R _D	@ 100mA		2.5		Ω
Low Side Gate Driver		19	I.	I.	l	
Low-level output voltage	Voll	I _O = 100mA		0.15	0.32	V
High-level output voltage to rail	Vohl	I _O = -100mA		0.45	1	V
		V _{LO} = 0V, V _{DD} = 12V		1.5		Α
Peak pull-up current (5)	Іонь	V _{LO} = 0V, V _{DD} = 16V		2.5		Α
D 1 1 1 1 1 1 1 1 1	loll	V _{LO} = V _{DD} = 12V		2.5		Α
Peak pull-down current (5)		$V_{LO} = V_{DD} = 16V$		3.5		Α
Floating Gate Driver			1	•		•
Low-level output voltage	V_{OLH}	I _O = 100mA		0.15	0.32	V
High-level output voltage to rail	Vонн	I _O = -100mA		0.45	1	V
Dock pull up ourrent (5)	Іонн	V _{HO} = 0V, V _{DD} = 12V		1.5		Α
Peak pull-up current (5)		V _{HO} = 0V, V _{DD} = 16V		2.5		Α
Peak pull-down current (5)	Іогн	V _{HO} = V _{DD} = 12V		2.5		Α
Peak pull-down current		$V_{HO} = V_{DD} = 16V$		3.5		Α
Switching spec – low-side gate driver						
Turn-off propagation delay INL falling to DRVL falling	T _{DLFF}			16		ns
Turn-on propagation delay INL rising to DRVL rising	T _{DLRR}			16		
DRVL rise time		C _L = 1nF		12		ns
DRVL fall time		C _L = 1nF		9		ns



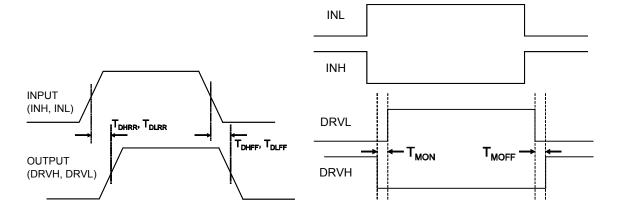
ELECTRICAL CHARACTERISTICS (continued) $V_{DD} = V_{BST} - V_{SW} = 12V, \ V_{SS} = V_{SW} = 0V, \ no \ load \ at \ DRVH \ and \ DRVL, \ T_J = -40^{\circ}C \ to \ +125^{\circ}C, \ typical \ values tested \ at \ T_J = +25^{\circ}C, \ unless \ otherwise \ noted.$

Parameter	Symbol	Condition	Min	Тур	Max	Units
Switching Spec - Floating Gate	e Driver					
Turn-off propagation delay INL falling to DRVH falling	T_{DHFF}			16		ns
Turn-on propagation delay INL rising to DRVH rising	T _{DHRR}			16		ns
DRVH rise time		C _L = 1nF		12		ns
DRVH fall time		C _L = 1nF		9		ns
Switching Spec – Matching						
Floating driver turn-off to low- side drive turn-on (5)	T _{MON}			1	5	ns
Low-side driver turn-off to floating driver turn-on (5)	T _{MOFF}			1	5	ns
Minimum input pulse width that changes the output	T _{PW}				50 ⁽⁵⁾	ns
Bootstrap diode turn-on or turn-off time	T _{BS}			10 ⁽⁵⁾		ns
Thermal shutdown (5)				170		°C
Thermal shutdown hysteresis (5)				25		°C

NOTE:

5) Guaranteed by design.

TIMING DIAGRAM

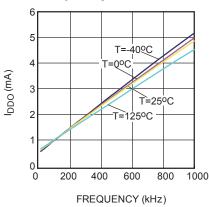




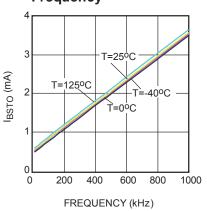
TYPICAL PERFORMANCE CHARACTERISTICS

 V_{DD} = 12V, V_{SS} = V_{SW} = 0V, T_A = 25°C, unless otherwise noted.

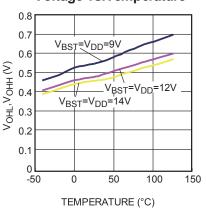
IDDO Operation Current vs. Frequency



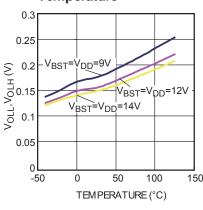
IBSTO Operation Current vs. Frequency



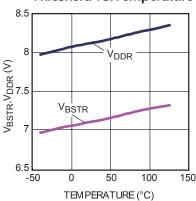
High-Level Output Voltage vs.Temperature



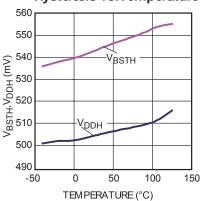
Low-Level Output Voltage vs. **Temperature**



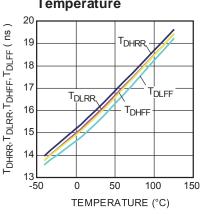
Under-Voltage Lockout Threshold vs. Temperature



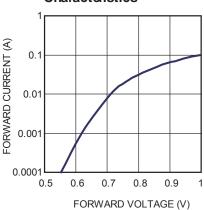
Under-Voltage Lockout Hysteresis vs. Temperature



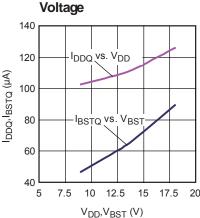
Propagation Delay vs. **Temperature**



Bootstrap Diode I-V Characteristics



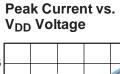
Quiescent Current vs.

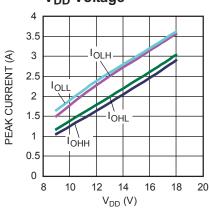




TYPICAL PERFORMANCE CHARACTERISTICS (continued)

 V_{DD} = 12V, V_{SS} = V_{SW} = 0V, T_A = 25°C, unless otherwise noted.

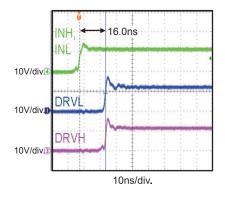


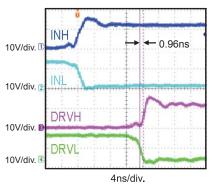


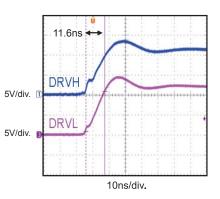
Turn-On Propagation Delay

Gate Drive Matching TMOFF

Drive Rise Time (1nF Load)



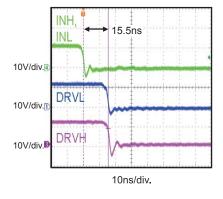


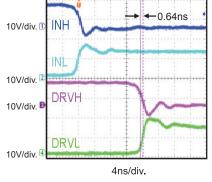


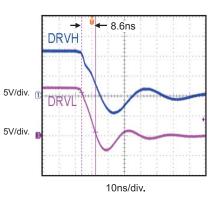
Turn-Off Propagation Delay

Gate Drive Matching TMON

Drive Fall Time (1nF Load)









BLOCK DIAGRAM

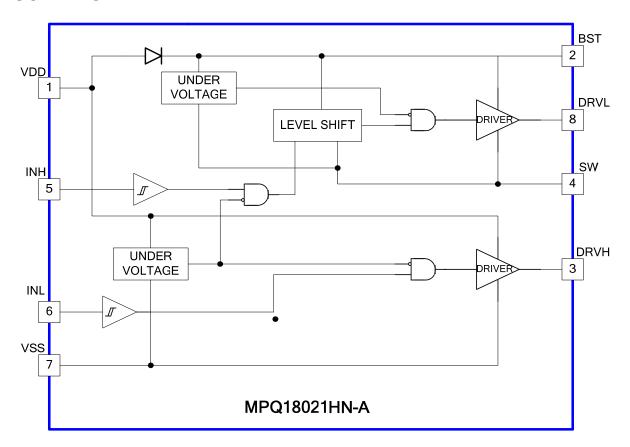


Figure 1: Functional Block Diagram



APPLICATION

The input signals of INH and INL can be controlled independently. If both INH and INL are controlling the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) of the same bridge, shoot through can be prevented by setting a sufficient dead time between INH and INL low, and vice versa (see Figure 2). Dead time is defined as the time interval between INH low and INL low.

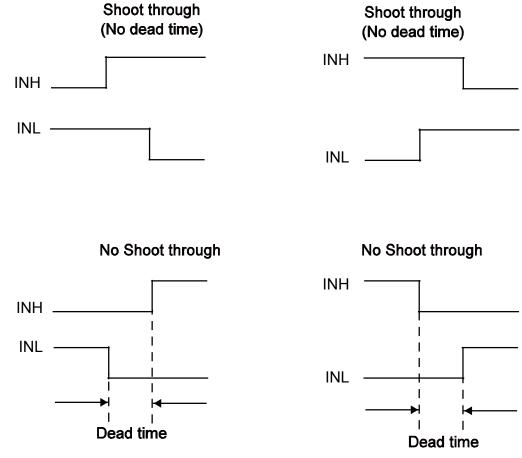


Figure 2: Shoot-Through Timing Diagram



REFERENCE DESIGN CIRCUITS

Half-Bridge Converter

In the half-bridge converter topology, the MOSFETs are driven alternately with some dead time. Therefore, INH and INL are driven

with alternating signals from the pulse-width modulation (PWM) controller. The input voltage can rise as high as 100V in this application (see Figure 3 through Figure 5).

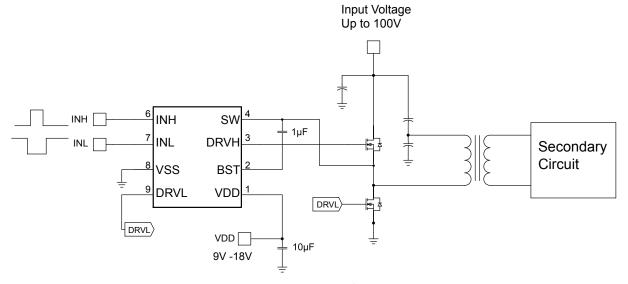


Figure 3: Half-Bridge Converter

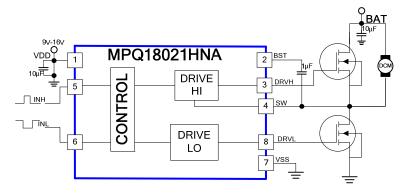


Figure 4: Half-Bridge for Unidirectional Motor

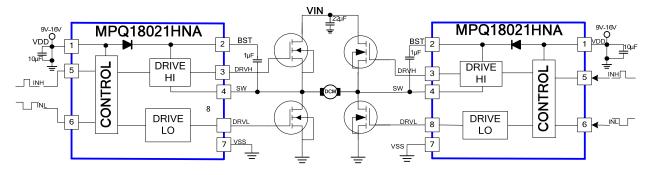


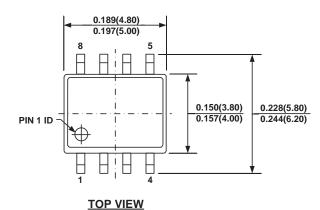
Figure 5: 2x MPQ18024 for One Bidirectional DC Motor

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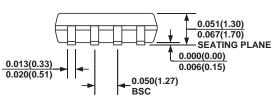
PACKAGE INFORMATION

SOIC-8E

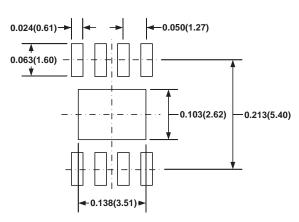


0.124(3.15) 0.136(3.45) 0.089(2.26) 0.101(2.56) Н

BOTTOM VIEW

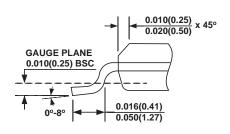


FRONT VIEW



RECOMMENDED LAND PATTERN

SEE DETAIL "A" 0.0075(0.19) 0.0098(0.25) **SIDE VIEW**



DETAIL "A"

NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN **BRACKET IS IN MILLIMETERS.**
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.

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