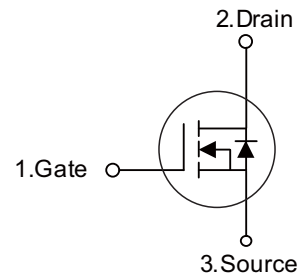


PRODUCT CHARACTERISTICS

VDSS	650V
$R_{DS(on)Typ}(V_{GS}=10V)$	0.54Ω
Qg@type	13.8nC
ID	7.3A

Symbol

APPLICATIONS

- * Power factor correction
- * Switched mode power supplies
- * Uninterruptible power supply

FEATURES

- * low $R_{DS(on)}$
- * low gate charge
- * RoHS compliant


ORDER INFORMATION

Order codes		Package	Packing
Halogen-Free	Halogen		
N/A	MOT65R600F	TO-220F	50 pieces/Tube

ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain – Source voltage	V_{DSS}	650	V
Gate – Source voltage	V_{GSS}	±30	V
Continuous drain current	I_D	7.3	A
Pulsed drain current ⁽¹⁾	I_{DM}	21.9	A
Power dissipation	P_D	25	W
Single - pulse avalanche energy	E_{AS}	142	mJ
MOSFET dv/dt ruggedness	dv/dt	50	V/ns
Diode dv/dt ruggedness ⁽²⁾	dv/dt	15	V/ns
Storage temperature	T_{stg}	-55 ~150	°C
Maximum operating junction temperature	T_j	150	°C

 1) Pulse width t_P limited by $T_{j,max}$

 2) $I_{SD} \leq I_D, V_{DS\ peak} \leq V_{(BR)DSS}$
THERMAL CHARACTERISTICS

Parameter	Symbol	Rating	Unit
Thermal resistance, junction-case max	R_{thjc}	5	°C/W
Thermal resistance, junction-ambient max	R_{thja}	75	°C/W

■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Drain – Source Breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	650	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	3	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650V, V_{GS} = 0V$	-	-	1	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 30V, V_{DS} = 0V$	-	-	100	nA
Drain-Source On State Resistance	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 2.1A$	-	0.54	0.60	Ω
Input Capacitance	C_{iss}	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0MHz$	-	545	-	pF
Output Capacitance	C_{oss}		-	640	-	
Reverse Transfer Capacitance	C_{rss}		-	28.6	-	
Turn On Delay Time	$t_{d(on)}$	$V_{GS} = 10V, R_G = 25\Omega,$ $V_{DS} = 325V, I_D = 7.3A$	-	18	-	ns
Rise Time	t_r		-	33	-	
Turn Off Delay Time	$t_{d(off)}$		-	80	-	
Fall Time	t_f		-	28	-	
Total Gate Charge	Q_g	$V_{GS} = 10V, V_{DS} = 520V,$ $I_D = 7.3A$	-	13.8	-	nC
Gate – Source Charge	Q_{gs}		-	3.6	-	
Gate – Drain Charge	Q_{gd}		-	5.6	-	
Gate Resistance	R_G	$V_{GS} = 0V, f = 1.0MHz$	-	20	-	Ω
Continuous Diode Forward Current	I_{SD}		-	-	7.3	A
Diode Forward Voltage	V_{SD}	$I_{SD} = 7.3A, V_{GS} = 0V$	-	-	1.4	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 7.3A$ $di/dt = 100A/\mu s$ $V_{DD} = 100V$	-	272	-	ns
Reverse Recovery Charge	Q_{rr}		-	3	-	μC
Reverse Recovery Current	I_{rrm}		-	22.2	-	A

■ ELECTRICAL CHARACTERISTICS DIAGRAMS

Fig.1 On-Region characteristics,

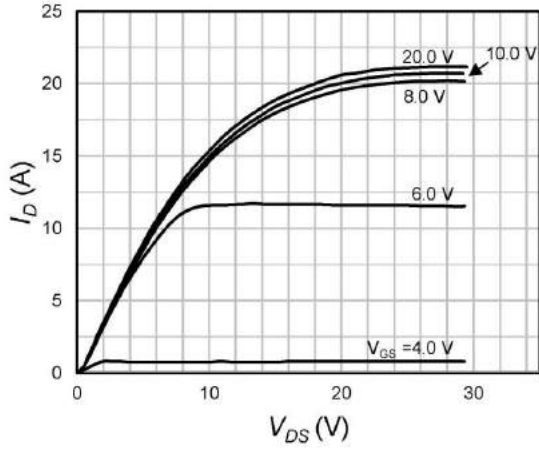


Fig.3 On-Resistance Variation with temperature (Normalized)

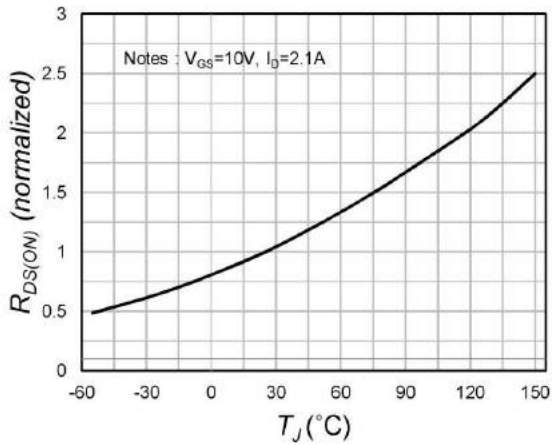


Fig.5 Transfer Characteristics

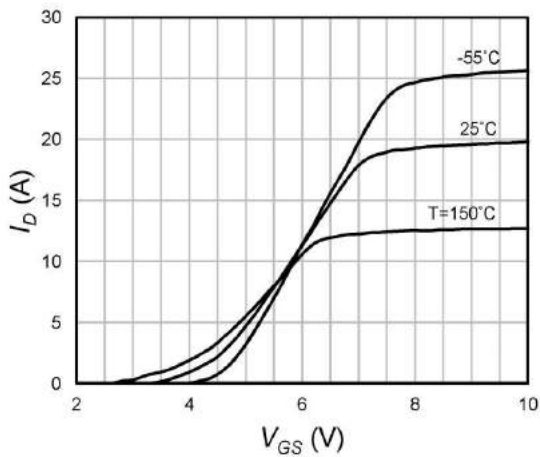


Fig.2 On-resistance Variation with Drain Current and Gate Voltage

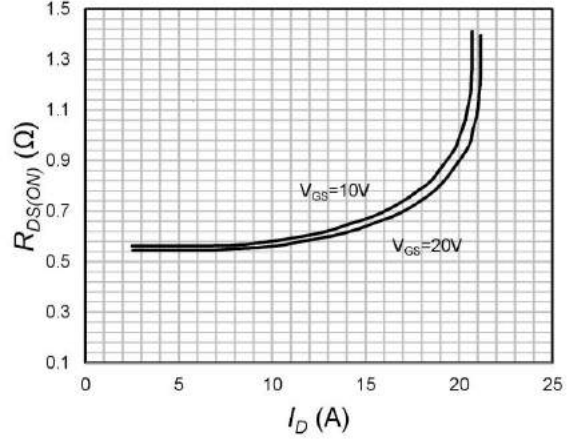


Fig.4 Breakdown Voltage Variation vs. Temperature (Normalized)

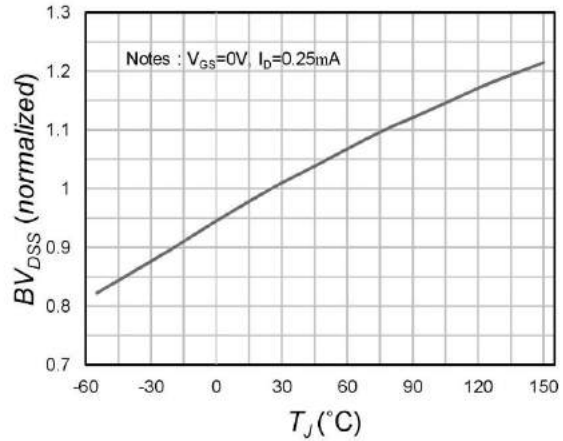
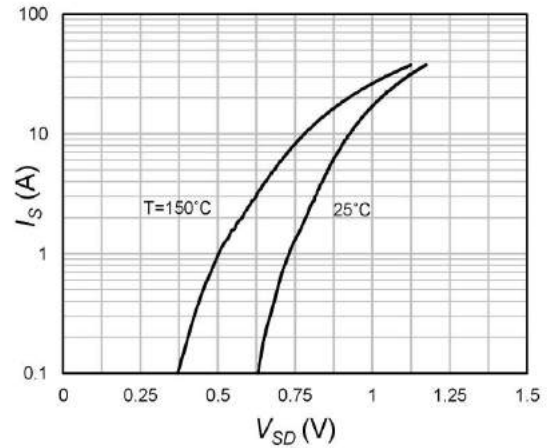


Fig.6 Body Diode Forward Voltage Variation with Source Current and Temperature



■ ELECTRICAL CHARACTERISTICS DIAGRAMS(Cont.)

Fig.7 Gate charge Characteristics

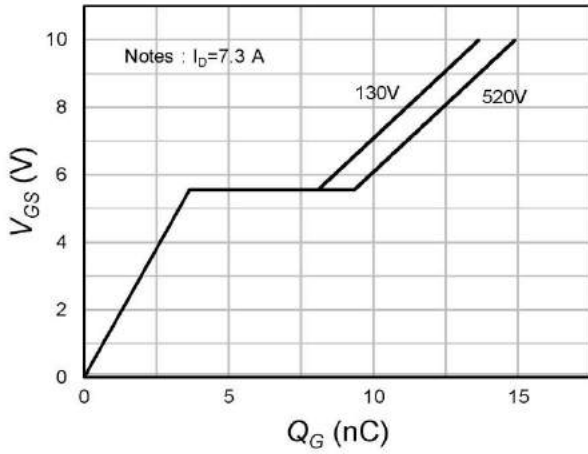


Fig.8 Capacitance Characteristics

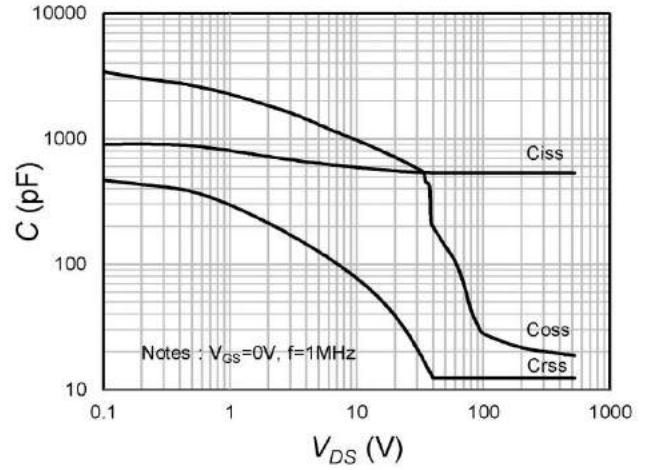


Fig.9 $V_{GS(th)}$ Variation with Temperature (Normalized)

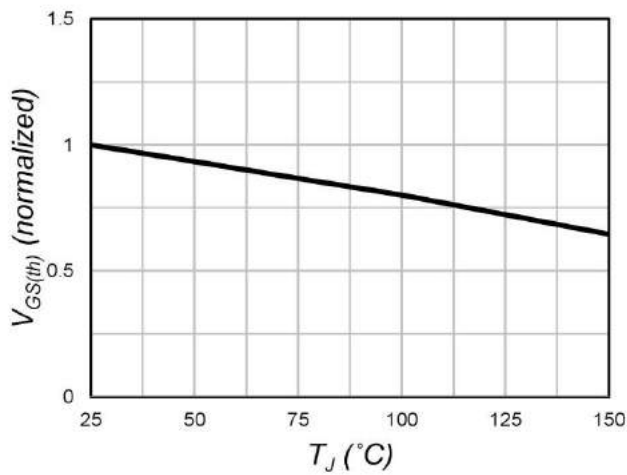


Fig.10 Maximum Drain Current vs. Case Temperature

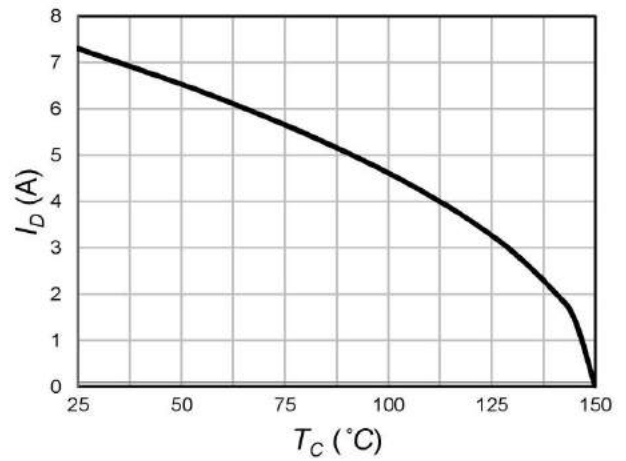


Fig. 11 Single Pulse Maximum Power Dissipation

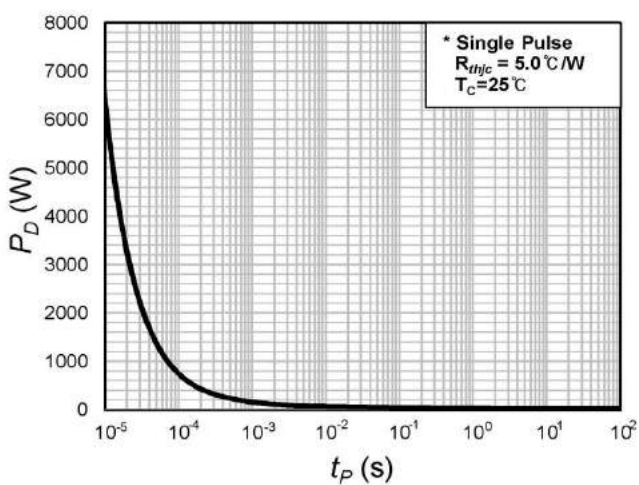
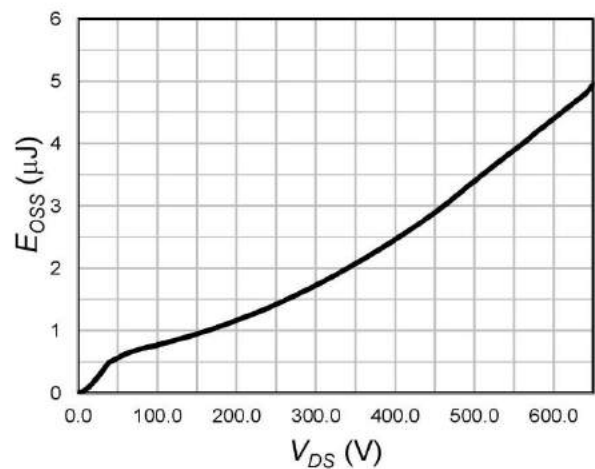


Fig. 12 Output Capacitance Stored Energy



■ ELECTRICAL CHARACTERISTICS DIAGRAMS(Cont.)

Fig.13 Transient Thermal Response Curve

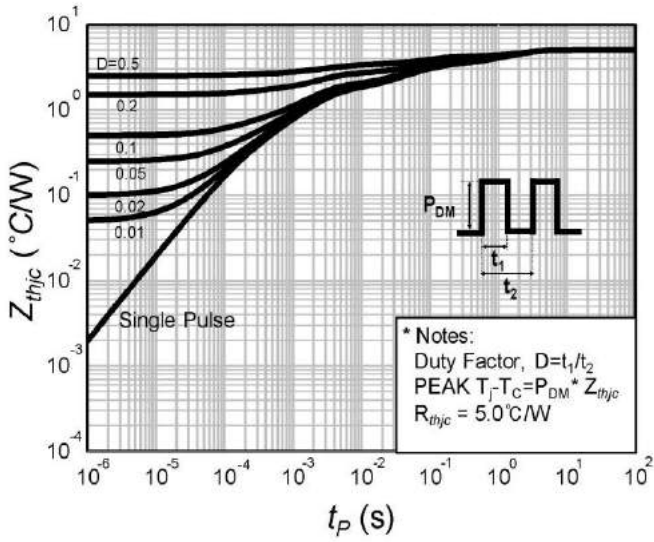
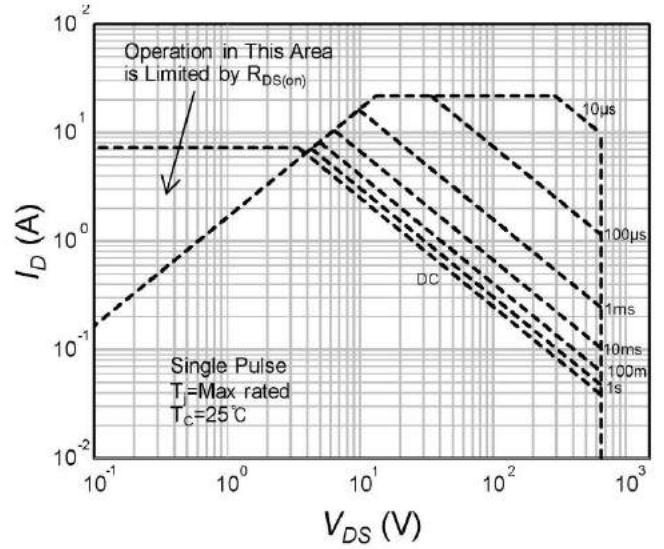


Fig. 14 Maximum Safe Operating Area



■ TEST CIRCUITS AND WAVEFORMS

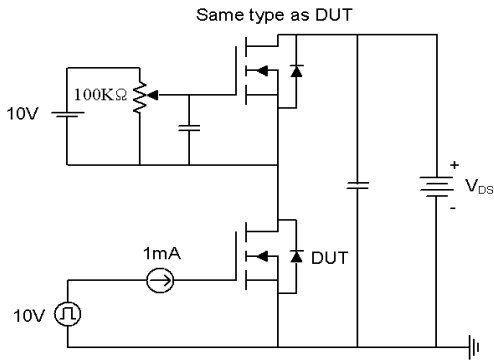


Fig15-1. Gate charge measurement circuit

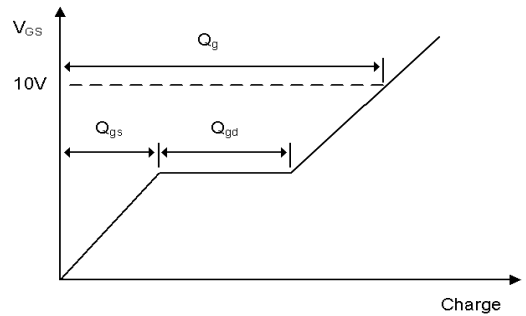


Fig15-2. Gate charge waveform

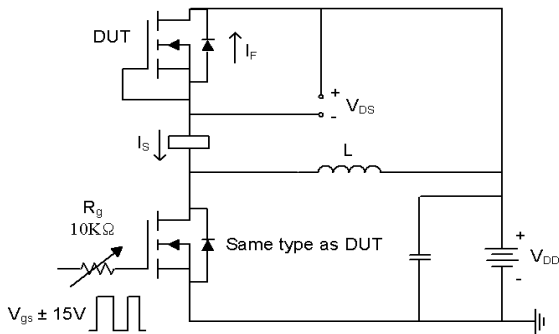


Fig16-1. Diode reverse recovery test circuit

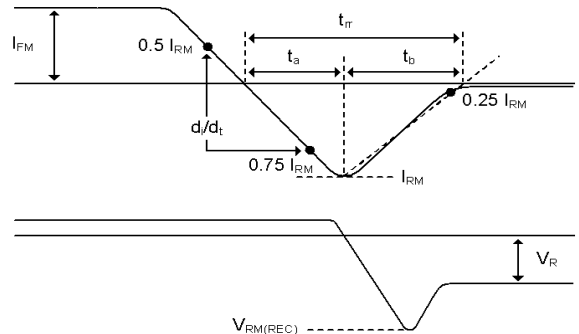


Fig16-2. Diode reverse recovery test waveform

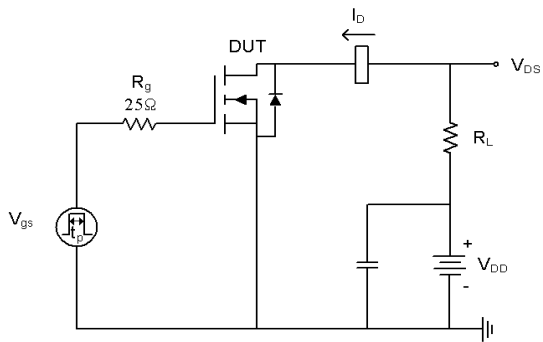


Fig17-1. Switching time test circuit for resistive load

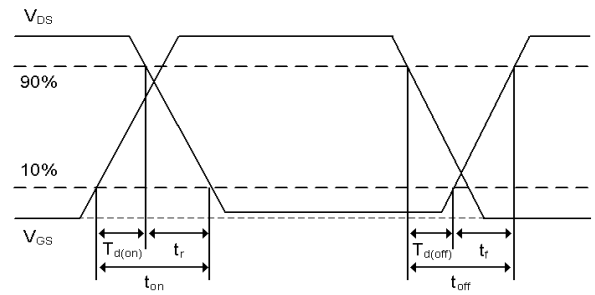


Fig17-2. Switching time waveform

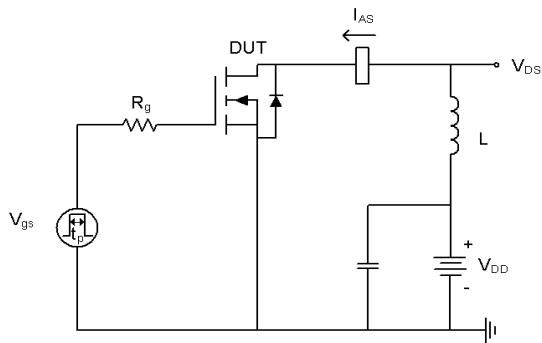


Fig18-1. Unclamped inductive load test circuit

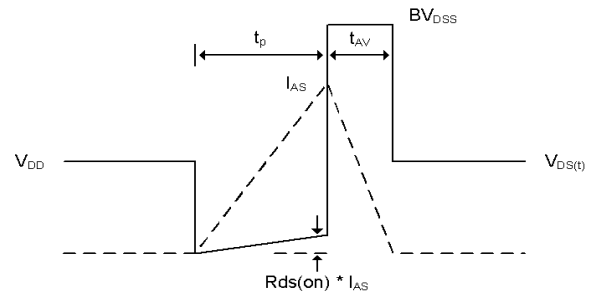
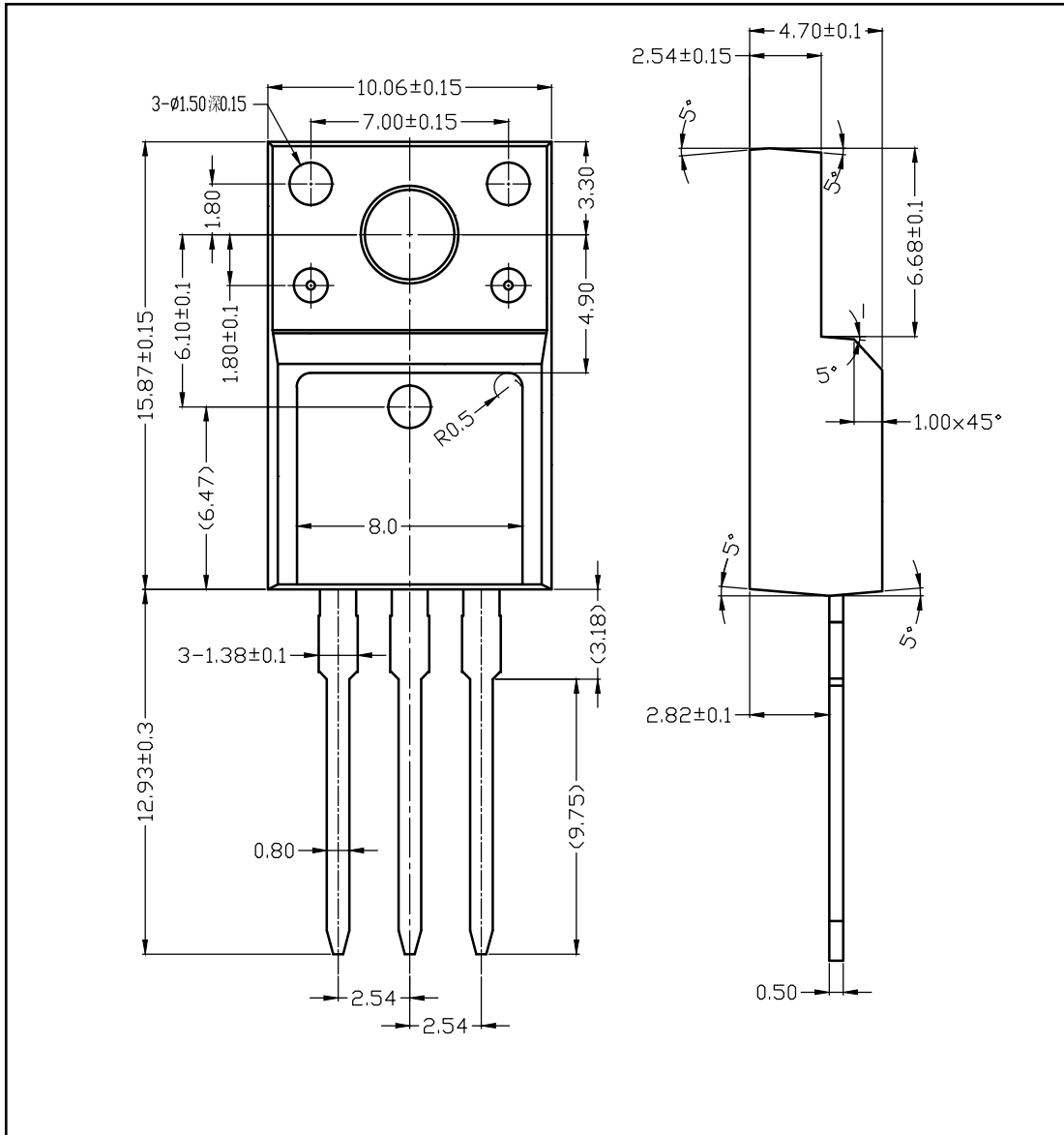


Fig18-2. Unclamped inductive waveform

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