

N-Channel 250-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME04N25 is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on state resistance. These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

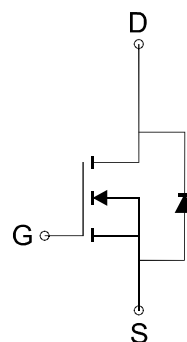
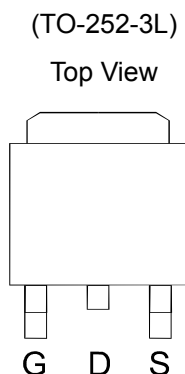
FEATURES

- $R_{DS(ON)} \leq 1.8 \Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 2.0 \Omega @ V_{GS}=5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION



N-Channel MOSFET

Ordering Information: ME04N25 (Pb-free)

ME04N25-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	250	V
Gate-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ C$	3.3
		$T_C=70^\circ C$	2.6
Pulsed Drain Current	I_{DM}	13	A
Maximum Power Dissipation	P_D	$T_C=25^\circ C$	31
		$T_C=70^\circ C$	20
Operating Junction Temperature	T_J	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Case *	$R_{\theta JC}$	4.0	$^\circ C/W$

* The device mounted on 1in² FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

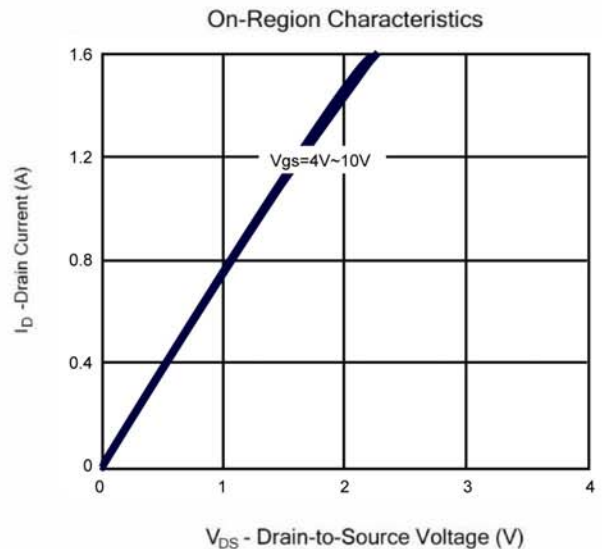
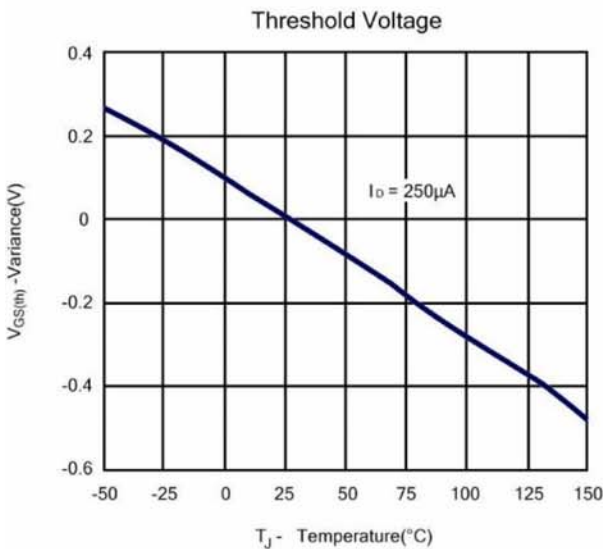
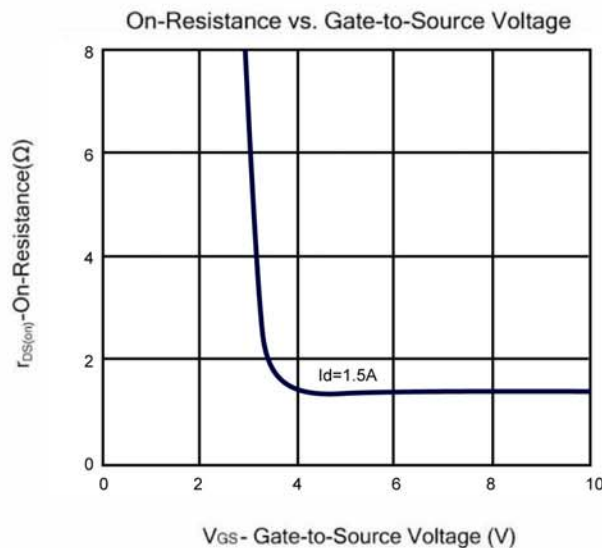
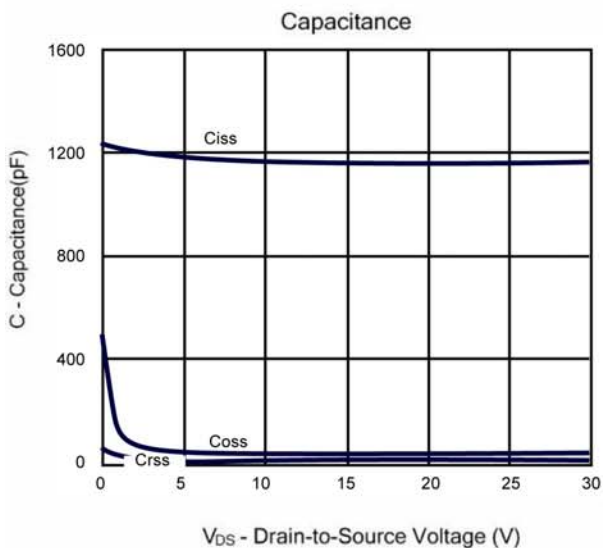
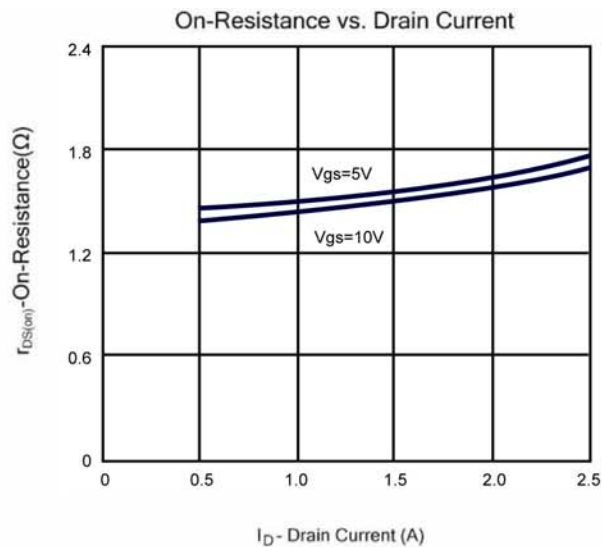
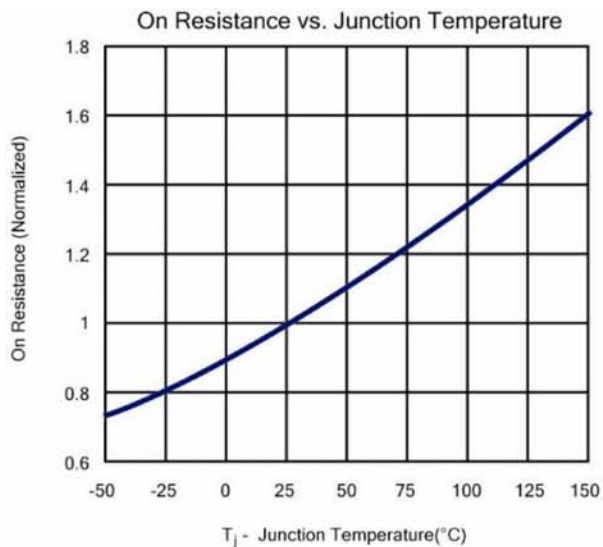
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	250			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1.5		3.5	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =250V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =10V, I _D = 1.5A		1.5	1.8	Ω
		V _{GS} =5V, I _D = 0.8A		1.55	2.0	
V _{SD}	Diode Forward Voltage	I _S =3A, V _{GS} =0V		0.86	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =200V, V _{GS} =10V, I _D =1.5A		30		nC
Q _g	Total Gate Charge	V _{DS} =200V, V _{GS} =4.5V, I _D =1.5A		17		
Q _{gs}	Gate-Source Charge			3		
Q _{gd}	Gate-Drain Charge			12		
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		1170		pF
C _{oss}	Output Capacitance			36		
C _{rss}	Reverse Transfer Capacitance			10		
t _{d(on)}	Turn-On Delay Time	V _{DS} =125V, R _L =125Ω, V _{GEN} =10V, R _G =6Ω		19		ns
t _r	Turn-On Rise Time			4		
t _{d(off)}	Turn-Off Delay Time			48		
t _f	Turn-Off Fall Time			13		

Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

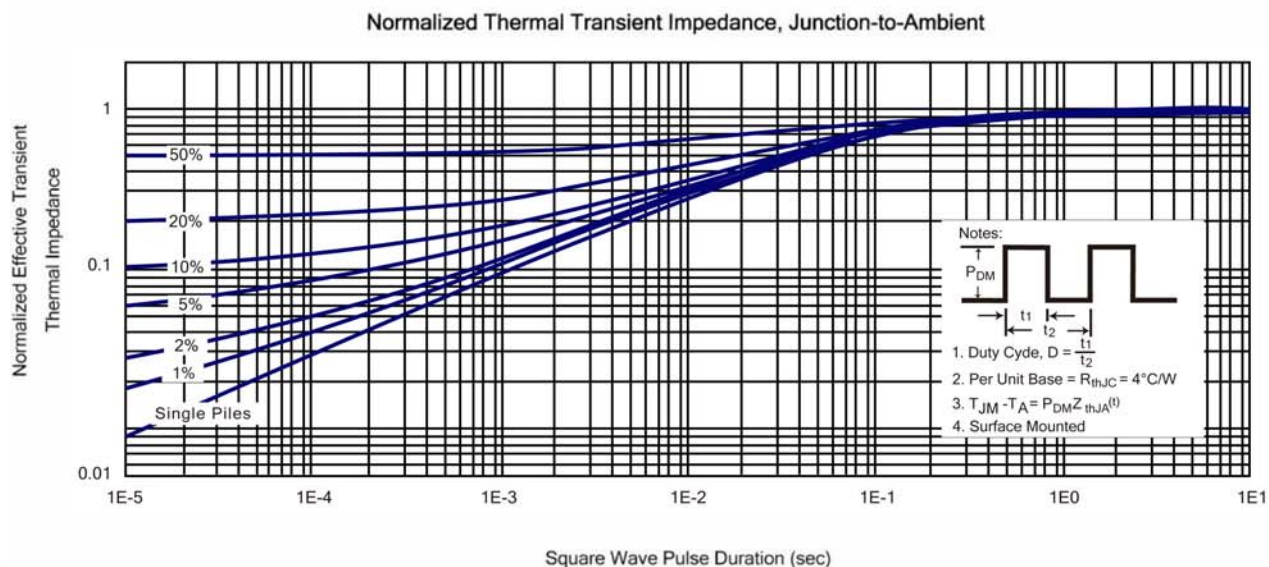
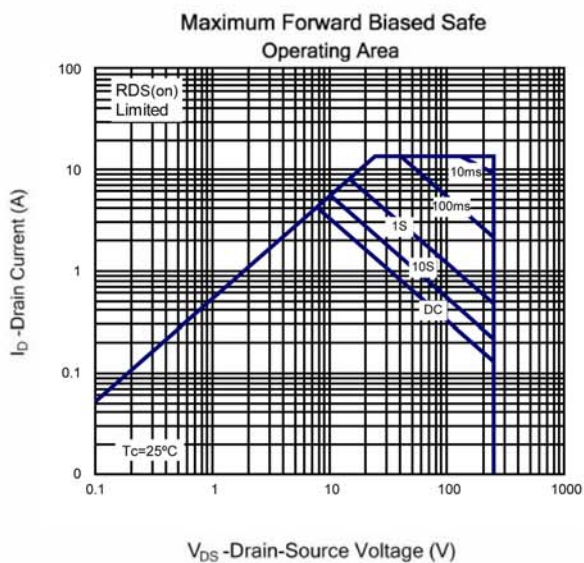
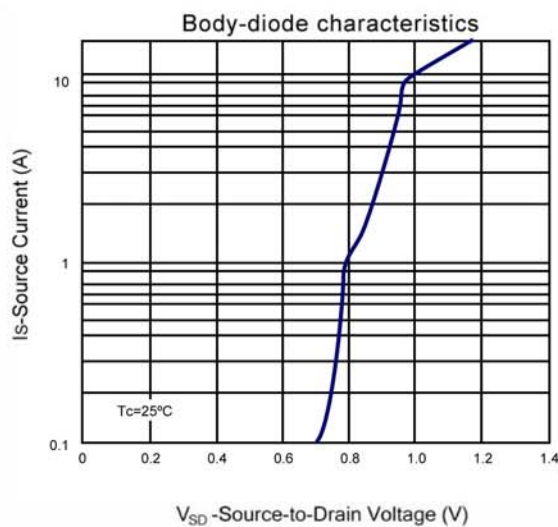
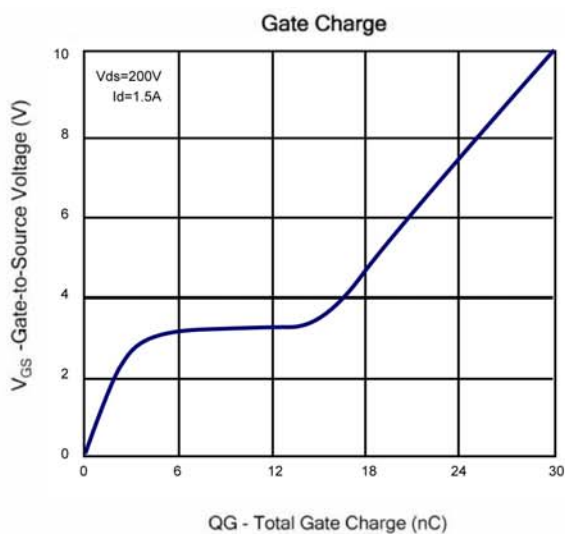
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Typical Characteristics (T_J = 25°C Noted)

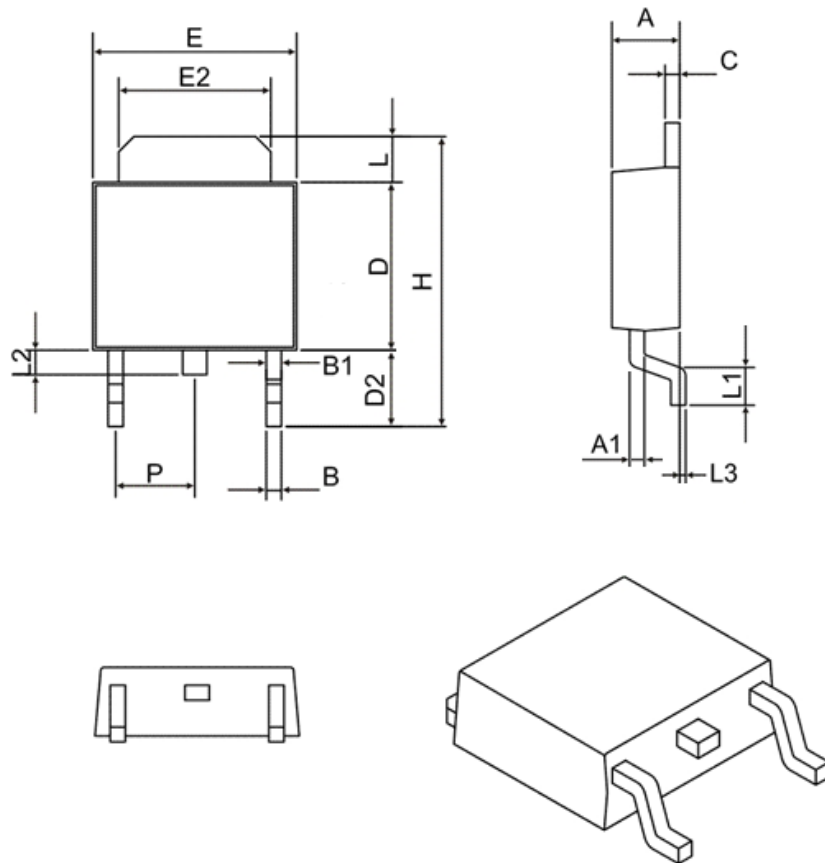


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Typical Characteristics (T_J = 25°C Noted)



TO252-3L Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	2.00	2.50
A1	0.45	0.60
B	0.50	0.88
B1	0.50	1.14
C	0.40	0.60
D	5.20	6.23
D2	2.743 REF	
H	9.40	10.50
E	6.30	6.80
E2	4.50	5.50
L	0.89	1.70
L1	0.90	1.77
L2	0.50	1.10
L3	0	0.30
P	2.286 BSC	

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