

N-Channel 100-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME120N10T is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on state resistance.

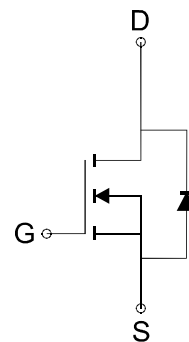
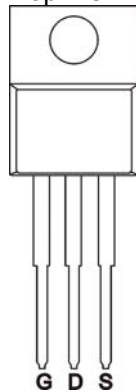
FEATURES

- $R_{DS(ON)} \leq 5.0m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

PIN CONFIGURATION

(TO-220)

Top View



N-Channel MOSFET

Ordering Information : ME120N10T(Pb-free)
ME120N10T-G(Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	100	V
Gate-Source Voltage	V_{GSS}	± 25	V
Continuous Drain Current*	I_D	$T_C=25^\circ C$	180
		$T_C=100^\circ C$	132
Pulsed Drain Current	I_{DM}	640	A
Maximum Power Dissipation	P_D	$T_C=25^\circ C$	250
		$T_C=100^\circ C$	125
Operating Junction Temperature	T_J	-55 to 175	$^\circ C$
Thermal Resistance-Junction to Case**	$R_{\theta JC}$	0.6	$^\circ C/W$

* Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 180A.

** The device mounted on 1in² FR4 board with 2 oz copper.

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Electrical Characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	100			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	2	3	4	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±25V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =10V, I _D =90A		5.0	6.5	mΩ
V _{SD}	Diode Forward Voltage	I _S =90A, V _{GS} =0V		0.8	1.0	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =80V, V _{GS} =10V, I _D =90A		180		nC
Q _{gs}	Gate-Source Charge			34		
Q _{gd}	Gate-Drain Charge			60		
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz		7889		pF
C _{oss}	Output Capacitance			1013		
C _{rss}	Reverse Transfer Capacitance			631		
R _g	Gate-Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		2.3		Ω
t _{d(on)}	Turn-On Delay Time	V _{DD} =50V, R _G =6Ω, V _{GS} =10V, I _{DS} =90A		28		ns
t _r	Turn-On Rise Time			45		
t _{d(off)}	Turn-Off Delay Time			85		
t _f	Turn-Off Fall Time			50		

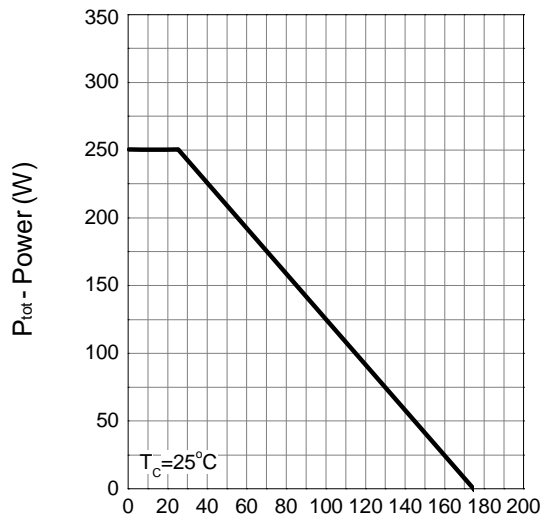
Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

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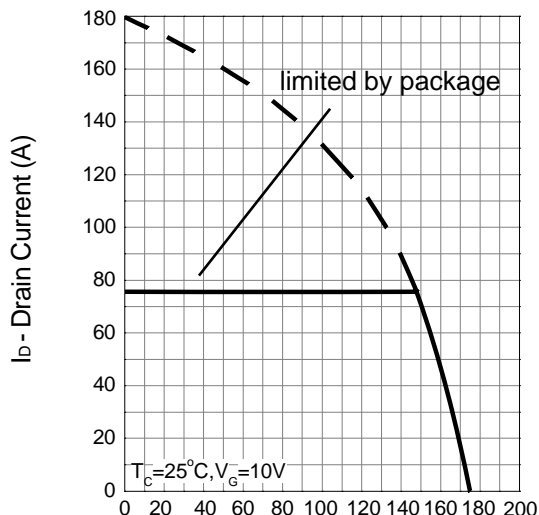
Typical Characteristics (T_J =25°C Noted)

Power Dissipation



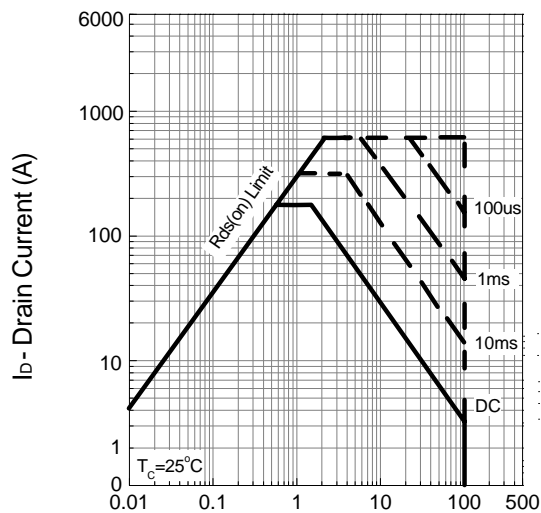
T_J- Junction Temperature (°C)

Drain Current



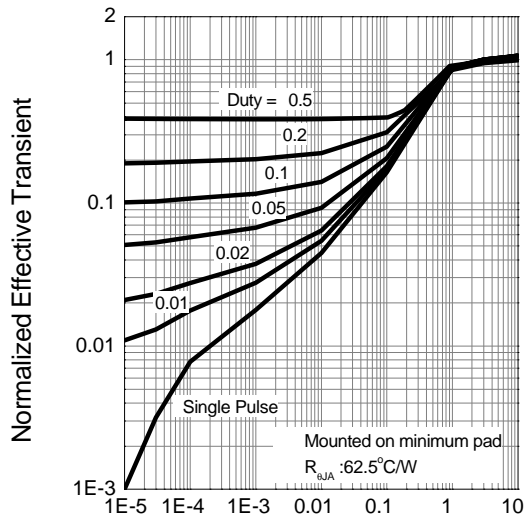
T_J- Junction Temperature (°C)

Safe Operation Area



V_{DS} - Drain - Source Voltage (V)

Thermal Transient Impedance

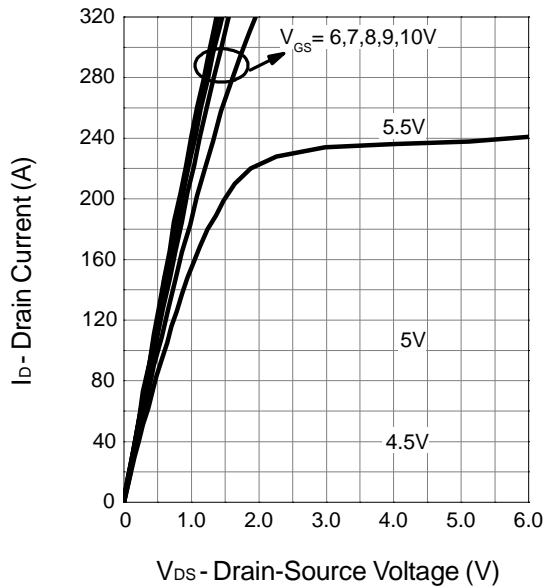


Square Wave Pulse Duration (sec)

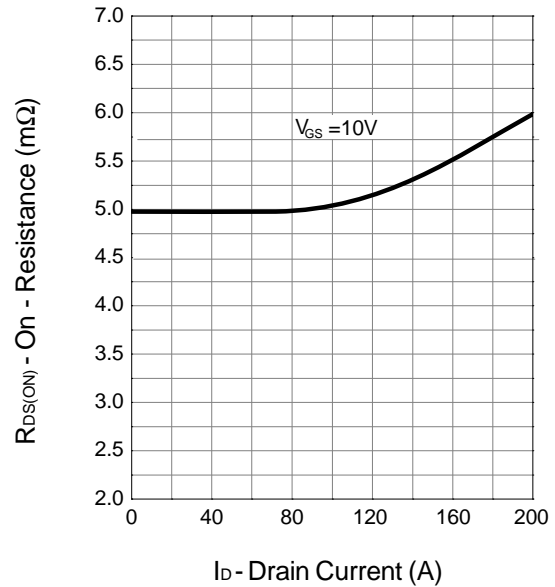
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Typical Characteristics (T_J =25°C Noted)

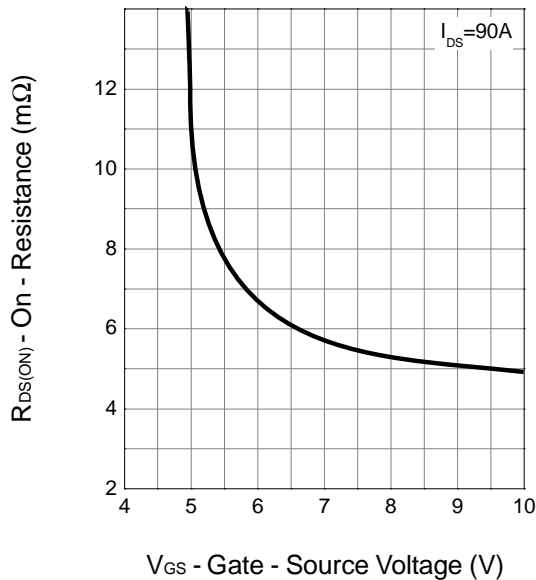
Output Characteristics



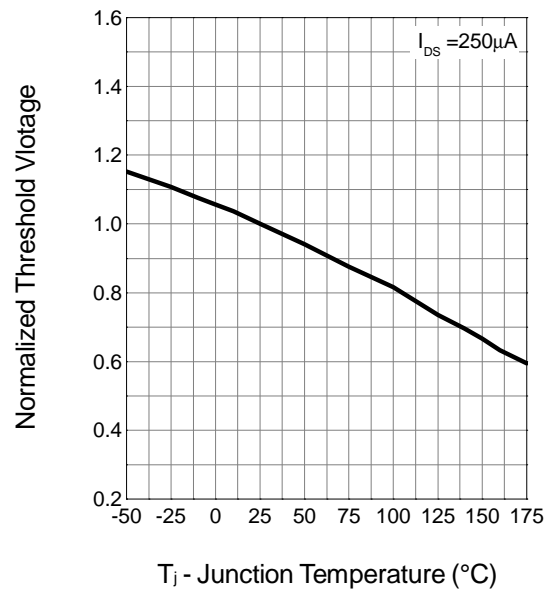
Drain-Source On Resistance



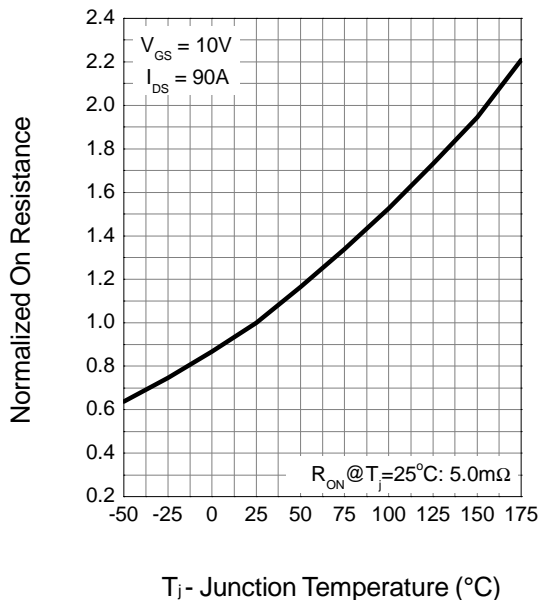
Drain-Source On Resistance



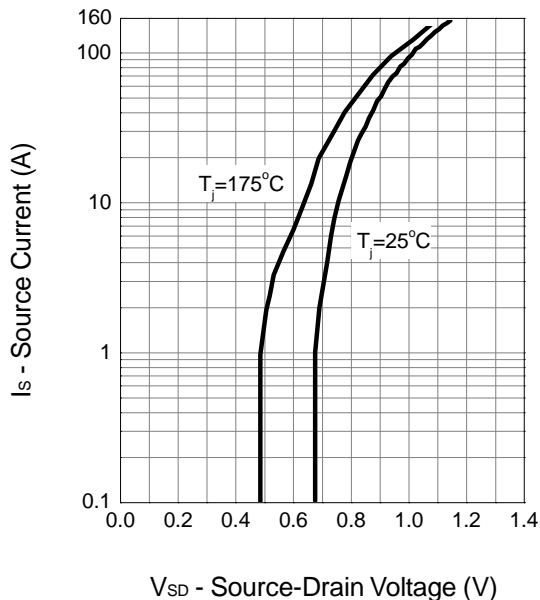
Gate Threshold Voltage



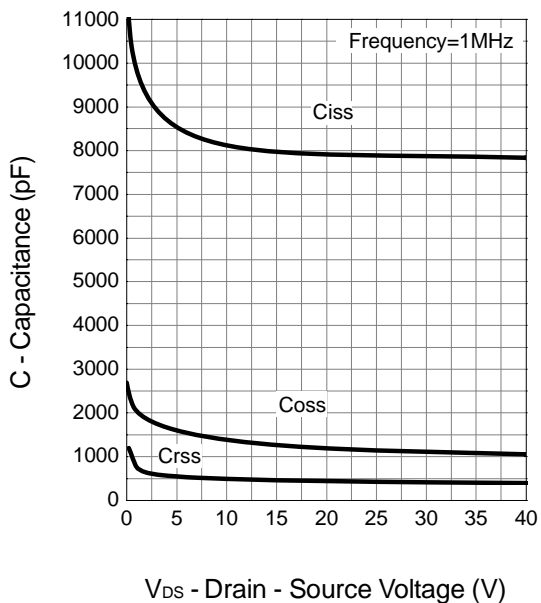
Drain-Source On Resistance



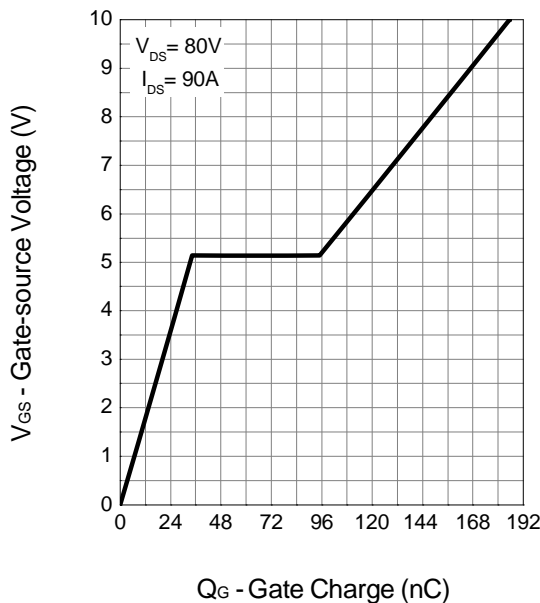
Source-Drain Diode Forward



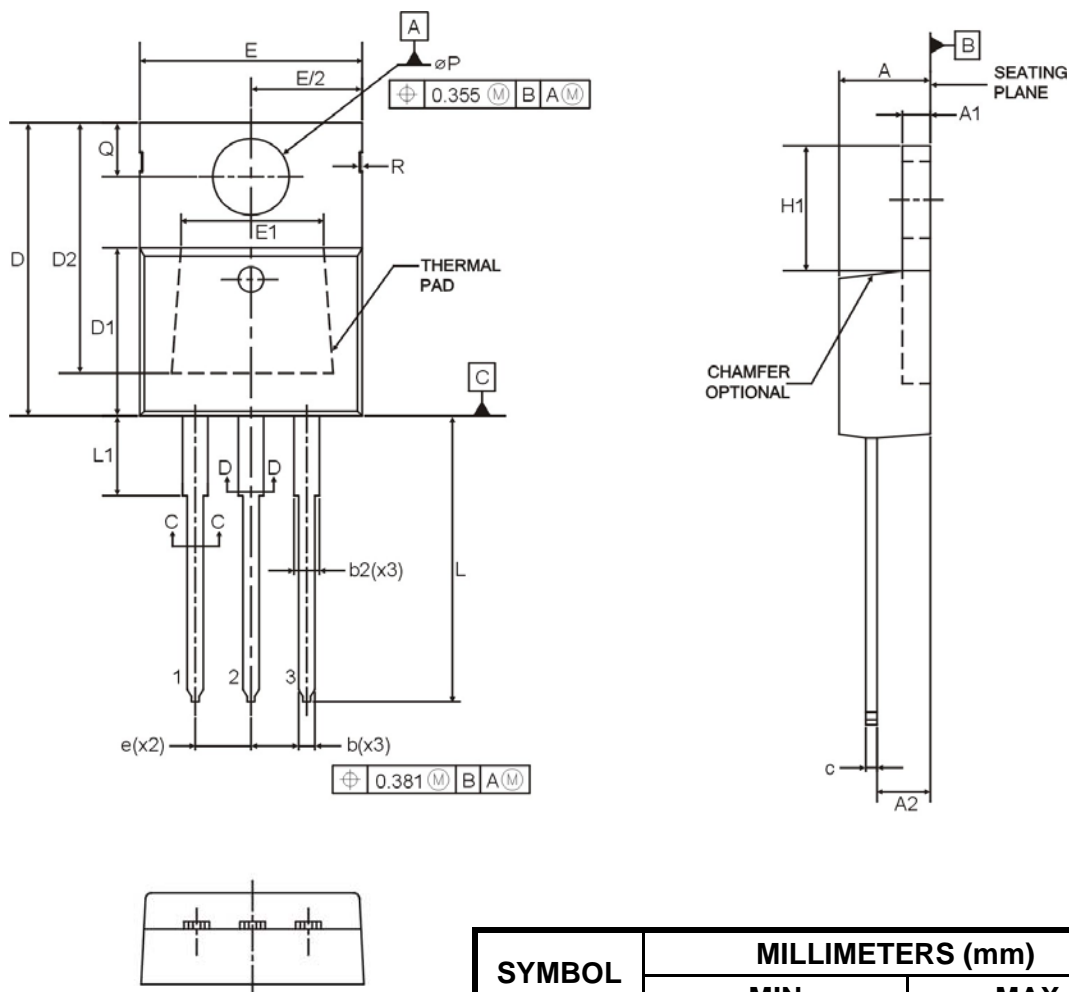
Capacitance



Gate Charge



TO-220 Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	3.500	4.90
A1	1.000	1.40
A2	2.000	3.00
b	0.500	1.00
c	0.350	0.65
D	14.00	16.50
D1	8.382	9.017
D2	12.00	13.00
E	9.600	10.70
E1	6.858	8.890
e	2.540 BSC	
H1	5.500	7.50
L	12.50	15.00
$\varnothing P$	3.810	3.860
Q	2.540	3.048
b2	1.100	1.80
L1	-	7.00

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