

N-Channel 60V (D-S) MOSFET

GENERAL DESCRIPTION

The ME2308S is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leq 100m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 130m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION



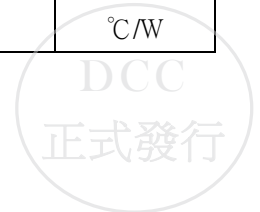
Ordering Information: ME2308S (Pb-free)

ME2308S-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current (Tj=150°C)*	I_D	TA=25°C	2.6
		TA=70°C	2.1
Pulsed Drain Current	I_{DM}	10	A
Maximum Power Dissipation*	P_D	TA=25°C	1.04
		TA=70°C	0.67
Operating Junction & Storage Temperature Range	T_J	-55 to 150	°C
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	110	°C/W

*The device mounted on 1in² FR4 board with 2 oz copper



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Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{DS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	60			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1.0		3.0	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =10V, I _D = 2.6A		82	100	mΩ
		V _{GS} =4.5V, I _D = 2.1A		96	130	
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.8	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =30V, V _{GS} =10V, I _D =2.6A		12		nC
Q _g	Total Gate Charge	V _{DS} =30V, V _{GS} =4.5V, I _D =2.6A		6.5		
Q _{gs}	Gate-Source Charge			2.2		
Q _{gd}	Gate-Drain Charge			2.7		
C _{iss}	Input capacitance	V _{DS} =30V, V _{GS} =0V, f=1.0MHz		350		pF
C _{oss}	Output Capacitance			40		
C _{rss}	Reverse Transfer Capacitance			12		
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		0.7		Ω
t _{d(on)}	Turn-On Delay Time	V _{DD} =20V, R _L =20Ω I _D =1A, V _{GEN} =10V R _G =1Ω		10		ns
t _r	Turn-On Rise Time			11		
t _{d(off)}	Turn-Off Delay Time			29		
t _f	Turn-Off Fall Time			3		

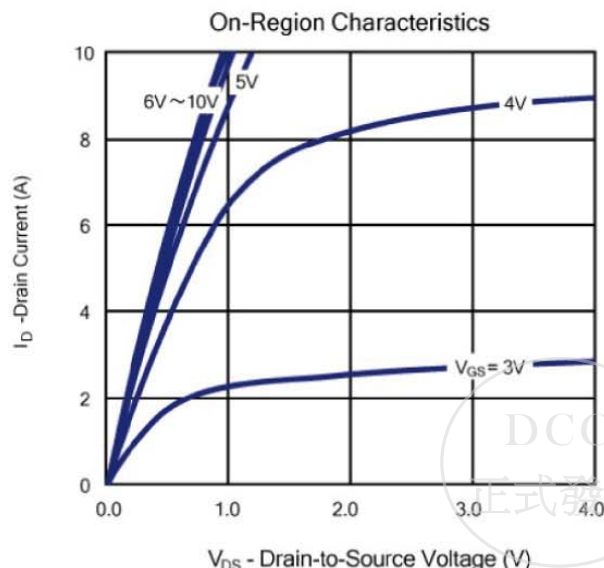
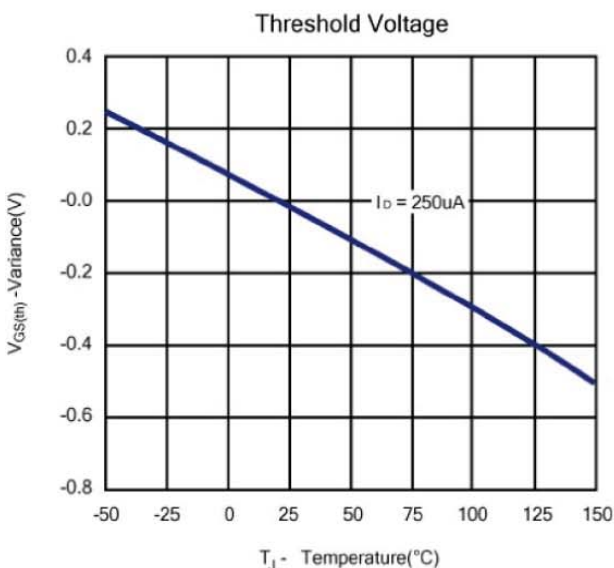
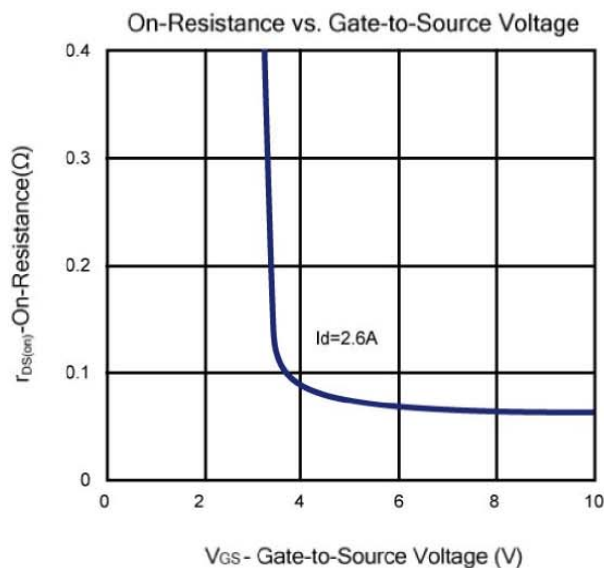
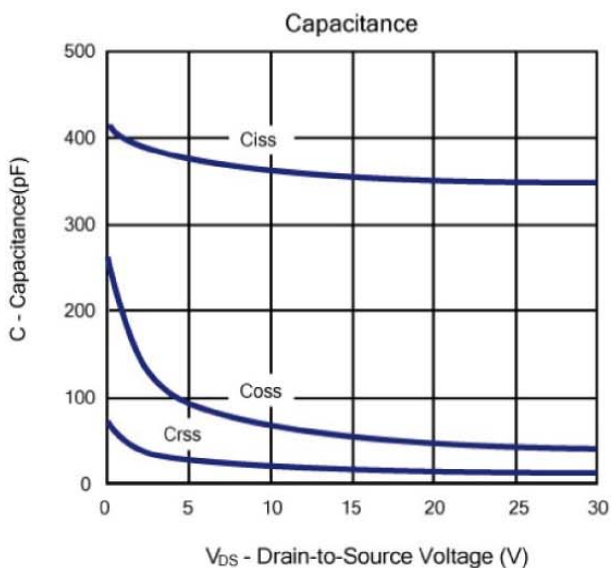
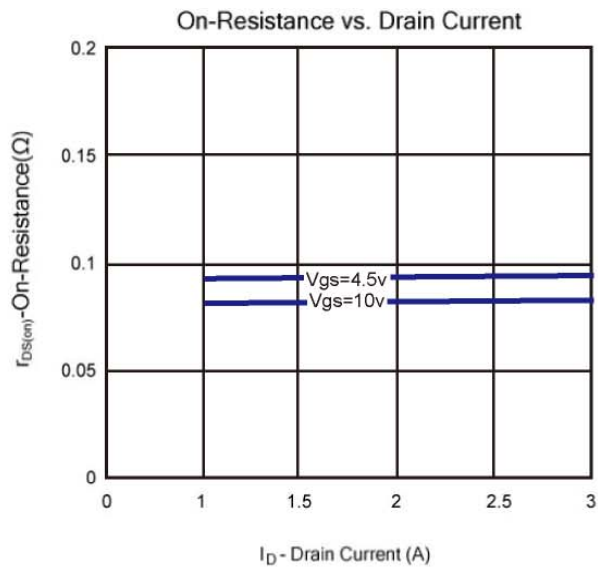
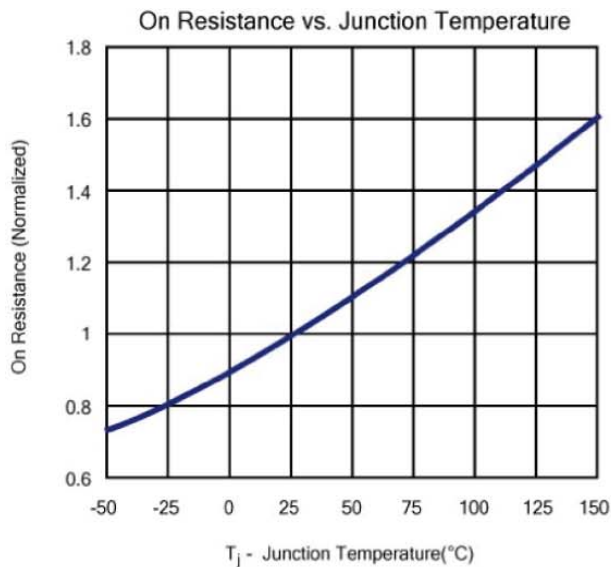
Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



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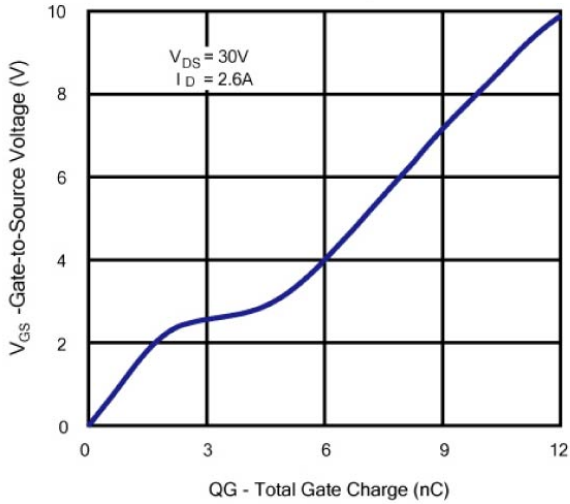
Typical Characteristics (T_J = 25°C Noted)



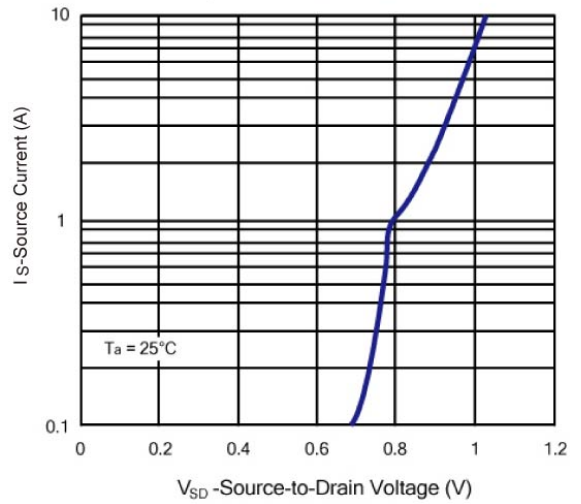
N-Channel 60V (D-S) MOSFET

Typical Characteristics (T_J = 25°C Noted)

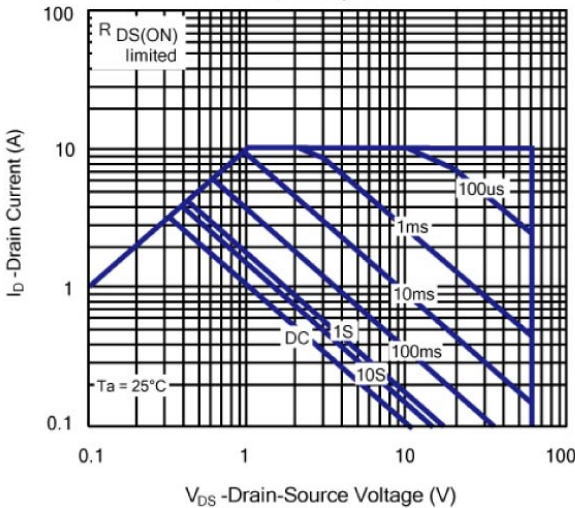
Gate Charge



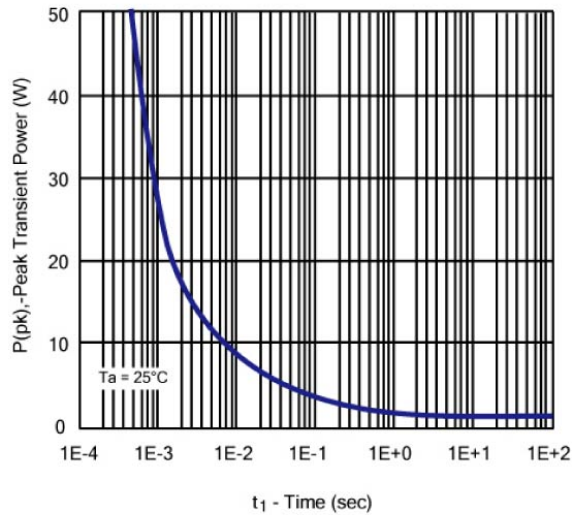
Body-diode characteristics



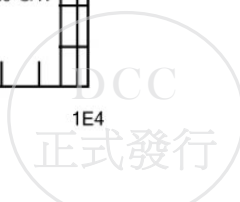
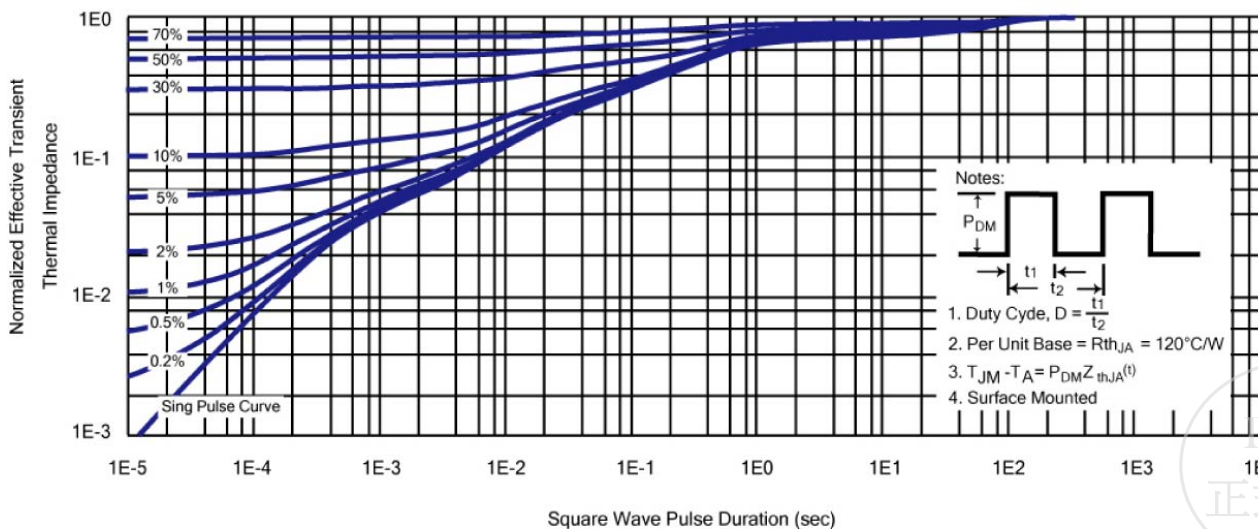
Maximum Forward Biased Safe Operating Area



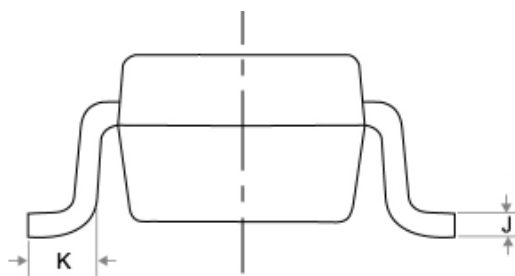
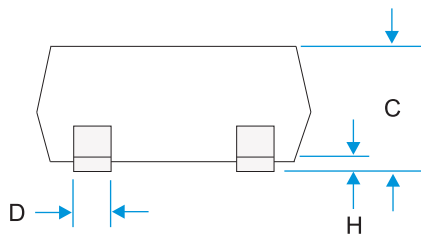
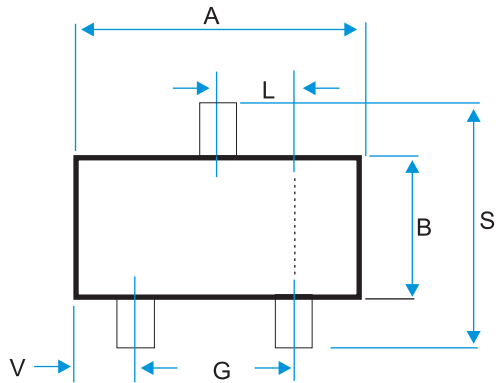
Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-23 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60



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