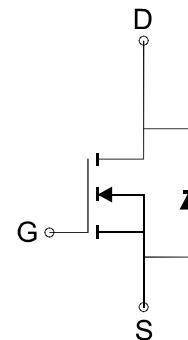
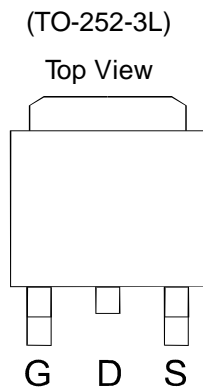


N-Channel 60-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME35N06-G is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on state resistance. These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

PIN CONFIGURATION



N-Channel MOSFET

FEATURES

- $R_{DS(ON)} \leq 32m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 40m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

Ordering Information: ME35N06/ME35N06-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V _{DS}	60	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current	I _D	T _c =25°C	25.4
		T _c =70°C	23.4
Pulsed Drain Current	I _{DM}	101	A
Maximum Power Dissipation	P _D	T _c =25°C	33
		T _c =70°C	21
Operating Junction Temperature	T _J	-55 to 150	°C
Thermal Resistance-Junction to Case *	R _{θJC}	3.8	°C/W

* The device mounted on 1in² FR4 board with 2 oz copper



N-Channel 60-V (D-S) MOSFET

Electrical Characteristics (T_c =25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	60			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1		3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =48V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =10V, I _D = 20A		27	32	mΩ
		V _{GS} =4.5V, I _D = 16A		34	40	
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =30V, V _{GS} =10V, I _D =20A		23		nC
Q _g	Total Gate Charge			12		
Q _{gs}	Gate-Source Charge	V _{DS} =30V, V _{GS} =4.5V, I _D =20A		4.8		
Q _{gd}	Gate-Drain Charge			6.2		
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		885		pF
C _{oss}	Output Capacitance			98		
C _{rss}	Reverse Transfer Capacitance			30		
t _{d(on)}	Turn-On Delay Time	V _{DS} =30V, R _L =1.5Ω, V _{GEN} =10V, R _G =3Ω		12		ns
t _r	Turn-On Rise Time			8		
t _{d(off)}	Turn-Off Delay Time			43		
t _f	Turn-Off Fall Time			4		

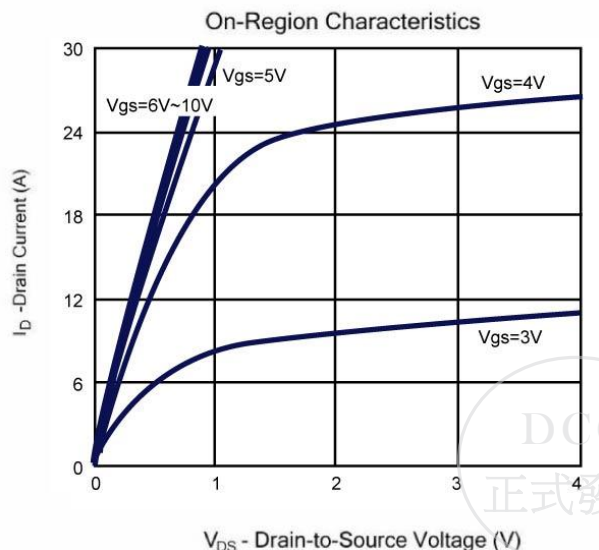
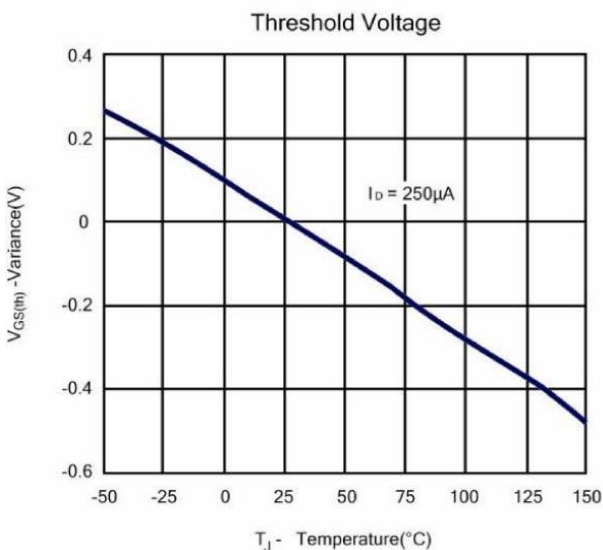
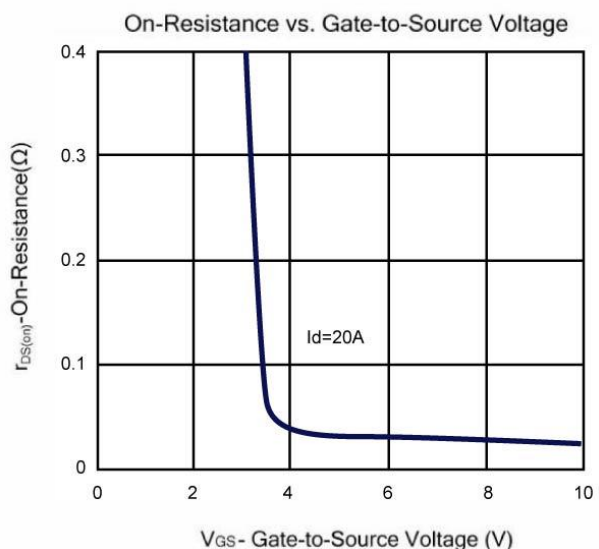
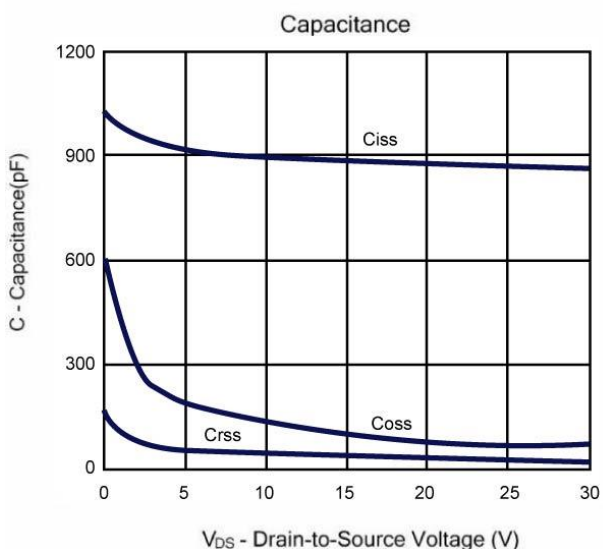
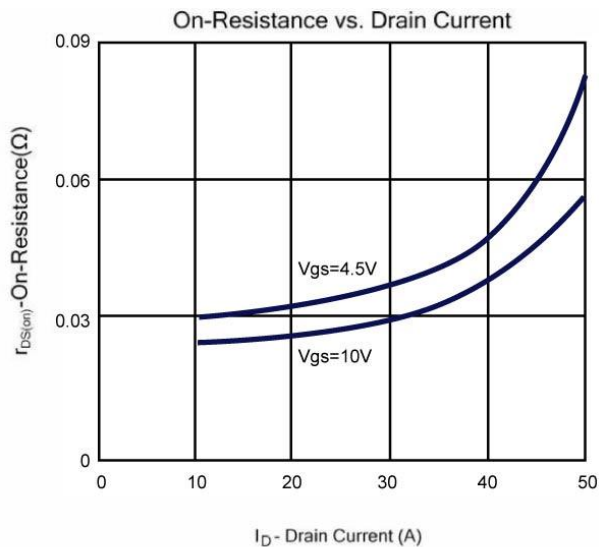
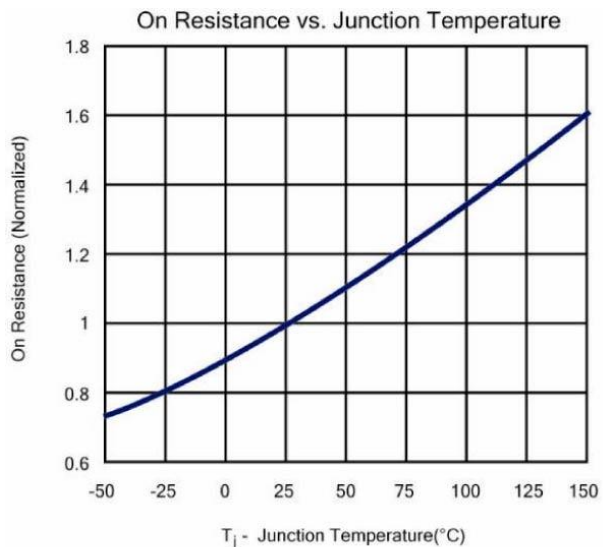
Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



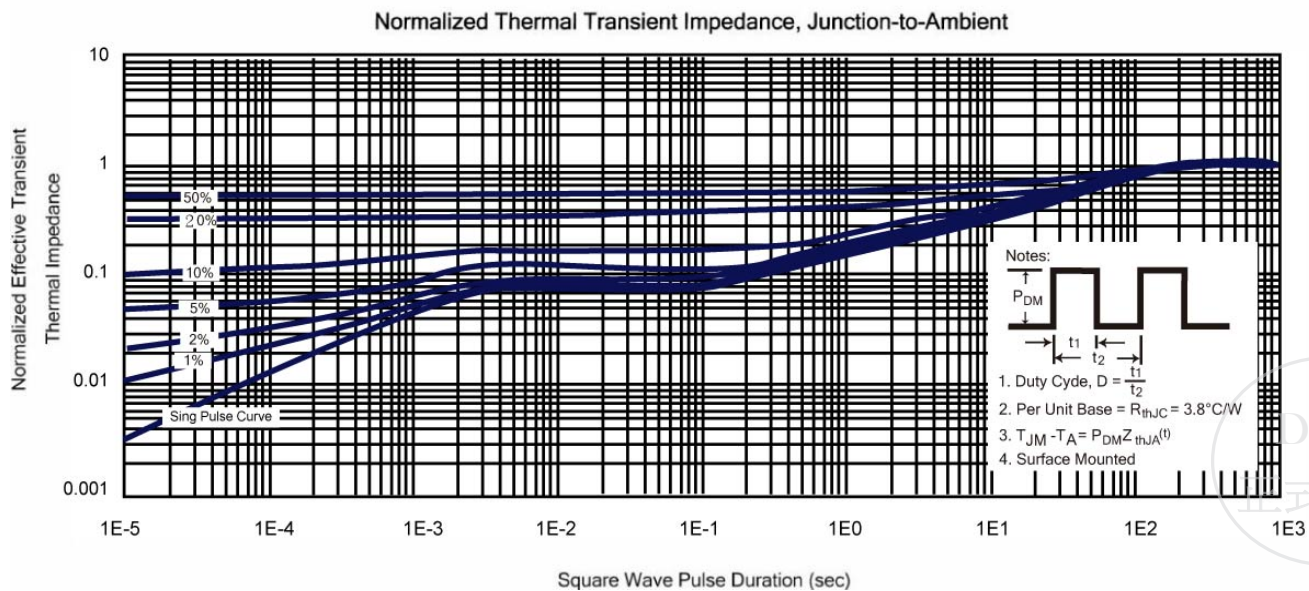
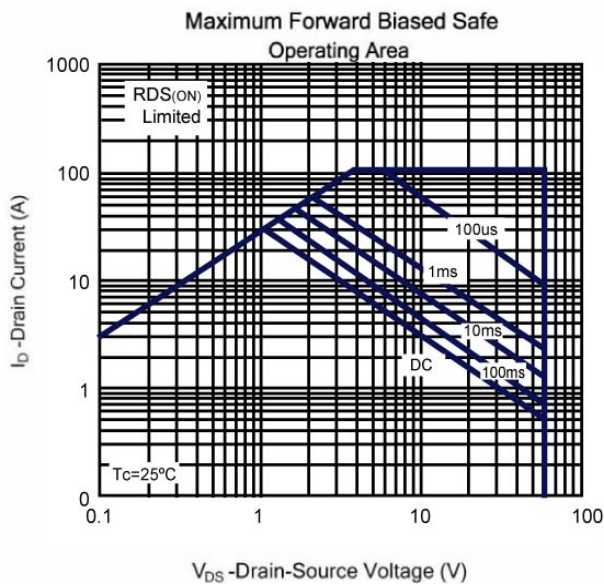
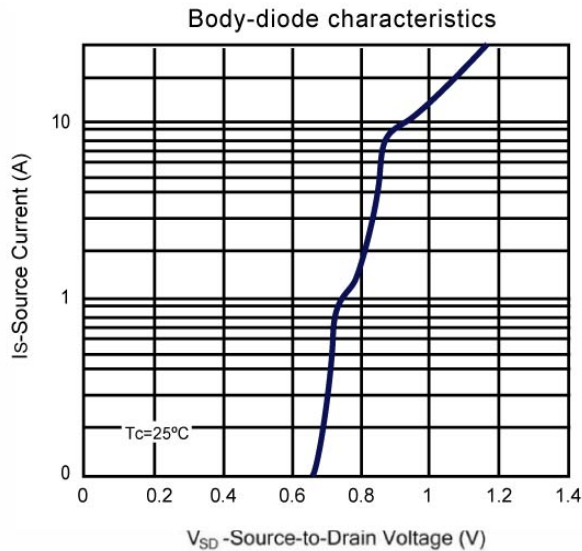
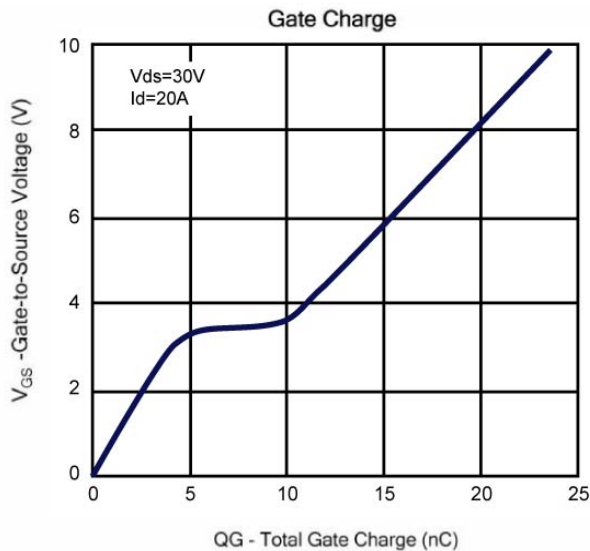
N-Channel 60-V (D-S) MOSFET

Typical Characteristics (T_J = 25°C Noted)

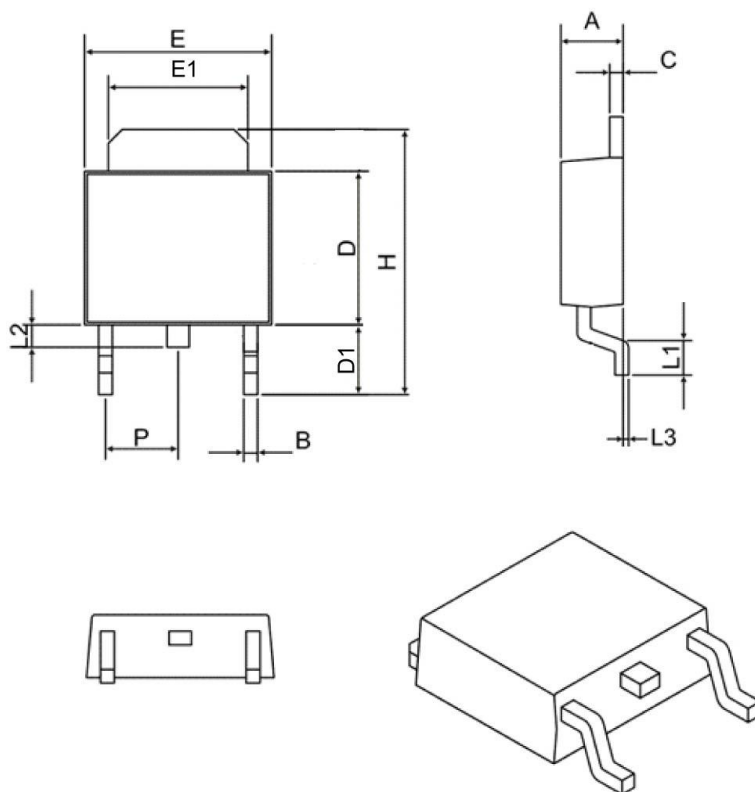


N-Channel 60-V (D-S) MOSFET

Typical Characteristics (T_J = 25°C Noted)



TO252-3L Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	



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