

**N and P- Channel 30-V (D-S) MOSFET**

**GENERAL DESCRIPTION**

The ME4542 is the N and P Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

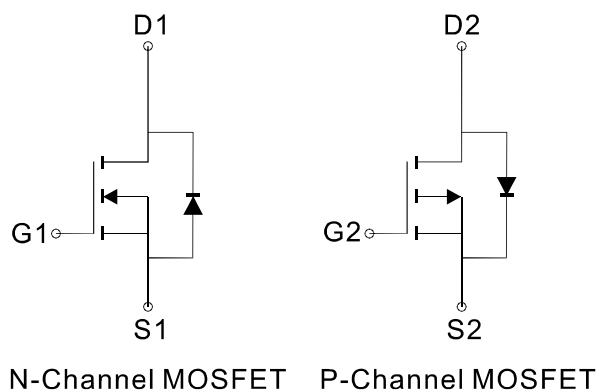
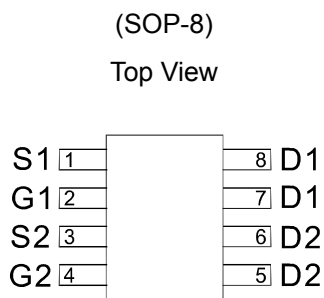
**FEATURES**

- R<sub>DS(ON)</sub> 25mΩ@V<sub>GS</sub>=10V (N-Ch)
- R<sub>DS(ON)</sub> 40mΩ@V<sub>GS</sub>=4.5V (N-Ch)
- R<sub>DS(ON)</sub> 35mΩ@V<sub>GS</sub>=-10V (P-Ch)
- R<sub>DS(ON)</sub> 58mΩ@V<sub>GS</sub>=-4.5V (P-Ch)
- Super high density cell design for extremely low R<sub>DS(ON)</sub>
- Exceptional on-resistance and maximum DC current capability

**APPLICATIONS**

- Power Management
- DC/DC Converter
- LCD TV & Monitor Display inverter
- CCFL inverter
- LCD Display inverter

**PIN CONFIGURATION**



**Ordering Information:** ME4542 (Pb-free)  
ME4542-G (Green product-Halogen free)

**Absolute Maximum Ratings (T<sub>A</sub>=25 Unless Otherwise Noted)**

Parameter	Symbol	N-Channel	P-Channel	Unit
		Maximum Ratings	Maximum Ratings	
Drain-Source Voltage	V <sub>DS</sub>	30	-30	V
Gate-Source Voltage	V <sub>GS</sub>	±20	±20	
Continuous Drain Current	I <sub>D</sub>	T <sub>A</sub> =25	-6	A
		T <sub>A</sub> =70	-4.8	
Pulsed Drain Current	I <sub>DM</sub>	28	-24	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>A</sub> =25	2	W
		T <sub>A</sub> =70	1.3	
Operating Junction Temperature	T <sub>J</sub>	-55 to 150		
Thermal Resistance-Junction to Ambient *	R <sub>θJA</sub>	62.5	62.5	/W

\*The device mounted on 1in2 FR4 board with 2 oz copper

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Electrical Characteristics (TA=25 Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>STATIC</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250 μA V <sub>GS</sub> =0V, I <sub>D</sub> =-250 μA	N-Ch P-Ch	30 -30		V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 μA V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250 μA	N-Ch P-Ch	1.0 -1.0	3.0 -3.0	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V	N-Ch P-Ch		±100 ±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V	N-Ch P-Ch		1 -1	μA
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance <sup>a</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> = 6.7A V <sub>GS</sub> =-10V, I <sub>D</sub> = -6.1A	N-Ch P-Ch	21 30	25 35	m
		V <sub>GS</sub> =4.5V, I <sub>D</sub> = 5.0A V <sub>GS</sub> =-4.5V, I <sub>D</sub> = -5.0A	N-Ch P-Ch	32 48	40 58	
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1.7A, V <sub>GS</sub> =0V I <sub>S</sub> =-1.7A, V <sub>GS</sub> =0V	N-Ch P-Ch	0.8 -0.8	1.2 -1.2	V
<b>DYNAMIC</b>						
Q <sub>g</sub>	Total Gate Charge	N-Channel V <sub>DS</sub> =15V, V <sub>GS</sub> =10V, I <sub>D</sub> =6.7A P-Channel V <sub>DS</sub> =-15V, V <sub>GS</sub> =-10V, I <sub>D</sub> =-6.1A	N-Ch P-Ch	12 21		nC
Q <sub>gs</sub>	Gate-Source Charge		N-Ch P-Ch	2 4		
Q <sub>gd</sub>	Gate-Drain Charge		N-Ch P-Ch	2.5 6		
C <sub>iss</sub>	Input Capacitance	N-Channel V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz P-Channel V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	N-Ch P-Ch	360 840		pF
C <sub>oss</sub>	Output Capacitance		N-Ch P-Ch	70 120		
C <sub>rss</sub>	Reverse Transfer Capacitance		N-Ch P-Ch	17 32		
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	N-Ch P-Ch	0.5 5.5		
t <sub>d(on)</sub>	Turn-On Delay Time	N-Channel V <sub>DD</sub> =15V, R <sub>L</sub> =15 I <sub>D</sub> =1A, V <sub>GEN</sub> =10V, R <sub>G</sub> =6  P-Channel V <sub>DD</sub> =-15V, R <sub>L</sub> =15 I <sub>D</sub> =-1A, V <sub>GEN</sub> =-10V, R <sub>G</sub> =6	N-Ch P-Ch	9.3 32		ns
t <sub>r</sub>	Turn-On Rise Time		N-Ch P-Ch	14 13		
t <sub>d(off)</sub>	Turn-Off Delay Time		N-Ch P-Ch	32 58		
t <sub>f</sub>	Turn-Off Fall Time		N-Ch P-Ch	3.2 6.8		

Notes: a. Pulse test; pulse width 300us, duty cycle 2%

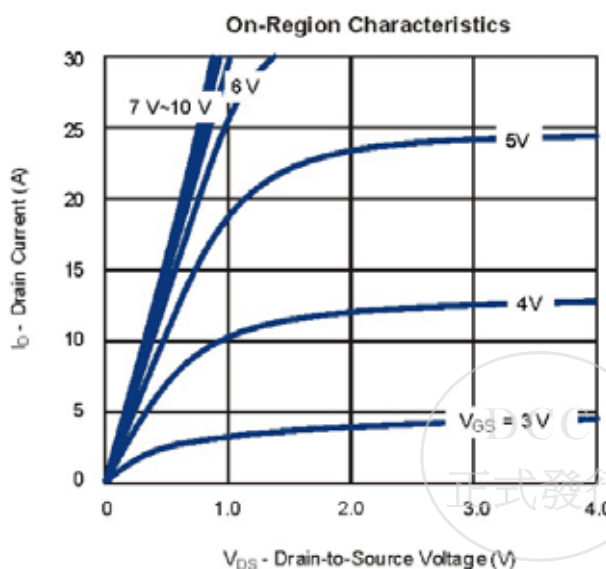
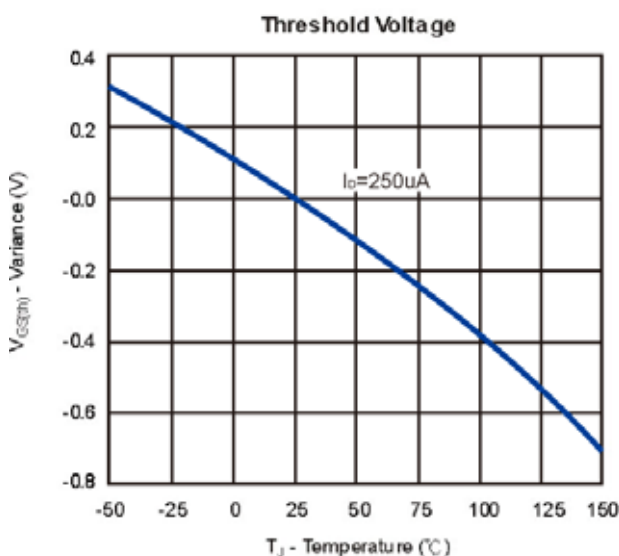
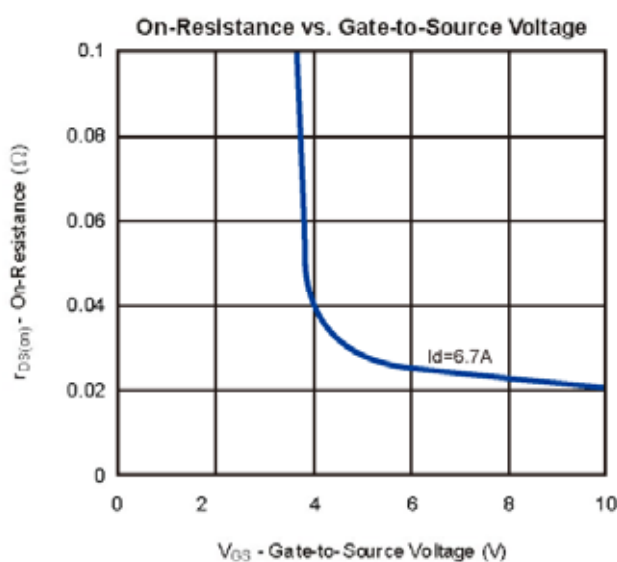
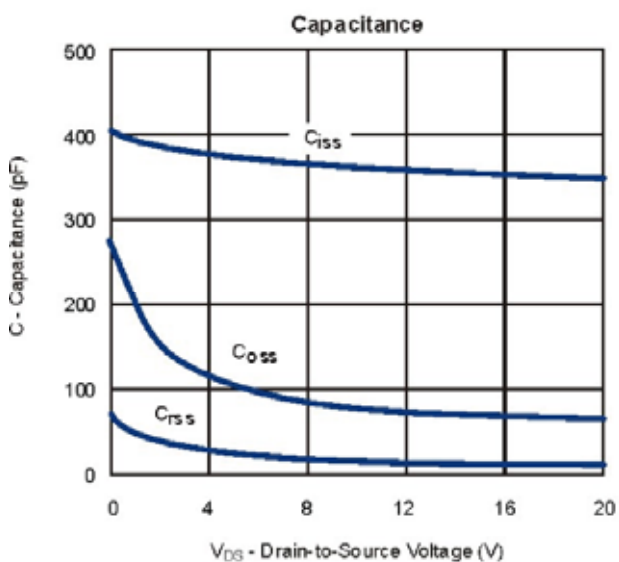
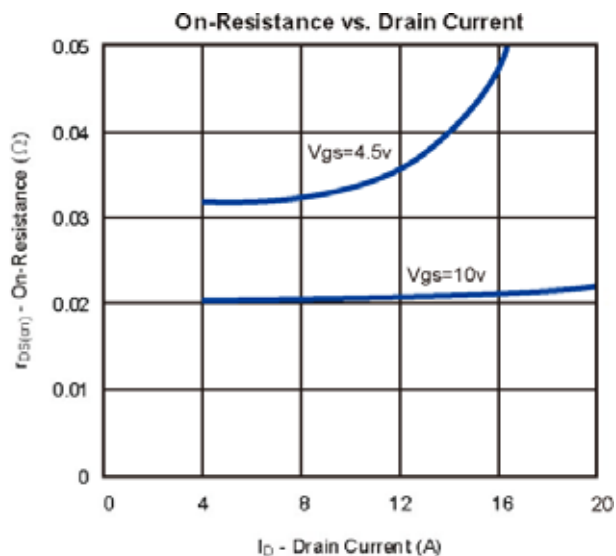
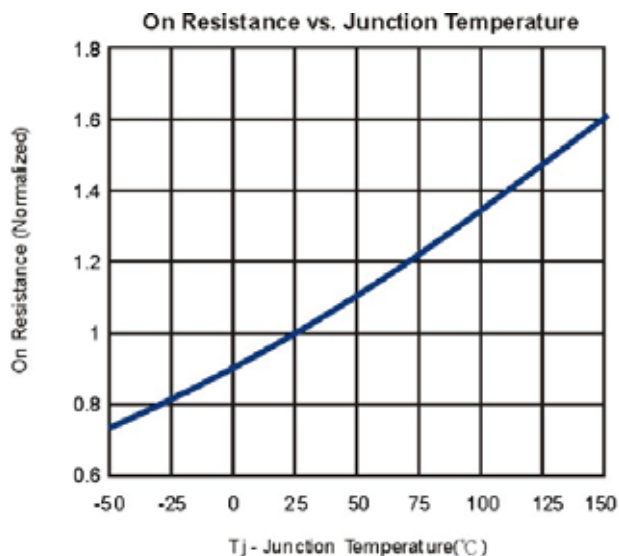
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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**N and P- Channel 30-V (D-S) MOSFET**

**Typical Characteristics (T<sub>J</sub> =25 Noted)**

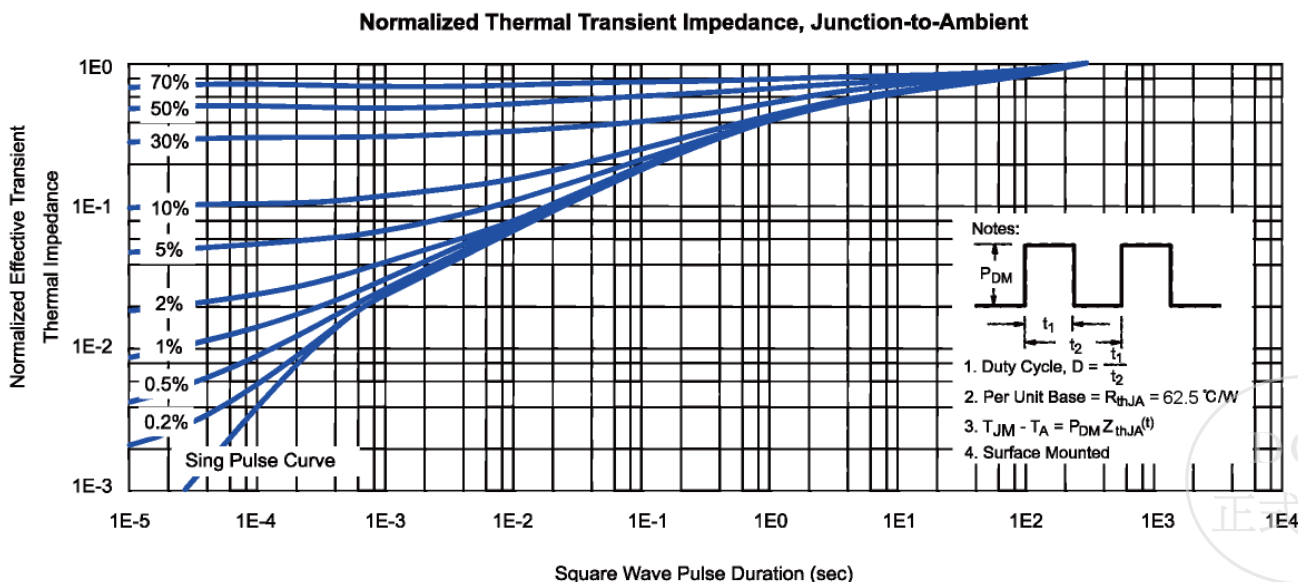
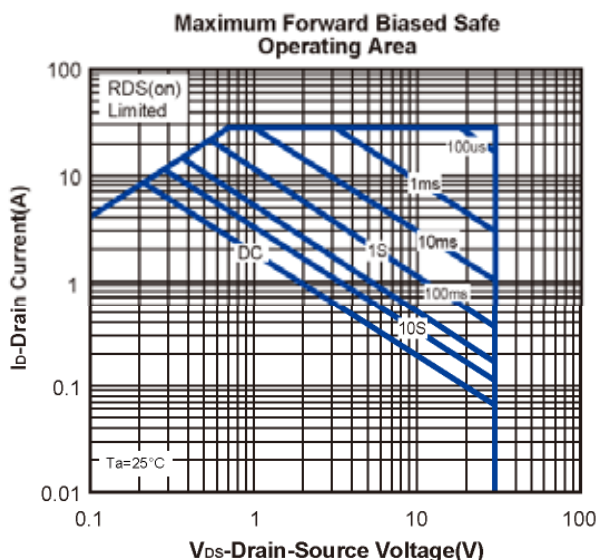
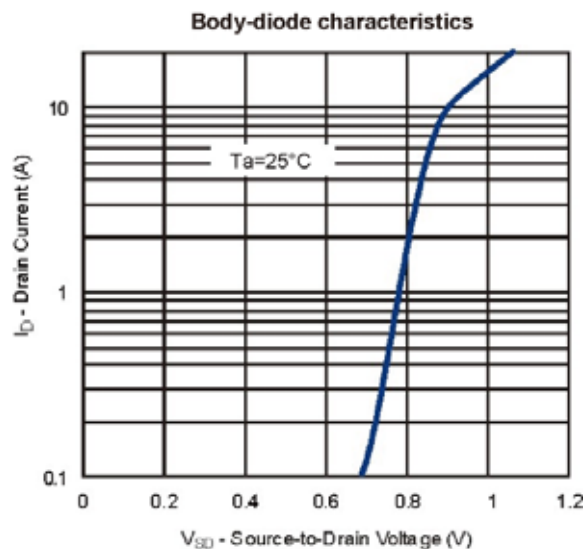
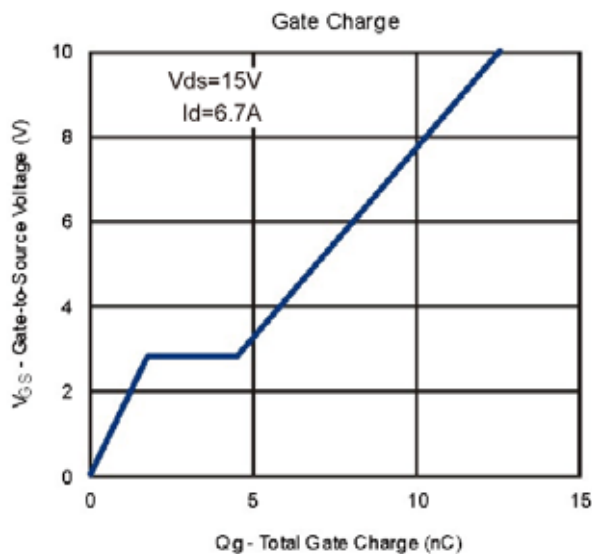
**N-CHANNEL**



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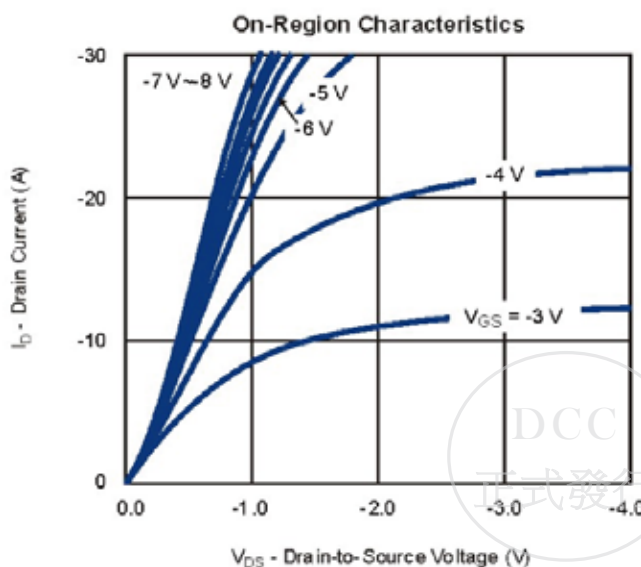
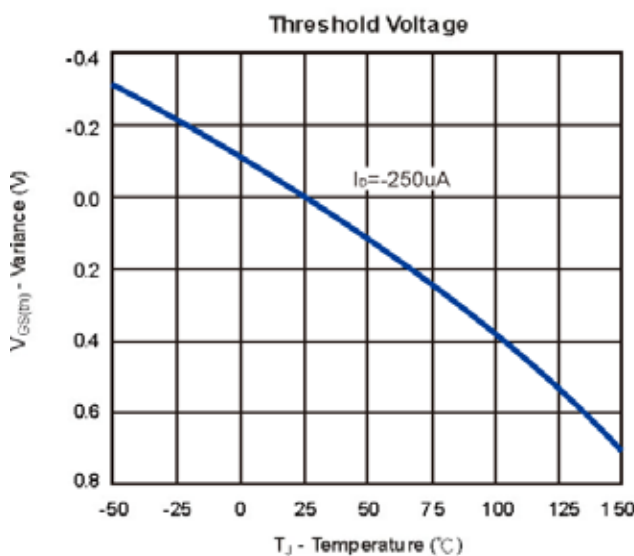
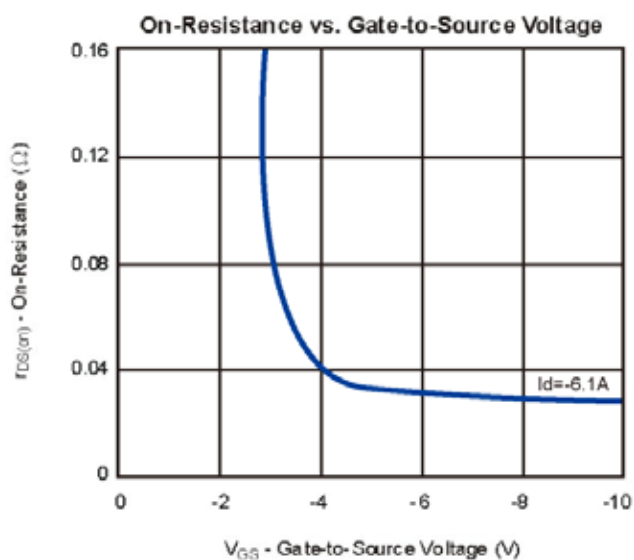
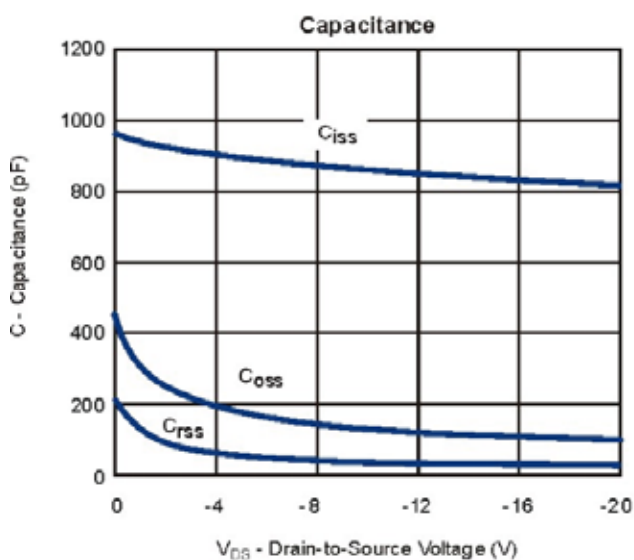
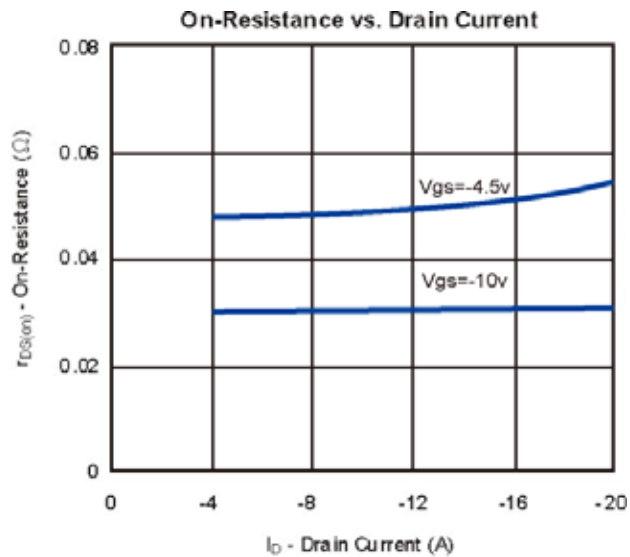
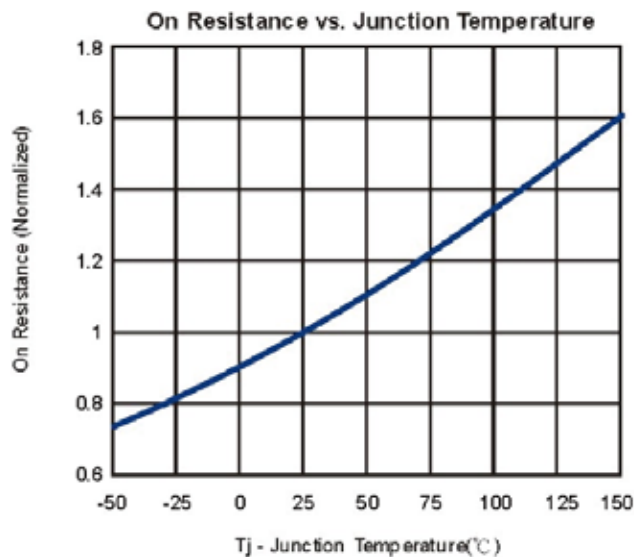
N-CHANNEL



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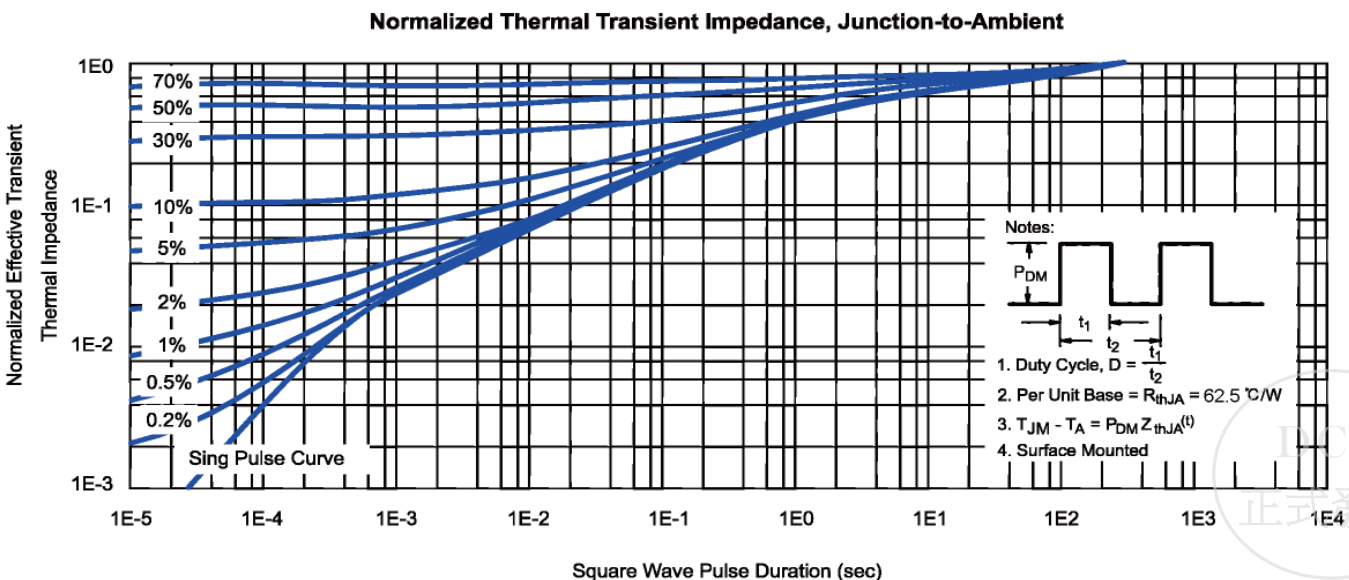
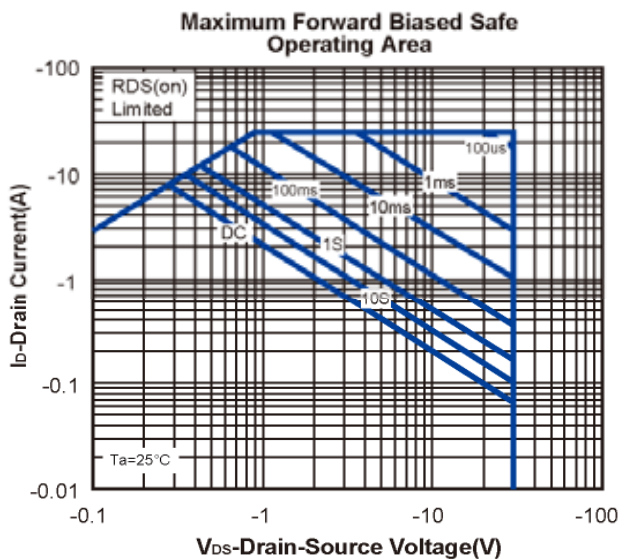
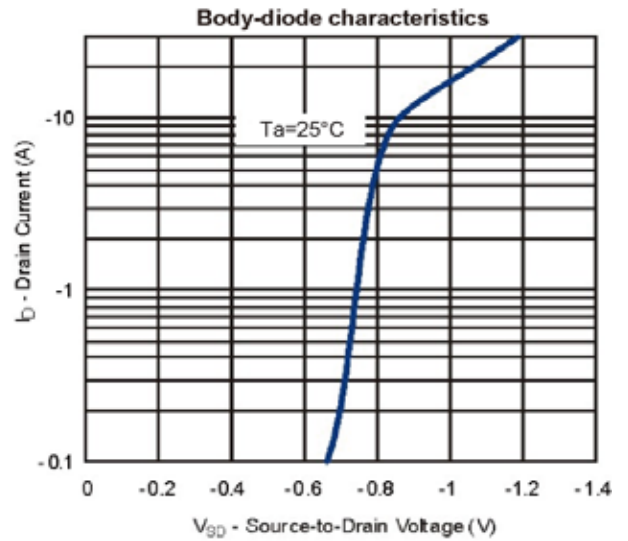
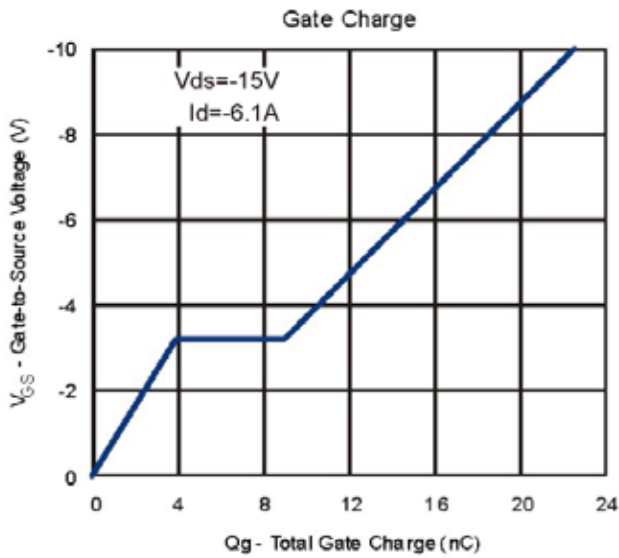
**P-CHANNEL**



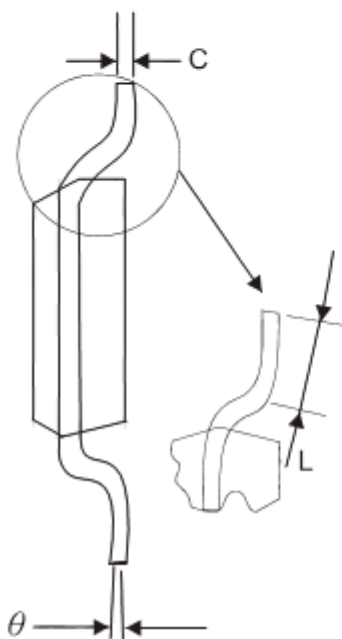
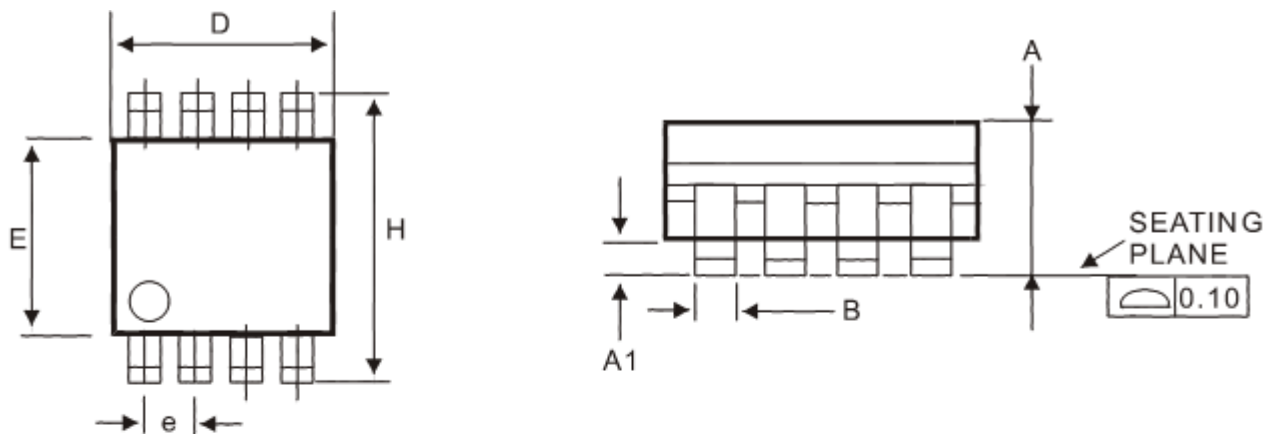
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Typical Characteristics (T<sub>J</sub> =25 Noted)

**P-CHANNEL**



**SOP-8 Package Outline**



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.



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