

GENERAL DESCRIPTION

The ME4565 is the N- and P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leq 40m\Omega @ V_{GS}=10V$ (N-Ch)
- $R_{DS(ON)} \leq 45m\Omega @ V_{GS}=4.5V$ (N-Ch)
- $R_{DS(ON)} \leq 54m\Omega @ V_{GS}=-10V$ (P-Ch)
- $R_{DS(ON)} \leq 60m\Omega @ V_{GS}=-4.5V$ (P-Ch)
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

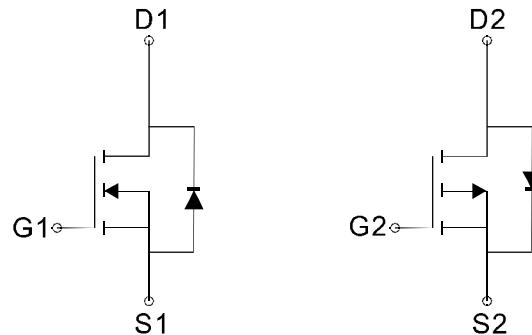
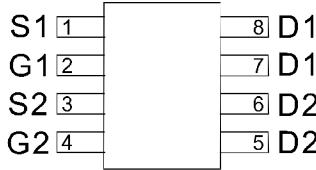
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(SOP-8)

Top View



N-Channel MOSFET

P-Channel MOSFET

Absolute Maximum Ratings ($T_A=25^\circ C$ Unless Otherwise Noted)

Parameter	Symbol	N-Channel		P-Channel		Unit
		10 secs	Steady State	10 secs	Steady State	
Drain-Source Voltage	V_{DSS}		40		-40	
Gate-Source Voltage	V_{GSS}		± 16		± 16	
Continuous Drain Current($T_j=150^\circ C$)	I_D	5.2	3.9	-4.5	-3.3	A
		4.2	3.1	-3.6	-2.7	
Pulsed Drain Current	I_{DM}	30		20		
Avalanche Current	I_{AS}	13		16		
Single Pulse Avalanche Energy		8.5		13		mJ
Maximum Power Dissipation	P_D	2.5	1.56	2.45	1.52	W
		2.0	1.3	2.0	1.27	
Operating Junction Temperature	T_J	-55 to 150				°C
Thermal Resistance-Junction to Ambient *	R_{JA}	50	80	51	82	°C/W
Thermal Resistance-Junction to Case	R_{JC}	49		50		°C/W

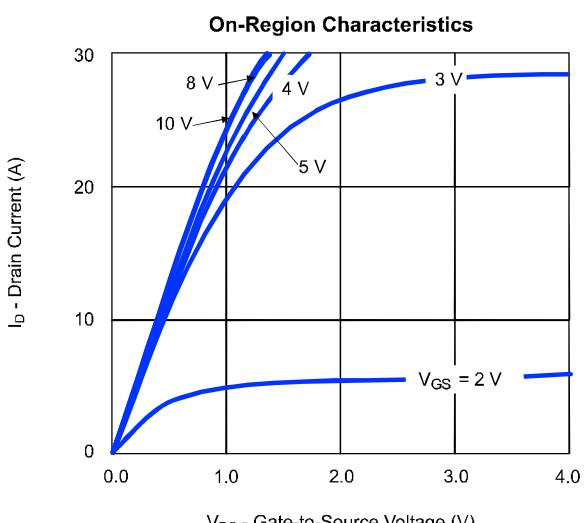
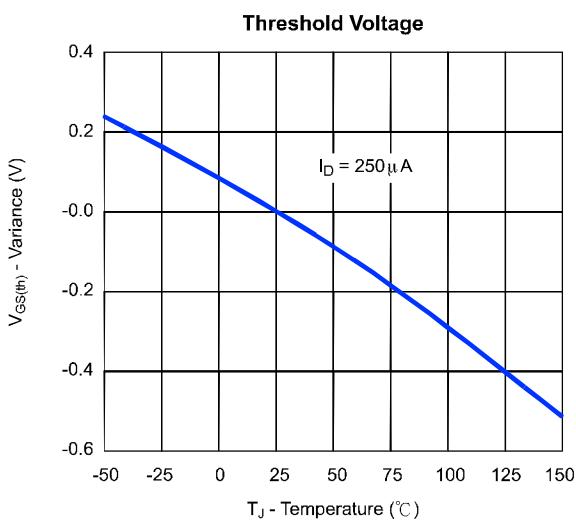
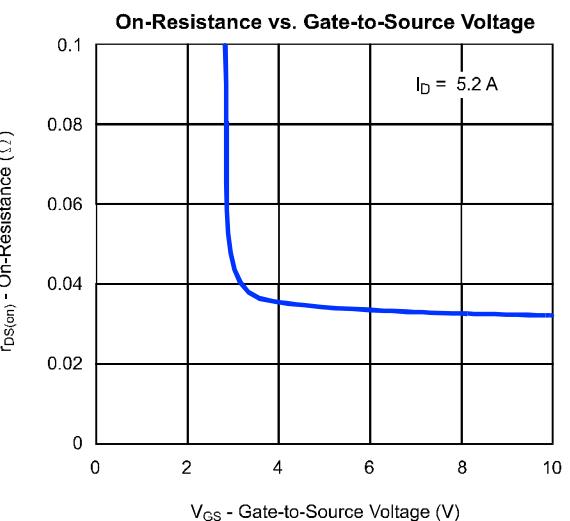
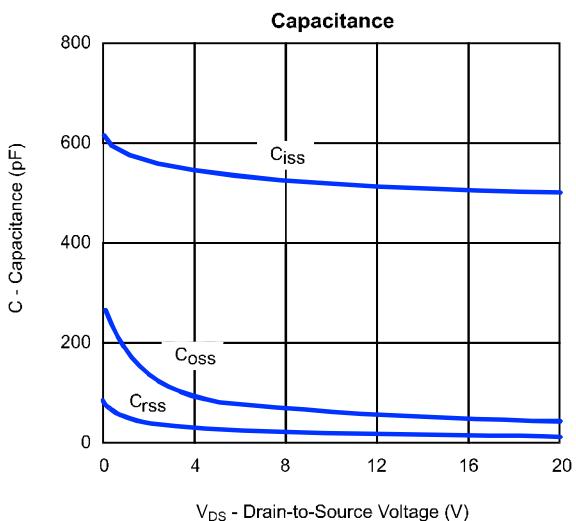
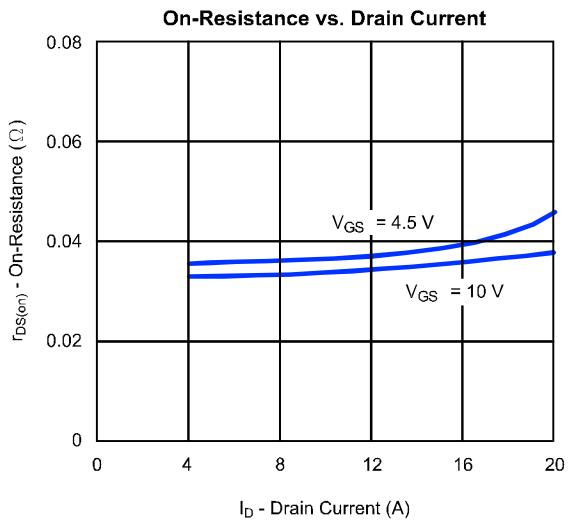
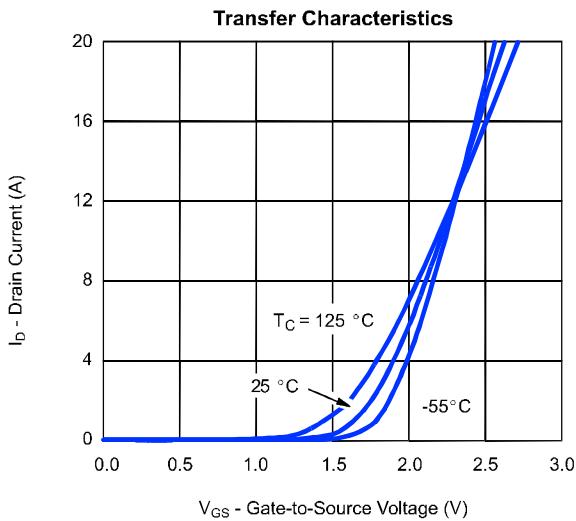
*The device mounted on 1in² FR4 board with 2 oz copper

Electrical Characteristics ($T_A = 25^\circ C$ Unless Otherwise Specified)

Symbol	Parameter	Limit		Min	Typ	Max	Unit
STATIC							
V(BR)DSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250 \mu A$ $V_{GS}=0V, I_D=-250 \mu A$	N-Ch P-Ch	40 -40			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250 \mu A$ $V_{DS}=V_{GS}, I_D=-250 \mu A$	N-Ch P-Ch	0.6 -0.8	0.9 -1.0	1.6 -1.8	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 16V$ $V_{DS}=0V, V_{GS}=\pm 16V$	N-Ch P-Ch			± 100 ± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=40V, V_{GS}=0V$ $V_{DS}=-40V, V_{GS}=0V$	N-Ch P-Ch			1 -1	μA
		$V_{DS}=40V, V_{GS}=0V, T_J=55^\circ C$ $V_{DS}=-40V, V_{GS}=0V, T_J=55^\circ C$	N-Ch P-Ch			10 -10	
$I_{D(ON)}$	On-State Drain Current	$V_{DS} \geq 5V, V_{GS}= 10V$ $V_{DS} \leq -5V, V_{GS}=-10V$	N-Ch P-Ch	20 -20			A
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D= 5.2A$ $V_{GS}=-10V, I_D= -4.5A$	N-Ch P-Ch		32 43	40 54	$m\Omega$
		$V_{GS}=4.5V, I_D= 4.9A$ $V_{GS}=-4.5V, I_D= -3.9A$	N-Ch P-Ch		35 48	45 60	
G_{FS}	Forward Transconductance	$V_{DS}=15V, I_D=5.2A$ $V_{DS}=-15V, I_D=-4.5A$	N-Ch P-Ch		18 13		S
V_{SD}	Diode Forward Voltage	$I_S=1.7A, V_{GS}=0V$ $I_S=-1.7A, V_{GS}=0V$	N-Ch P-Ch		0.78 -0.79	1.2 -1.2	V
DYNAMIC							
Q_g	Total Gate Charge	N-Channel $V_{DS}=20V, V_{GS}=4.5V, I_D=5.2A$ P-Channel $V_{DS}=-20V, V_{GS}=-4.5V, I_D=-4.5A$	N-Ch P-Ch		8 12	10 14	nC
Q_{gs}	Gate-Source Charge		N-Ch P-Ch		3.3 5		
Q_{gd}	Gate-Drain Charge		N-Ch P-Ch		2.8 5.2		
R_g	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, f=1MHz$ $V_{GS}=0V, V_{DS}=0V, f=1MHz$	N-Ch P-Ch		0.7 4.5		Ω
C_{iss}	Input capacitance	N-Channel $V_{DS}=20V, V_{GS}=0V, F=1MHz$ P-Channel $V_{DS}=-20V, V_{GS}=0V, F=1MHz$	N-Ch P-Ch		500 1000	600 1100	pF
C_{oss}	Output Capacitance		N-Ch P-Ch		43 81		
C_{rss}	Reverse Transfer Capacitance		N-Ch P-Ch		9.3 22		
$t_{d(on)}$	Turn-On Delay Time	N-Channel $V_{DD}=15V, R_L=15\Omega$ $I_D=1A, V_{GEN}=10V, R_G=6\Omega$ P-Channel $V_{DD}=-15V, R_L=15\Omega$ $I_D=-1A, V_{GEN}=-10V, R_G=6\Omega$	N-Ch P-Ch		8 30	11 38	ns
t_r	Turn-On Rise Time		N-Ch P-Ch		15 12	20 18	
$t_{d(off)}$	Turn-Off Delay Time		N-Ch P-Ch		36 62	45 70	
t_f	Turn-On Fall Time		N-Ch P-Ch		2 5	5 8	

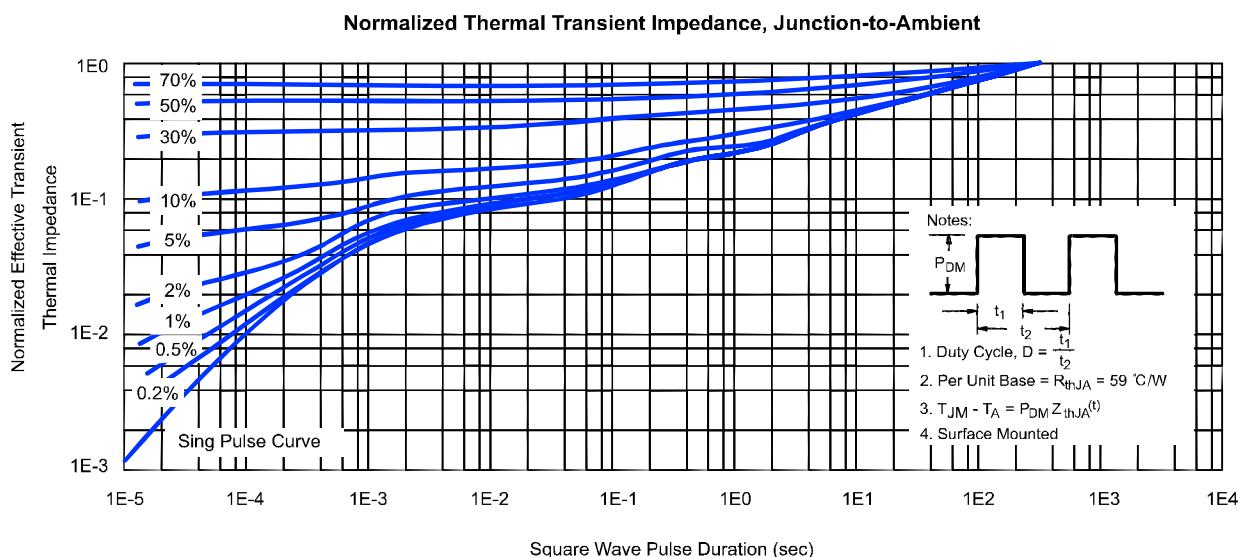
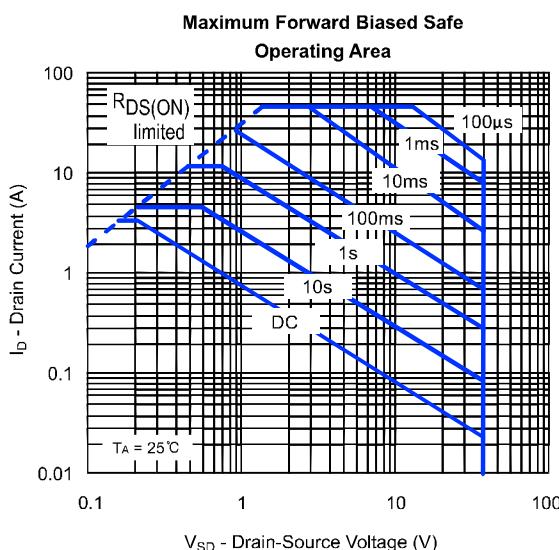
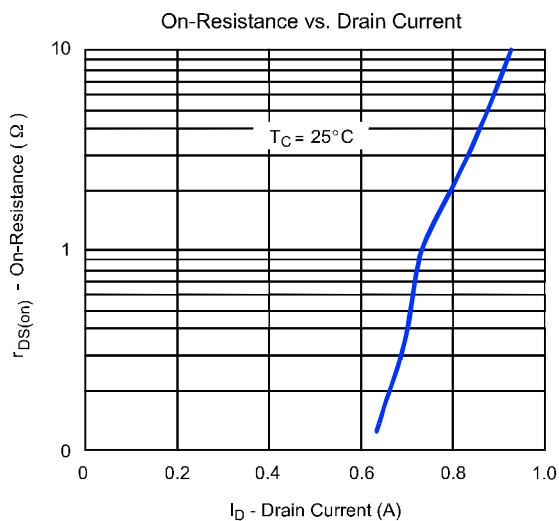
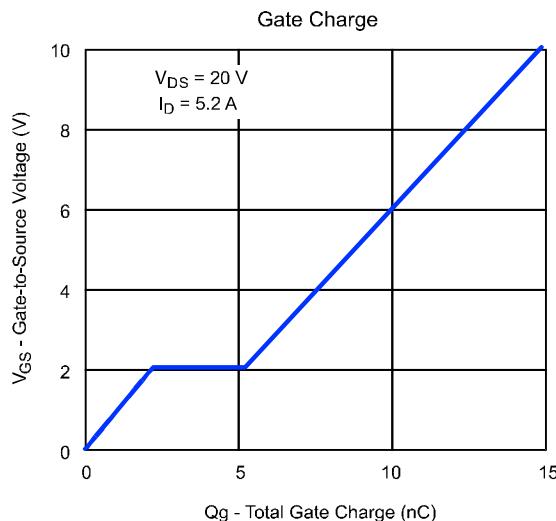
Typical Characteristics ($T_J = 25^\circ\text{C}$ Noted)

N-CHANNEL

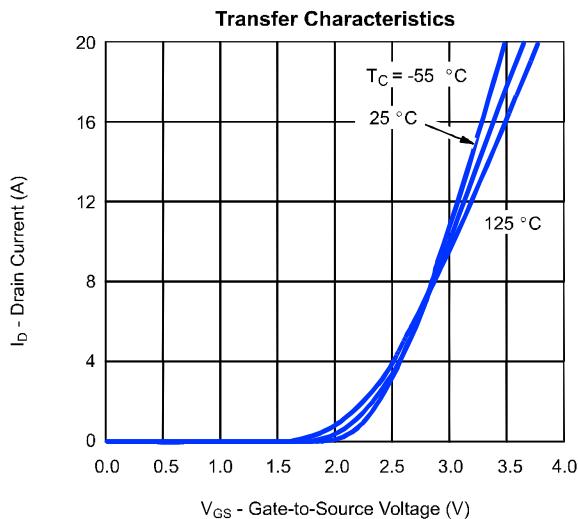


Typical Characteristics (T_J = 25°C Noted)

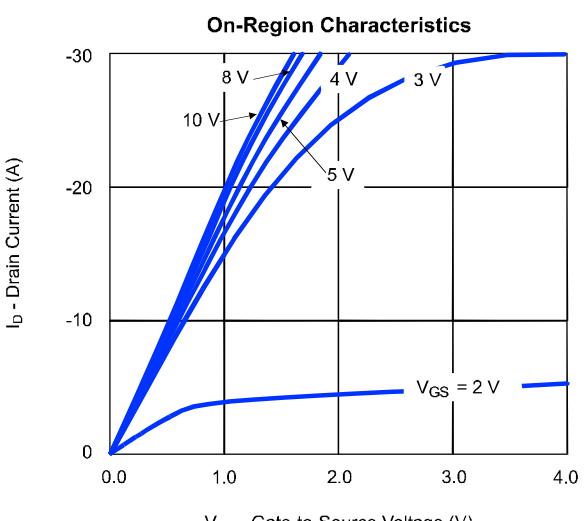
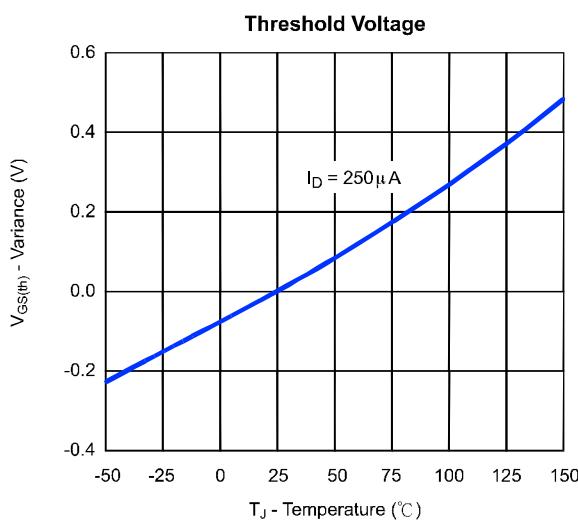
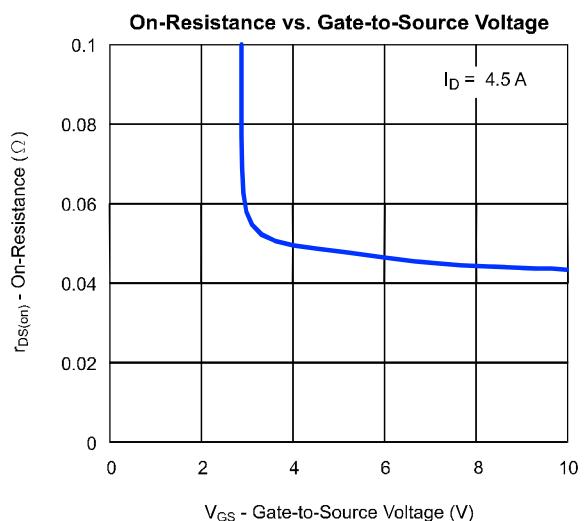
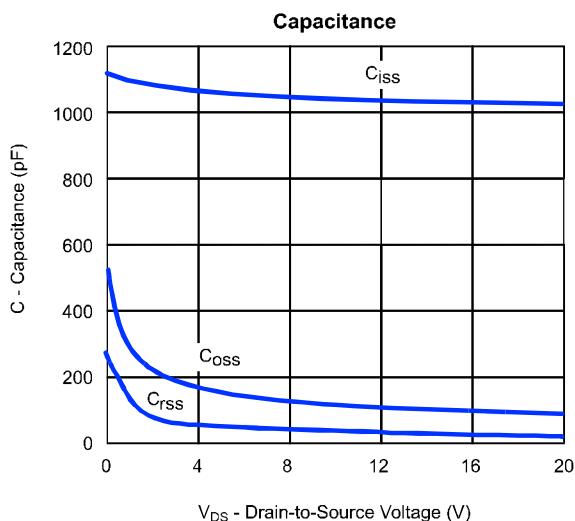
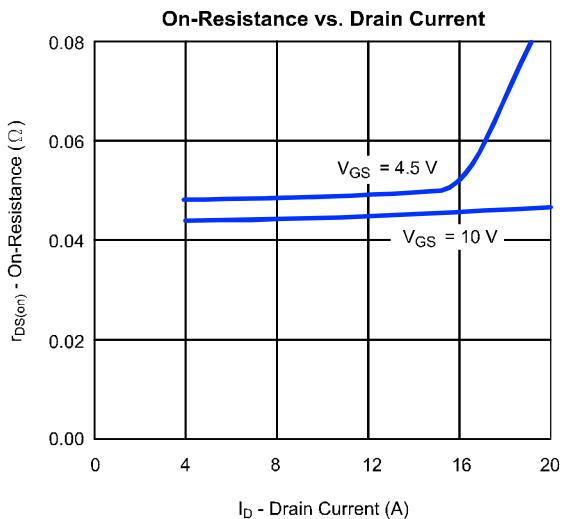
N-CHANNEL



Typical Characteristics ($T_J = 25^\circ\text{C}$ Noted)



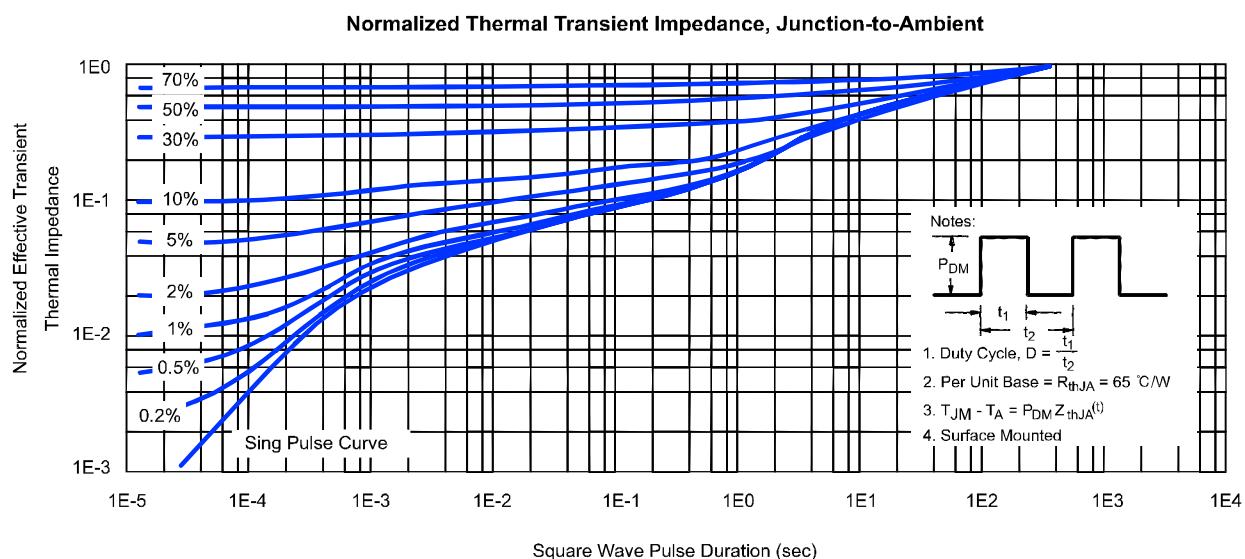
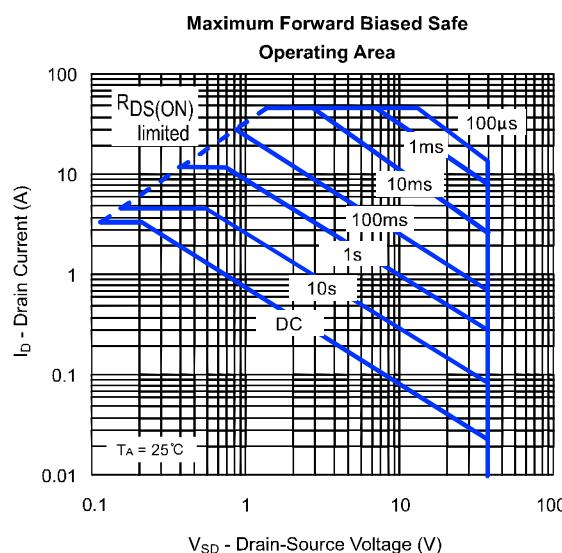
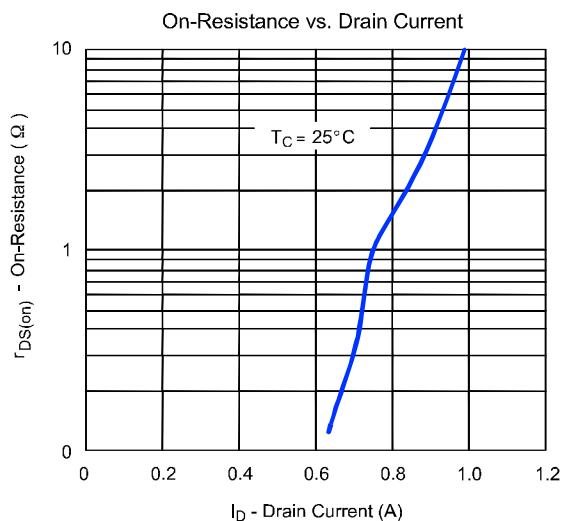
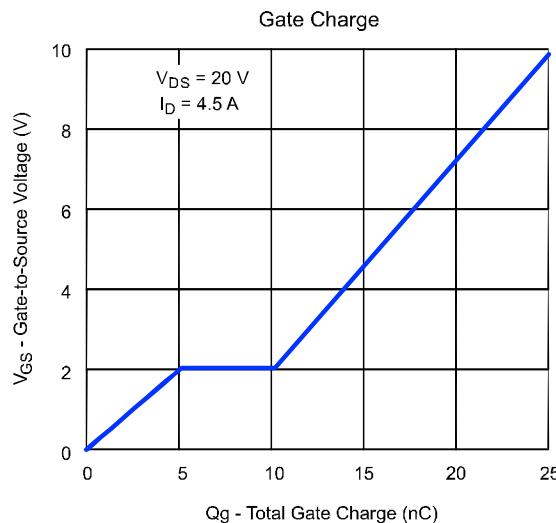
P-CHANNEL



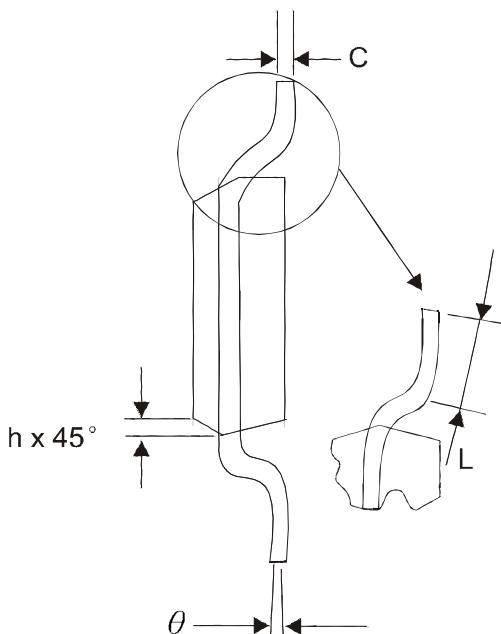
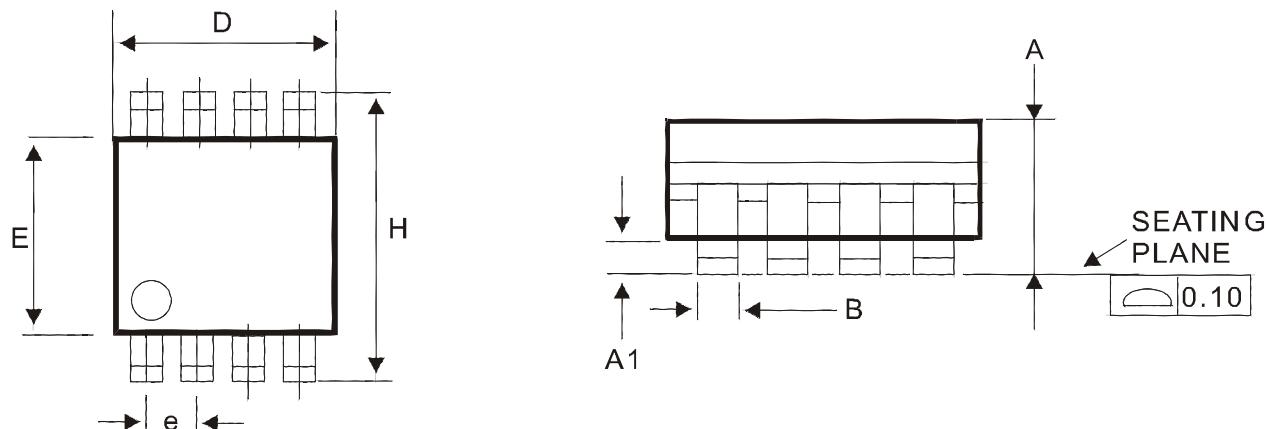
N- and P-Channel 40-V (D-S) MOSFET

Typical Characteristics ($T_J = 25^\circ\text{C}$ Noted)

P-CHANNEL



SOP-8 Package Outline



DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

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