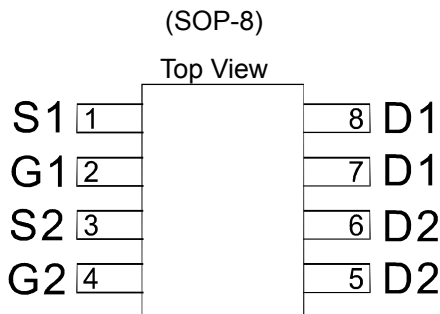


N- and P-Channel 40-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4565A is the N and P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION



Ordering Information: ME4565A (Pb-free)

ME4565A-G (Green product-Halogen free)

FEATURES

$R_{DS(ON)}$ 26.5m Ω @ $V_{GS}=10V$ (N-Ch)

$R_{DS(ON)}$ 45m Ω @ $V_{GS}=4.5V$ (N-Ch)

$R_{DS(ON)}$ 44m Ω @ $V_{GS}=-10V$ (P-Ch)

$R_{DS(ON)}$ 60m Ω @ $V_{GS}=-4.5V$ (P-Ch)

Super high density cell design for extremely low $R_{DS(ON)}$

Exceptional on-resistance and maximum DC current capability

APPLICATIONS

Power Management in Note book

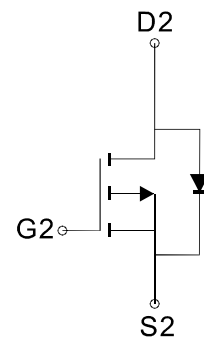
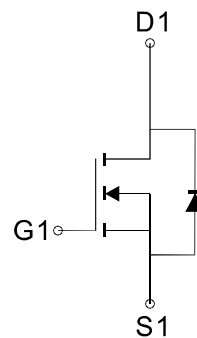
Portable Equipment

Battery Powered System

DC/DC Converter

Load Switch

LCD Display inverter



Absolute Maximum Ratings (TA=25 Unless Otherwise Noted)

Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	V_{DSS}	40	-40	V	
Gate-Source Voltage	V_{GSS}	± 20	± 20	V	
Continuous Drain Current($T_j=150$)*	I_D	$T_A=25$	6.9	-5.3	A
		$T_A=70$	5.5	-4.3	
Pulsed Drain Current	I_{DM}	27	-21	A	
Maximum Power Dissipation	P_D	$T_A=25$	2	2	W
		$T_A=70$	1.3	1.3	
Operating Junction Temperature	T_J	-55 to 150			
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	62.5	62.5	/W	

*The device mounted on 1in² FR4 board with 2 oz copper



N Channel 40-V (D-S) MOSFET

Electrical Characteristics (TA=25 Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	40			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1		3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =10V, I _D =5.2A		22	26.5	m
		V _{GS} =4.5V, I _D =4.9A		35	45	
V _{SD}	Diode Forward Voltage	I _S =6A, V _{GS} =0V		0.86	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =20V, V _{GS} =10V, I _D =6A		15		nC
Q _g	Total Gate Charge	V _{DS} =20V, V _{GS} =4.5V, I _D =6A		7		
Q _{gs}	Gate-Source Charge			4.1		
Q _{gd}	Gate-Drain Charge			3.4		
C _{iss}	Input capacitance	V _{DS} =15V, V _{GS} =0V, F=1MHz		565		pF
C _{oss}	Output Capacitance			76		
C _{rss}	Reverse Transfer Capacitance			24		
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		1		
t _{d(on)}	Turn-On Delay Time	V _{DD} =15V, R _L =15 I _D =1A, V _{GEN} =10V, R _G =6		13		ns
t _r	Turn-On Rise Time			14		
t _{d(off)}	Turn-Off Delay Time			36		
t _f	Turn-On Fall Time			4		

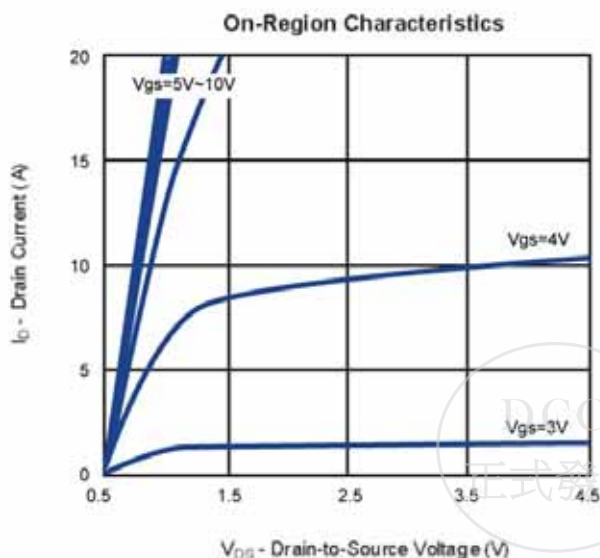
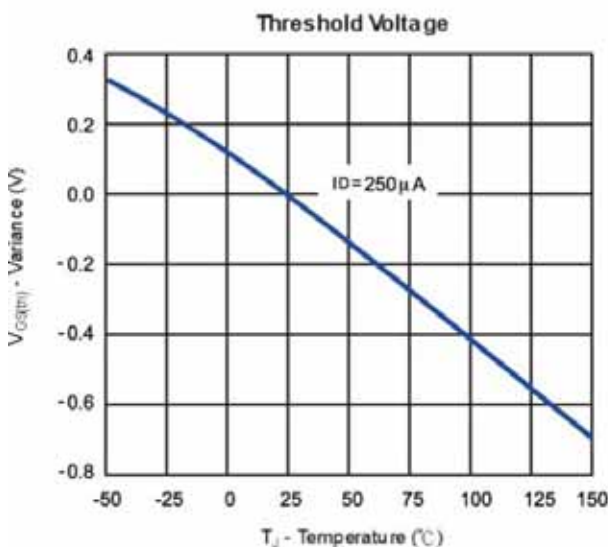
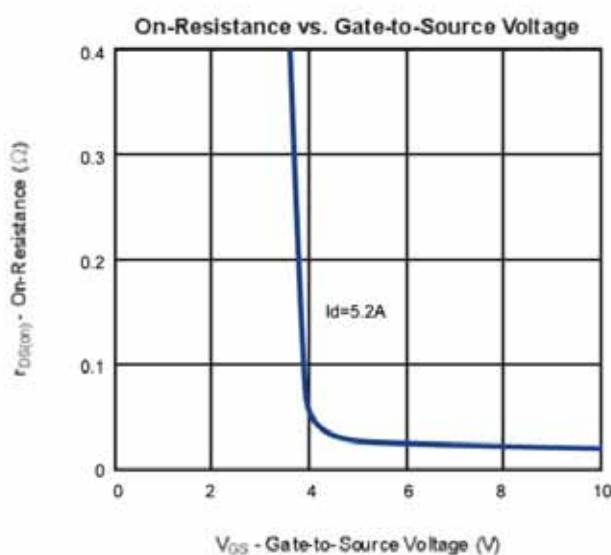
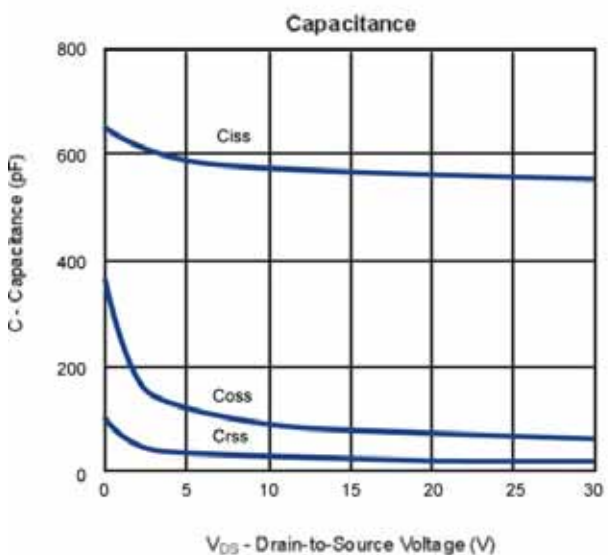
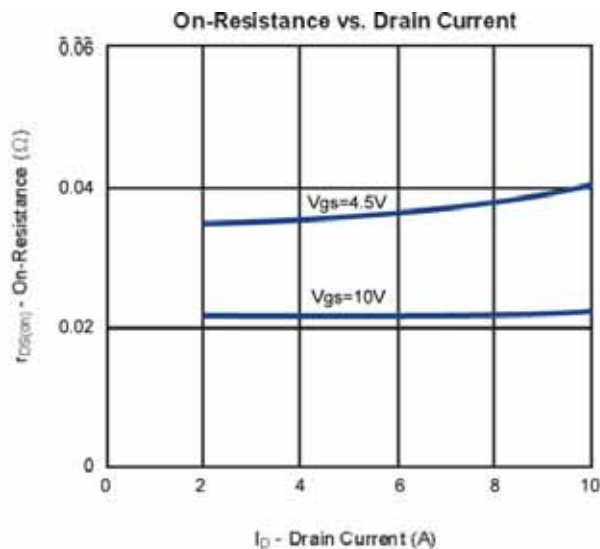
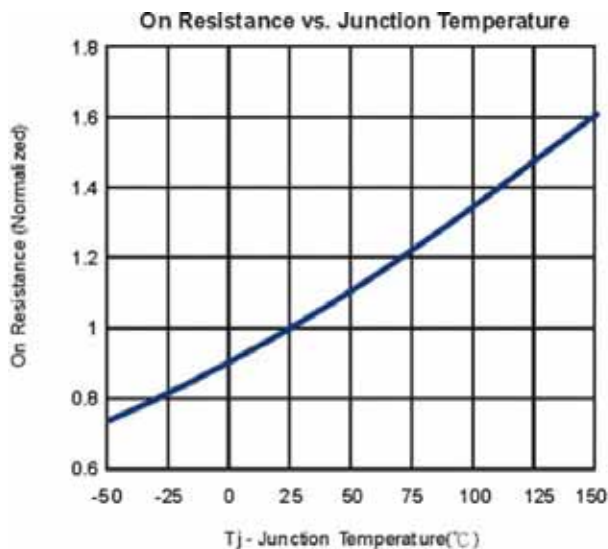
Notes: a. Pulse test: pulse width 300us, duty cycle 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.



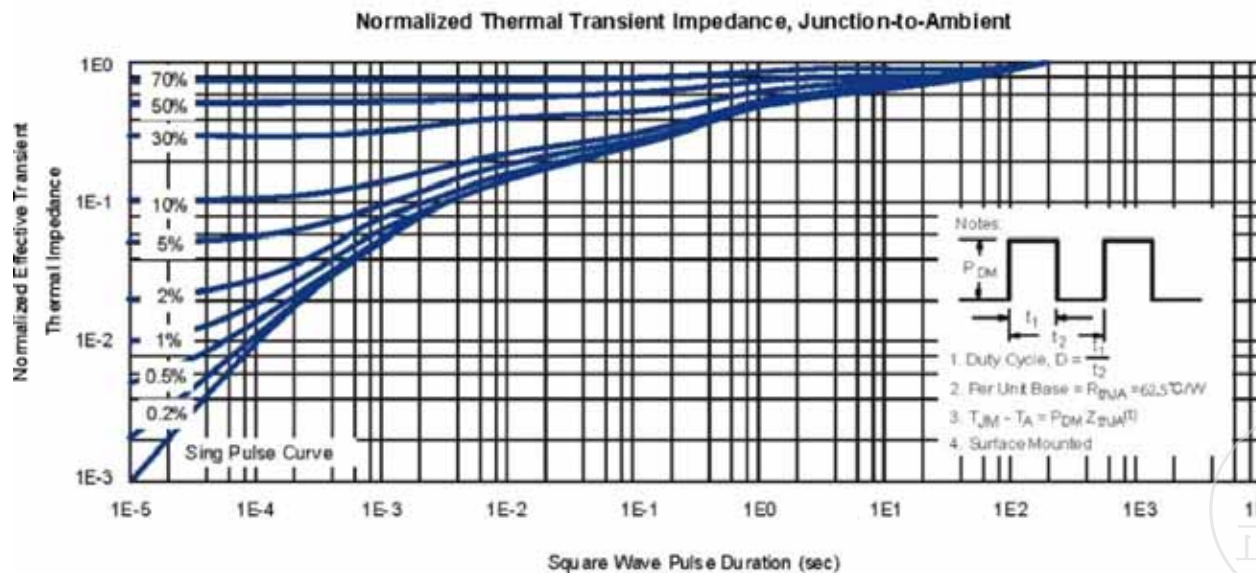
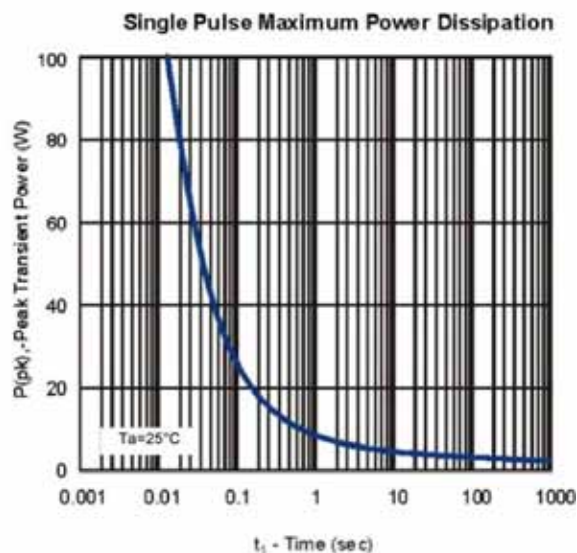
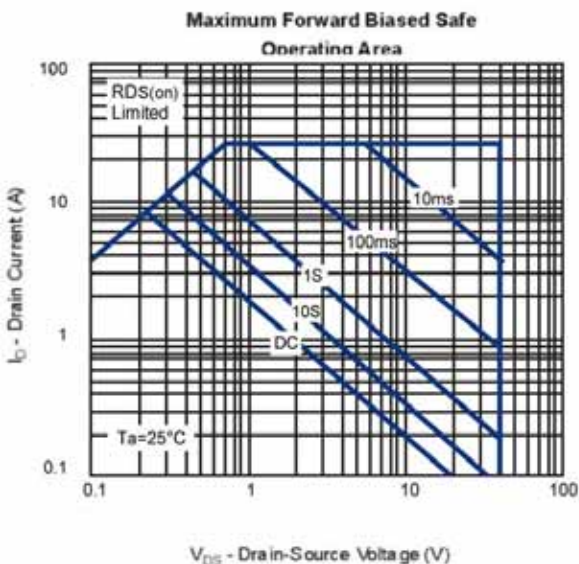
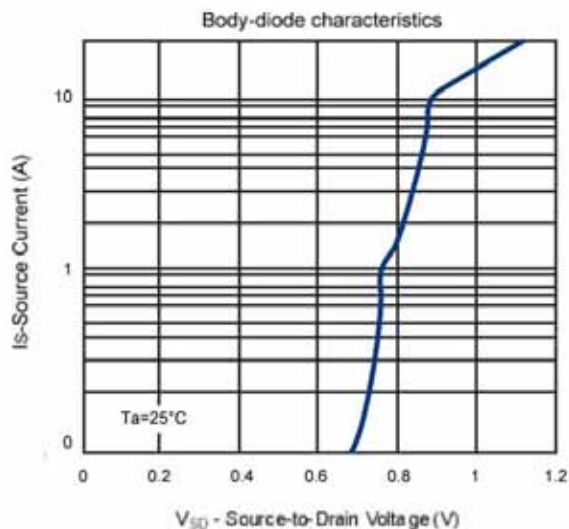
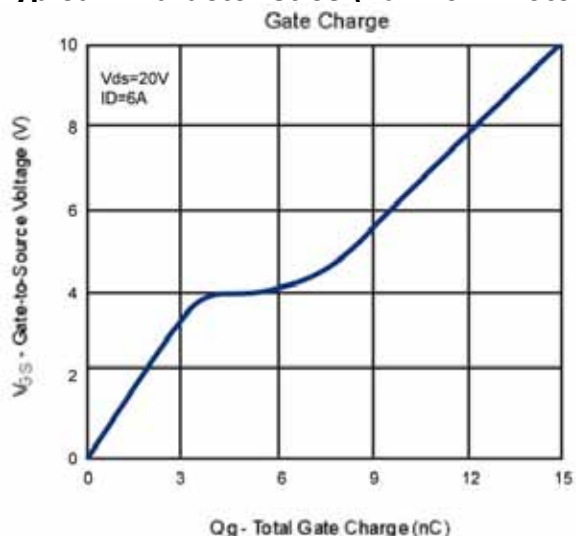
N Channel 40-V (D-S) MOSFET

Typical Characteristics (T_J =25 Noted)



N Channel 40-V (D-S) MOSFET

Typical Characteristics (T_J =25 Noted)



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P Channel 40-V (D-S) MOSFET

Electrical Characteristics (TA=25 Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250 μA	-40			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μA	-1		-3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-40V, V _{GS} =0V			-1	μA
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =-10V, I _D =-5A		36	44	m
		V _{GS} =-4.5V, I _D =-2A		47	60	
V _{SD}	Diode Forward Voltage	I _S =-5 A, V _{GS} =0V		-0.86	-1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =-20V, V _{GS} =-10V, I _D =-5A		20		nC
Q _g	Total Gate Charge	V _{DS} =-20V, V _{GS} =-4.5V, I _D =-5A		10		
Q _{gs}	Gate-Source Charge			4.1		
Q _{gd}	Gate-Drain Charge			4.9		
C _{iss}	Input capacitance	V _{DS} =-15V, V _{GS} =0V, F=1MHz		859		pF
C _{oss}	Output Capacitance			126		
C _{rss}	Reverse Transfer Capacitance			41		
t _{d(on)}	Turn-On Delay Time	V _{DD} =-15V, R _L =15 I _D =-1A, V _{GEN} =-10V, R _G =6		39		ns
t _r	Turn-On Rise Time			19		
t _{d(off)}	Turn-Off Delay Time			59		
t _f	Turn-On Fall Time			9		

Notes: a. Pulse test: pulse width 300us, duty cycle 2%, Guaranteed by design, not subject to production testing.

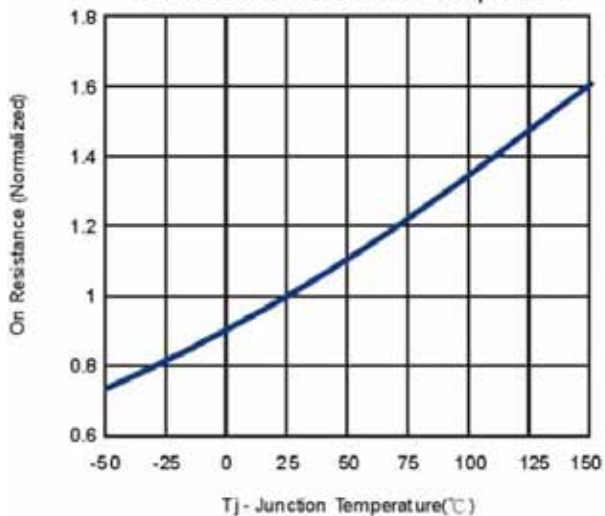
b. Matsuki reserves the right to improve product design, functions and reliability without notice.



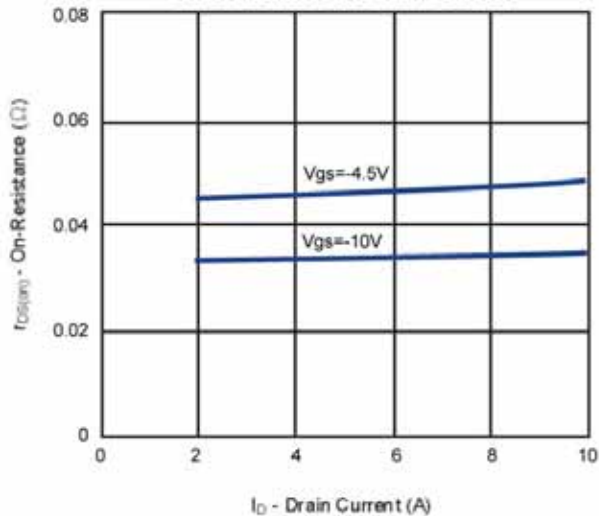
P Channel 40-V (D-S) MOSFET

Typical Characteristics (T_J = 25 Noted)

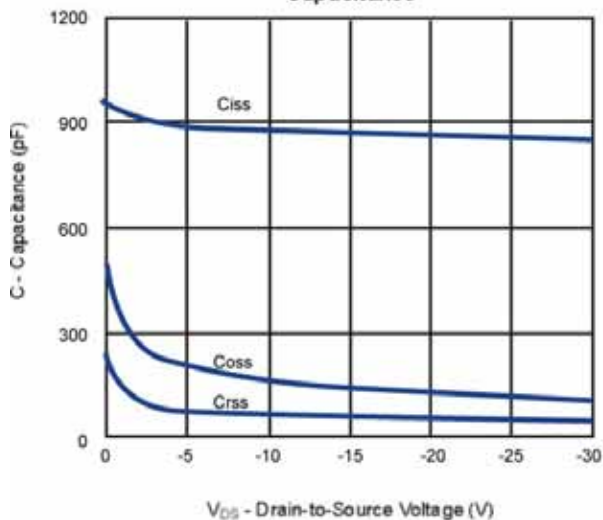
On Resistance vs. Junction Temperature



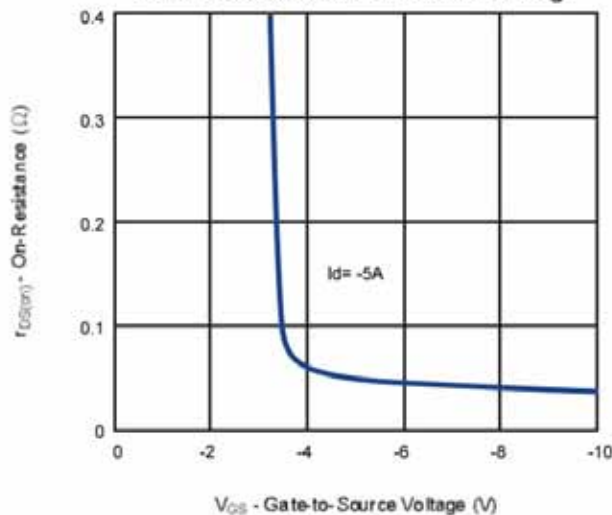
On-Resistance vs. Drain Current



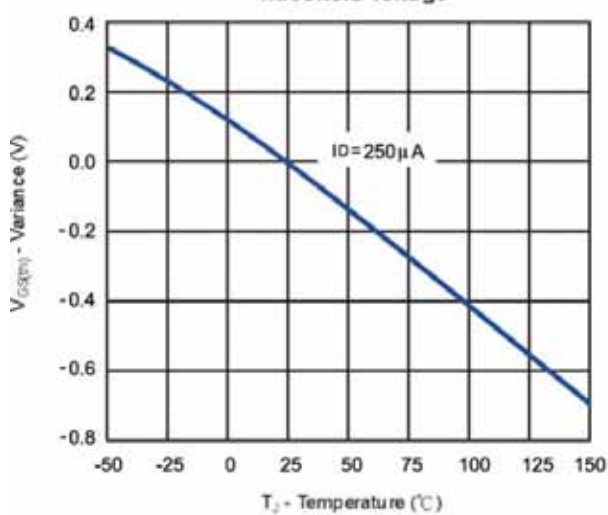
Capacitance



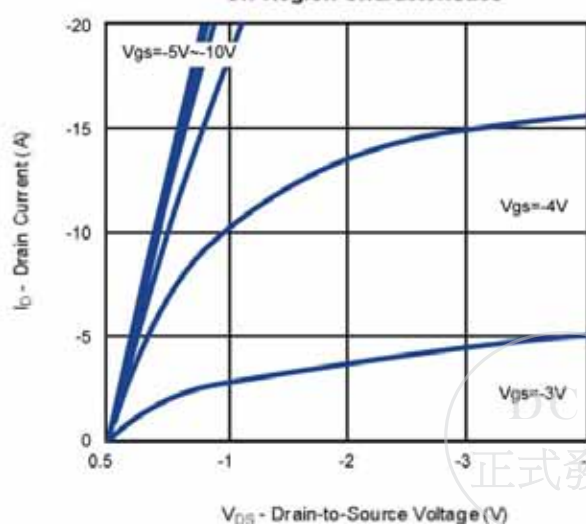
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

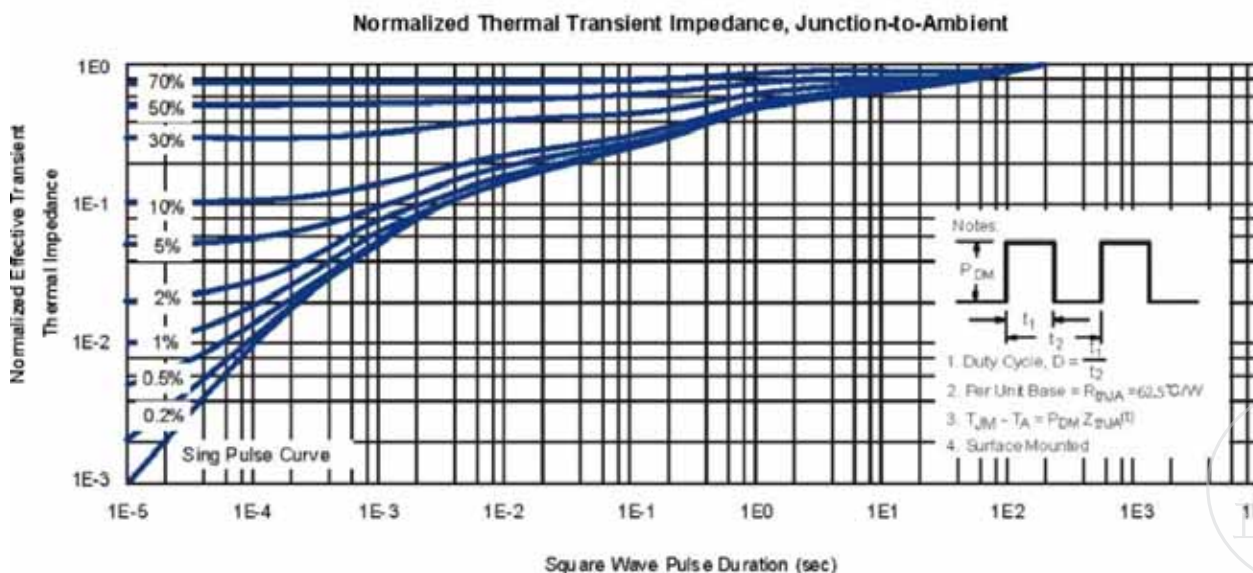
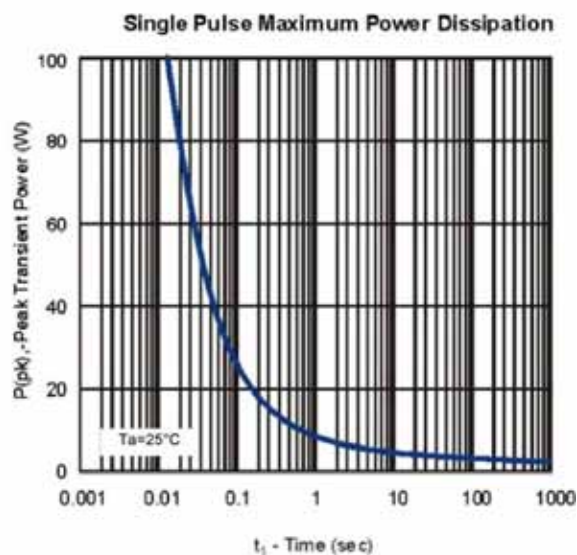
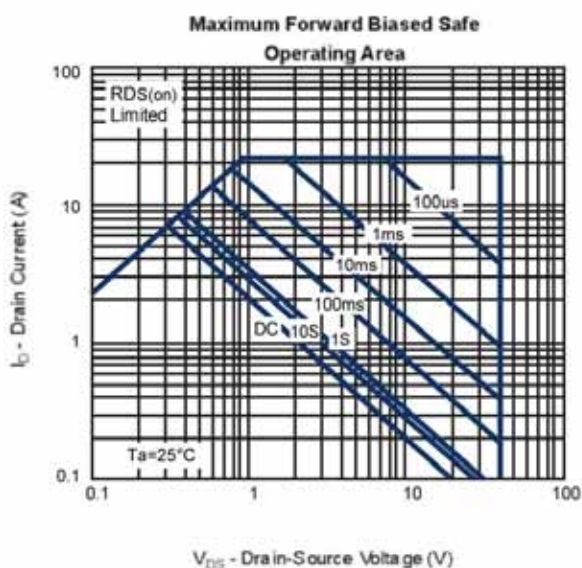
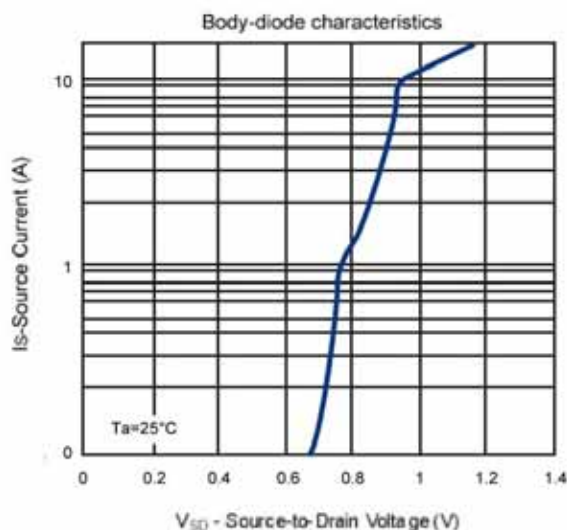
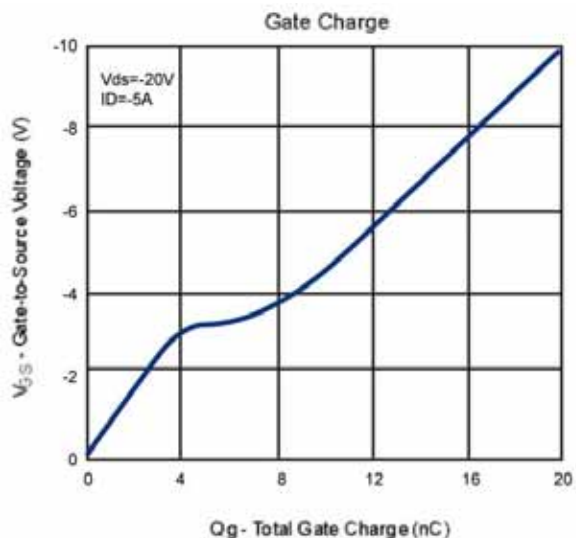


On-Region Characteristics



P Channel 40-V (D-S) MOSFET

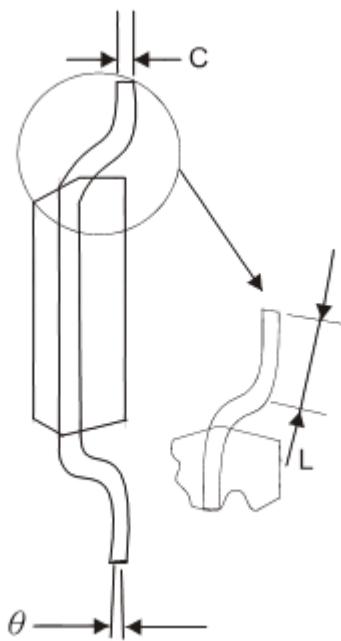
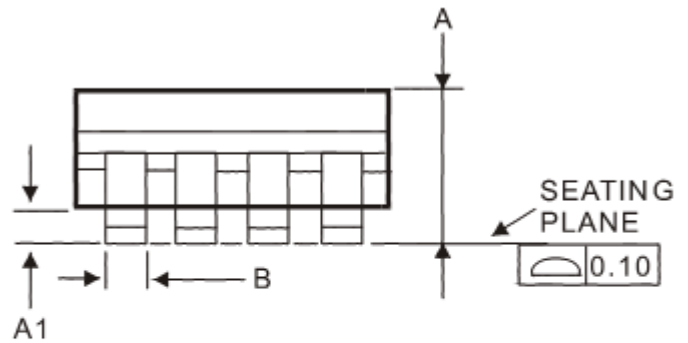
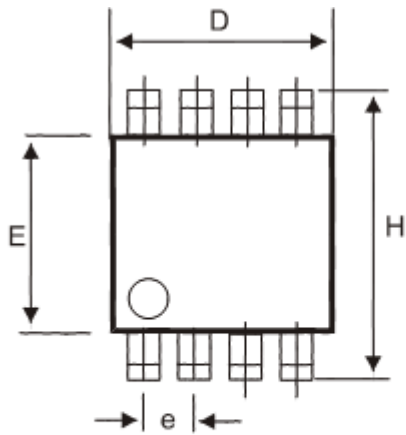
Typical Characteristics (T_J =25 Noted)



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SOP-8 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°



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