

Dual P-Channel 30V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4925 is the Dual P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

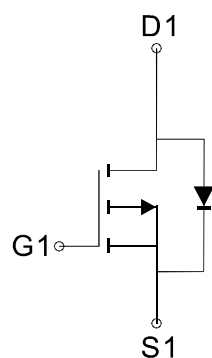
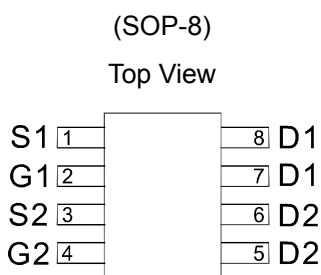
FEATURES

- $R_{DS(ON)} \leq 20m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 26m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

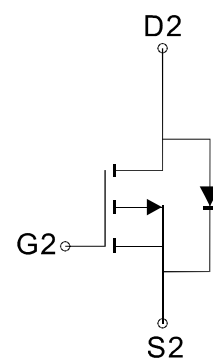
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION



P-Channel MOSFET



P-Channel MOSFET

Ordering Information: ME4925 (Pb-free)

ME4925-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_A = 25^\circ C$	-8
		$T_A = 70^\circ C$	-6.3
Pulsed Drain Current	I_{DM}	-32	A
Maximum Power Dissipation	P_D	$T_A = 25^\circ C$	2
		$T_A = 70^\circ C$	1.3
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ C/W$

*The device mounted on 1in² FR4 board with 2 oz copper



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Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{BR(DSS)}	Drain-source breakdown voltage	V _{GS} =0V, I _D =250 μA	-30			
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μA	-1		-3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V			-1	μA
R _{DS(ON)}	Drain-Source On-Resistance	V _{GS} =-10V, I _D = -7.1A		16	20	mΩ
		V _{GS} =-4.5V, I _D = -5.5A		21	26	
V _{SD}	Diode Forward Voltage	I _S =-1.7A, V _{GS} =0V		-0.7	-1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-10V, I _D =-9.1A		37		nC
Q _{gs}	Gate-Source Charge			5.6		
Q _{gd}	Gate-Drain Charge			8.7		
C _{iss}	Input capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz		1490		pF
C _{oss}	Output Capacitance			202		
C _{rss}	Reverse Transfer Capacitance			183		
R _g	Gate-Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		6.2		Ω
t _{d(on)}	Turn-On Delay Time	V _{DD} =-15V, R _L =15Ω I _D =-1.0A, V _{GEN} =-10V R _C =6Ω		39.1		ns
t _r	Turn-On Rise Time			16.9		
t _{d(off)}	Turn-Off Delay Time			107		
t _f	Turn-Off Fall Time			26.7		

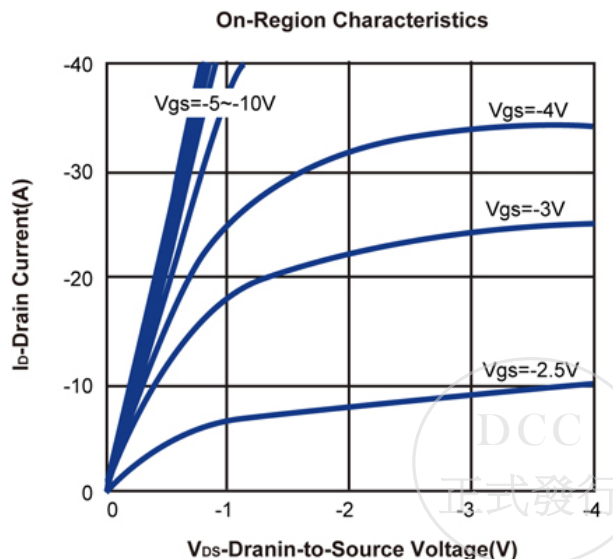
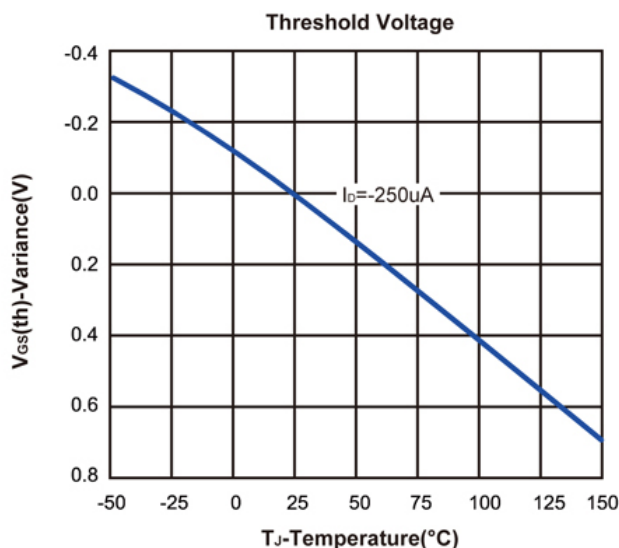
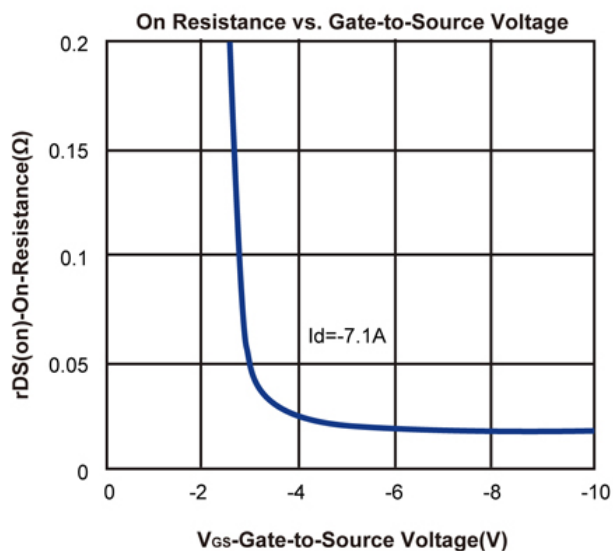
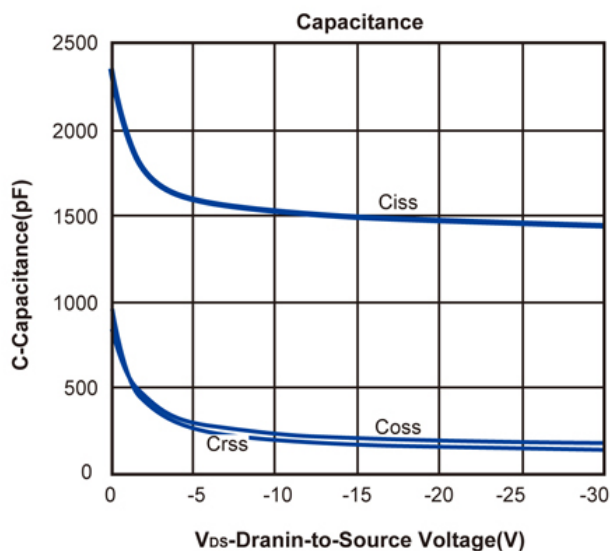
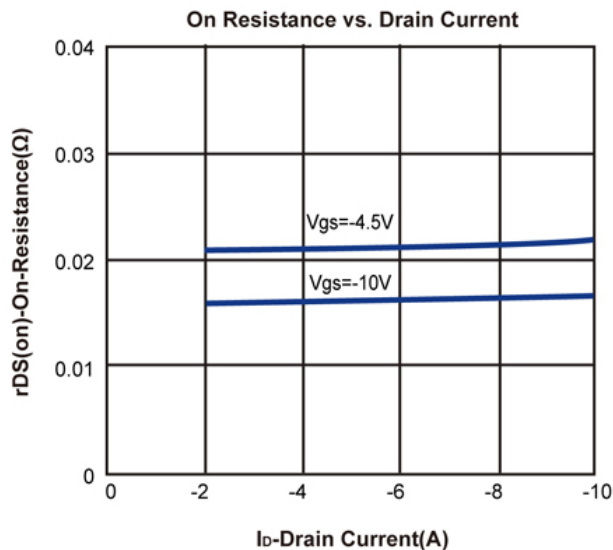
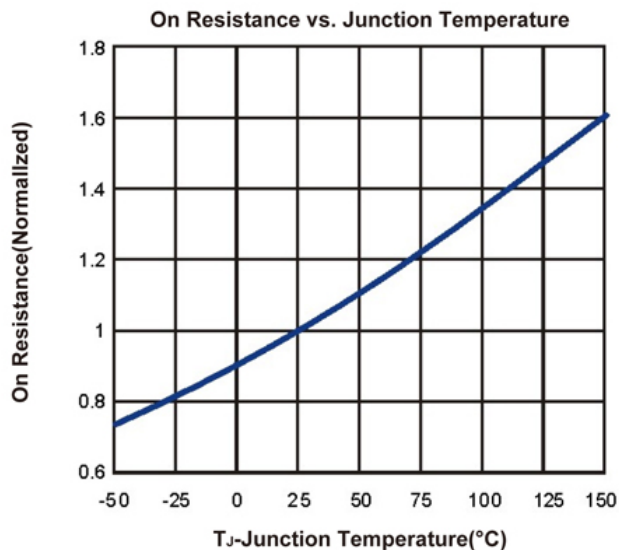
Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



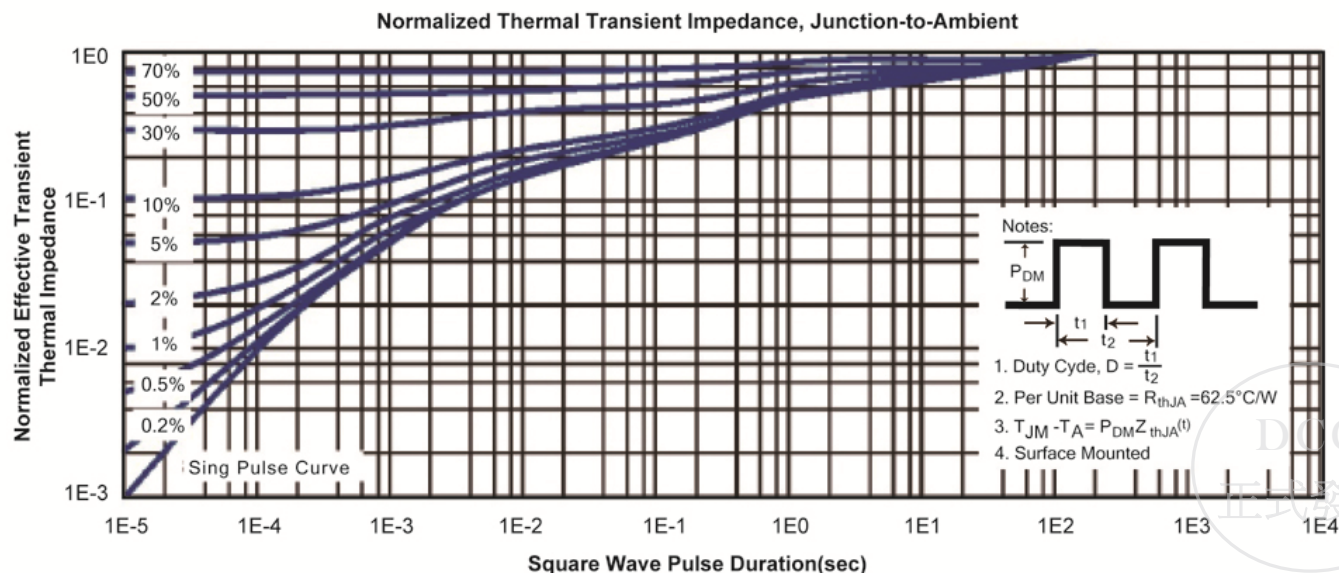
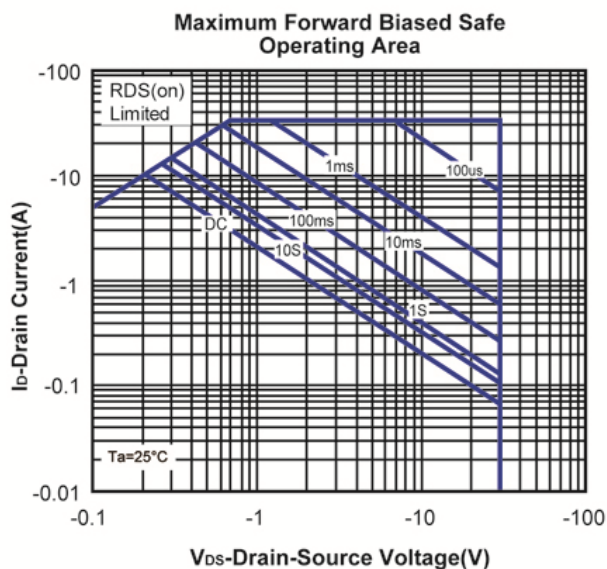
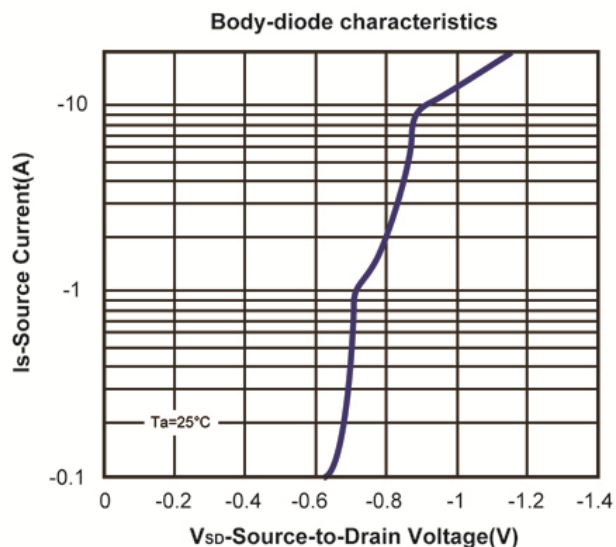
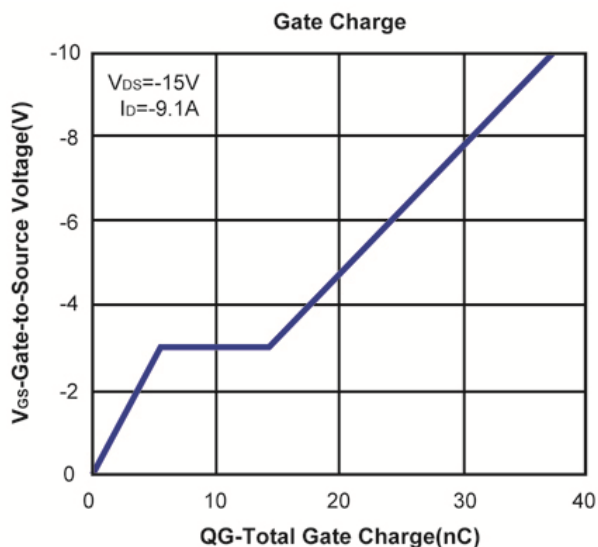
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Typical Characteristics (T_J = 25°C Noted)

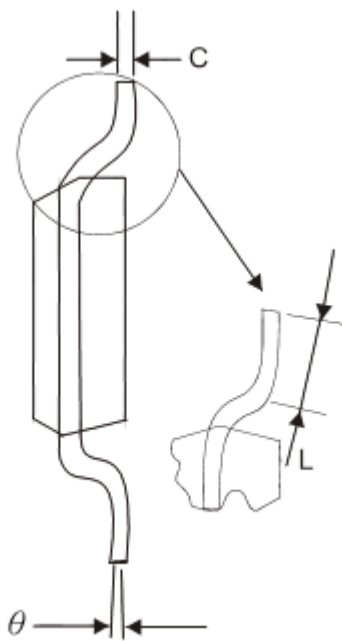
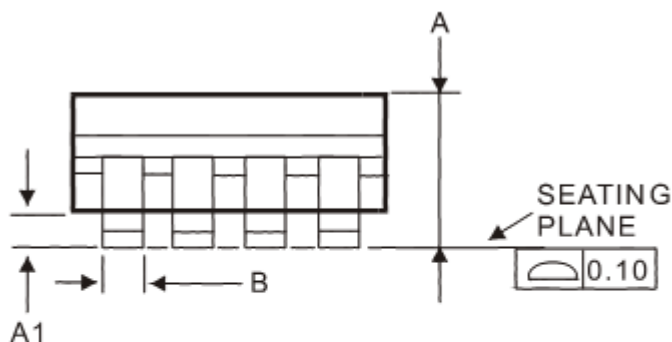
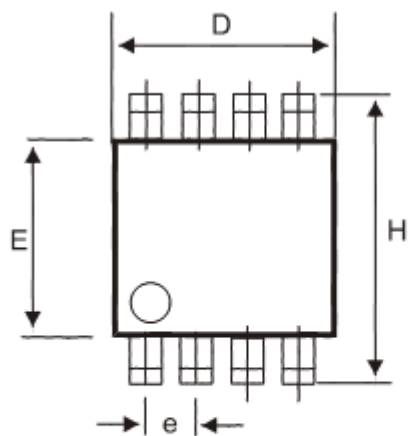


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SOP-8 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°



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