

**Dual N-Channel 60-V (D-S) MOSFET**

**GENERAL DESCRIPTION**

The ME4946 is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

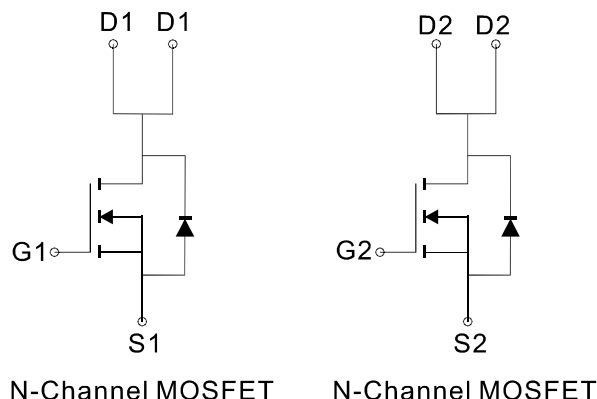
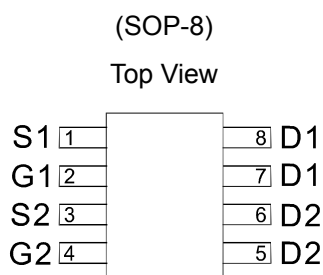
**FEATURES**

- $R_{DS(ON)} \leq 41m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 52m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

**APPLICATIONS**

- Power Management
- DC/DC Converter
- LCD TV & Monitor Display inverter
- CCFL inverter

**PIN CONFIGURATION**



Ordering Information: ME4946 (Pb-free)

ME4946-G (Green product-Halogen free)

**Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)**

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		$V_{DSS}$	60		V
Gate-Source Voltage		$V_{GSS}$	$\pm 20$		
Continuous Drain Current (Tj=150°C)	TA=25°C	$I_D$	6.4	5	A
	TA=70°C		5.1	4	
Pulsed Drain Current		$I_{DM}$	30		
Continuous Source-Drain Diode Current		$I_S$	2		
Avalanche Current	L=0.1mH	$I_{AS}$	15		mJ
Single-Pulse Avalanche Energy		$E_{AS}$	12		
Maximum Power Dissipation	TA=25°C	$P_D$	2.7	1.6	W
	TA=70°C		1.7	1	
Operating Junction & Storage Temperature Range		$T_J$	-55 to 150		°C
Thermal Resistance-Junction to Ambient *		$R_{\theta JA}$	46	76	°C/W
Thermal Resistance-Junction to Case *		$R_{\theta JC}$	43		

\*The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper

## Dual N-Channel 60-V (D-S) MOSFET

Electrical Characteristics (T<sub>A</sub> = 25°C Unless Otherwise Specified)

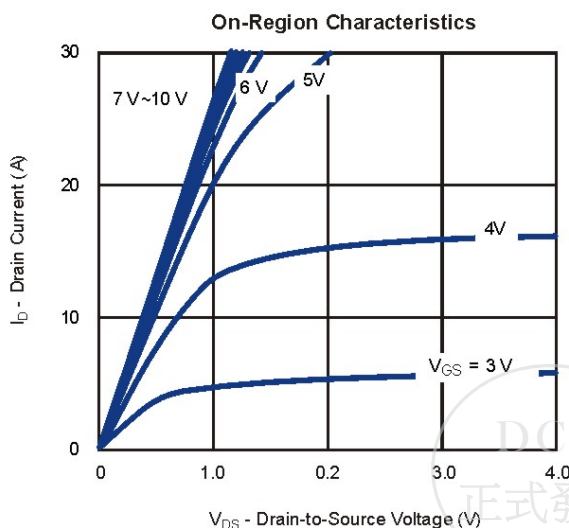
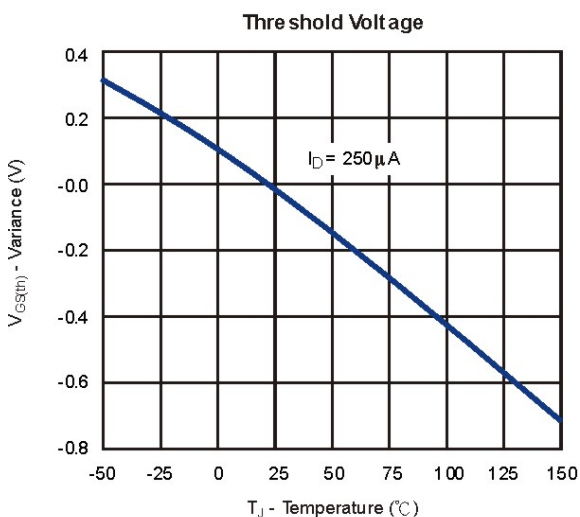
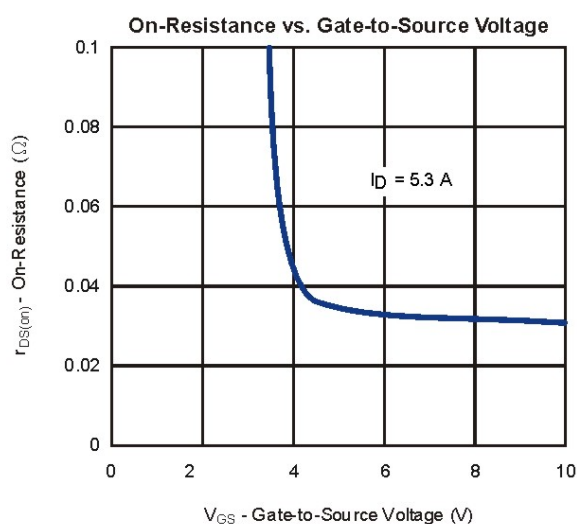
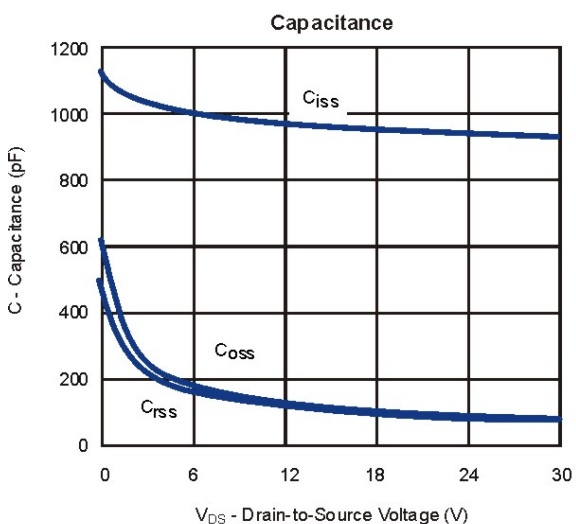
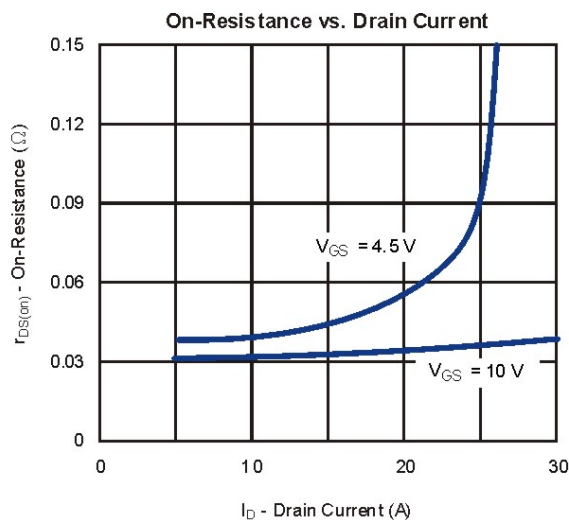
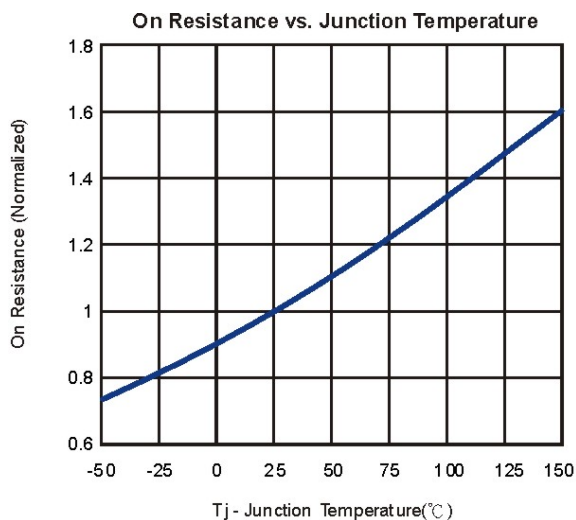
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>STATIC</b>						
V <sub>DS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250 μA	60			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 μA	1.0	1.8	3.0	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			1	μA
		V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			10	
		T <sub>J</sub> =55°C				
R <sub>DS(ON)</sub>	Drain-Source On-Resistance <sup>a</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> = 5.3A		33	41	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> = 4.7A		40	52	
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =2A		0.8	1.2	V
<b>DYNAMIC</b>						
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, f=1.0MHz		940	1100	pF
C <sub>oss</sub>	Output Capacitance			71		
C <sub>rss</sub>	Reverse Transfer Capacitance			33		
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =30V, V <sub>GS</sub> =10V, I <sub>D</sub> =5.3A		22	29	nC
				13.3	18	
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =30V, V <sub>GS</sub> =5V, I <sub>D</sub> =5.3A		7.1		
Q <sub>gd</sub>	Gate-Drain Charge			7.5		
R <sub>g</sub>	Gate Resistance	f=1MHz		0.9		Ω
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =30V, R <sub>L</sub> =6.8Ω I <sub>D</sub> =4.4A, V <sub>GEN</sub> =10V R <sub>G</sub> =1Ω		14	18	ns
t <sub>r</sub>	Turn-On Rise Time			26	33	
t <sub>d(off)</sub>	Turn-Off Delay Time			41	52	
t <sub>f</sub>	Turn-Off Fall Time			3.6	6	
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =30V, R <sub>L</sub> =6.8Ω I <sub>D</sub> =4.4A, V <sub>GEN</sub> =4.5V R <sub>G</sub> =1Ω		12	16	
t <sub>r</sub>	Turn-On Rise Time			26	33	
t <sub>d(off)</sub>	Turn-Off Delay Time			42	52	
t <sub>f</sub>	Turn-Off Fall Time			3.8	7	

Notes: a. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

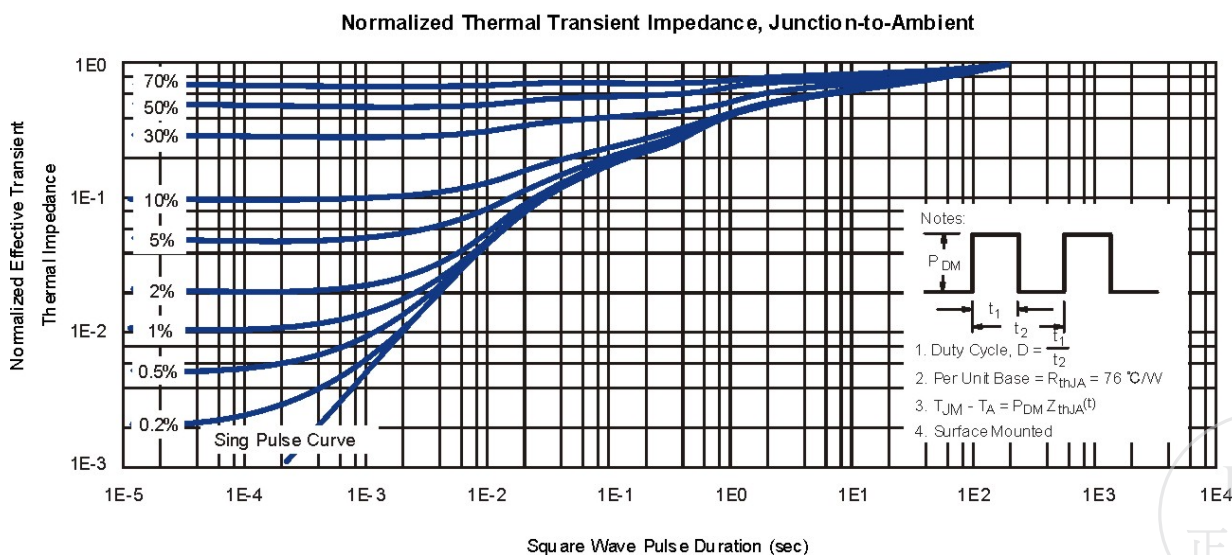
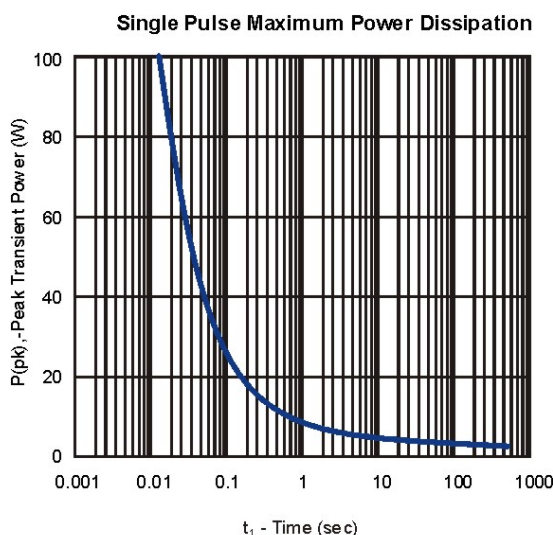
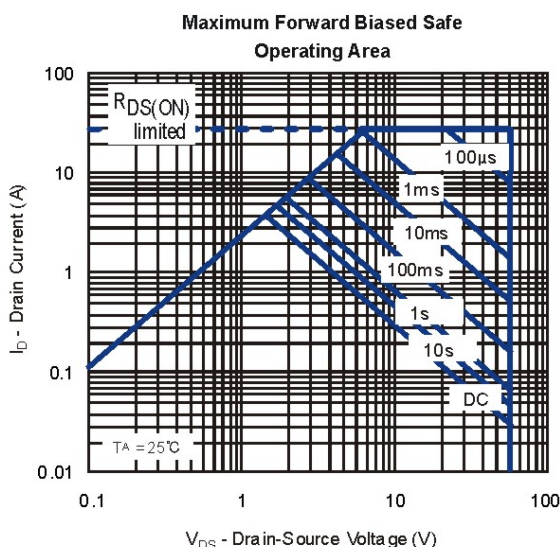
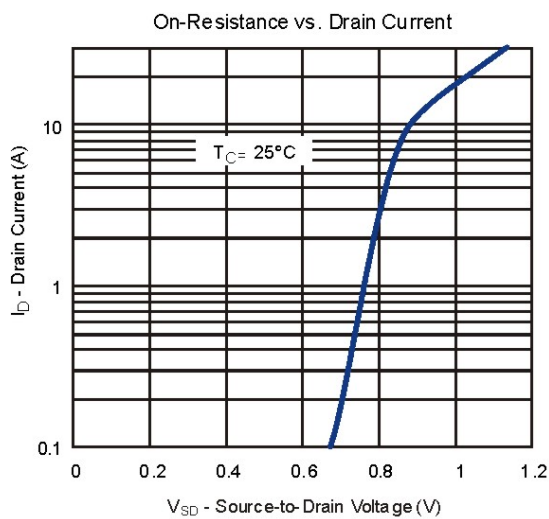
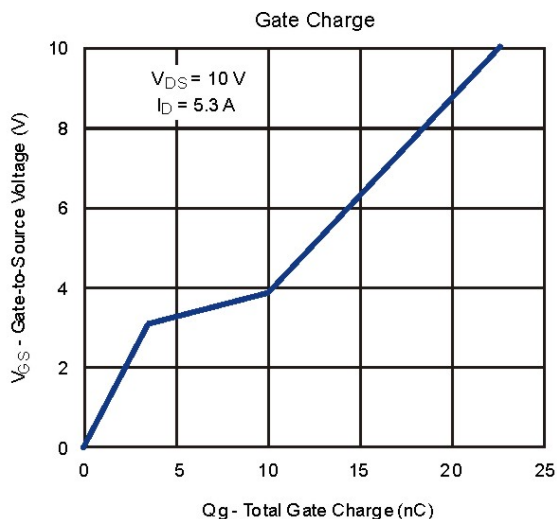


Typical Characteristics (T<sub>J</sub> = 25°C Noted)

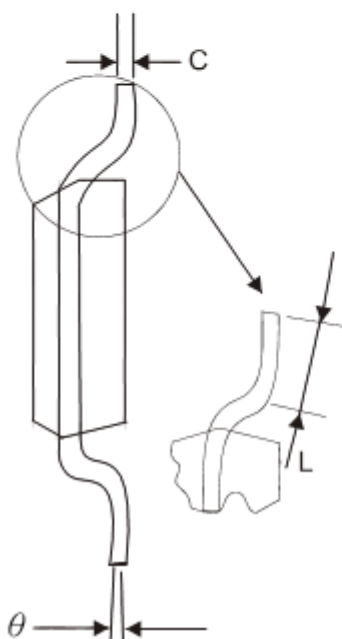
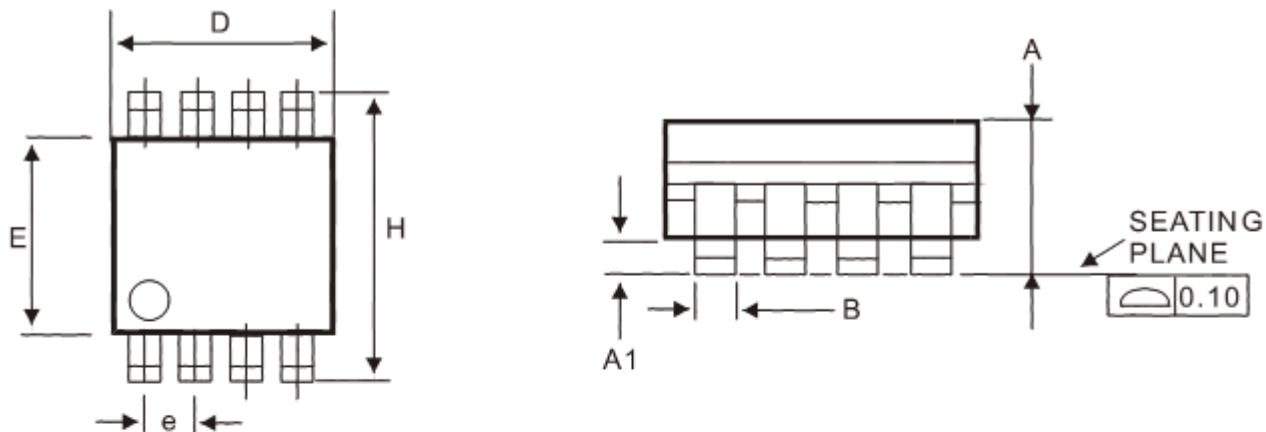


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Typical Characteristics (T<sub>J</sub> = 25°C Noted)



**SOP-8 Package Outline**



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
$\theta$	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.



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