

Dual P-Channel 30V (D-S) MOSFET
GENERAL DESCRIPTION

The ME4953 is the Dual P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

R_{DS(ON)} 60mΩ@V_{GS}=-10V

R_{DS(ON)} 90mΩ@V_{GS}=-4.5V

Super high density cell design for extremely low R_{DS(ON)}

Exceptional on-resistance and maximum DC current capability

APPLICATIONS

Power Management in Note book

Portable Equipment

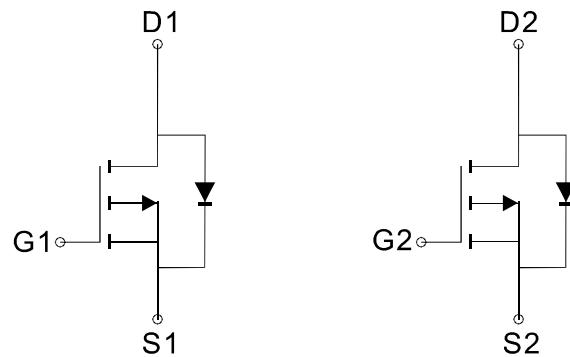
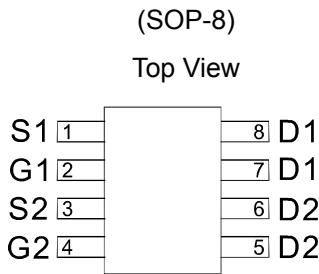
Battery Powered System

DC/DC Converter

Load Switch

DSC

LCD Display inverter

PIN CONFIGURATION


Ordering Information: ME4953 (Pb-free)

ME4953-G (Green product-Halogen free)

P-Channel MOSFET

P-Channel MOSFET

Absolute Maximum Ratings (TA=25 Unless Otherwise Noted)

Parameter	Symbol	Limit		Unit
Drain-Source Voltage	V _{DSS}	-30		V
Gate-Source Voltage	V _{GSS}	±20		V
Continuous Drain Current (T _j =150)	I _D	-5.3		A
T _A =70		-4.3		
Pulsed Drain Current	I _{DM}	-30		A
Continuous Source Current (Diode Conduction)	I _S	-1.7		A
Maximum Power Dissipation T _A =25	P _D	2.0		W
T _A =70		1.3		
Operating Junction Temperature	T _J	-55 to 150		
Storage Temperature Range	T _{Stg}	-55 to 150		
Thermal Resistance-Junction to Ambient*	R _{θJA}	T 10 sec	47	/W
Steady State		Steady State	75	
Thermal Resistance-Junction to Case	R _{θJC}	45		/W

*The device mounted on 1in² FR4 board with 2 oz copper

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Dual P-Channel 30V (D-S) MOSFET
Electrical Characteristics (TA=25 Unless Otherwise Specified)

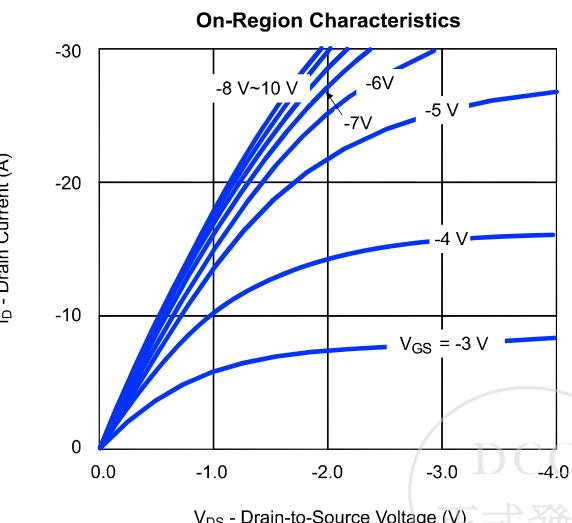
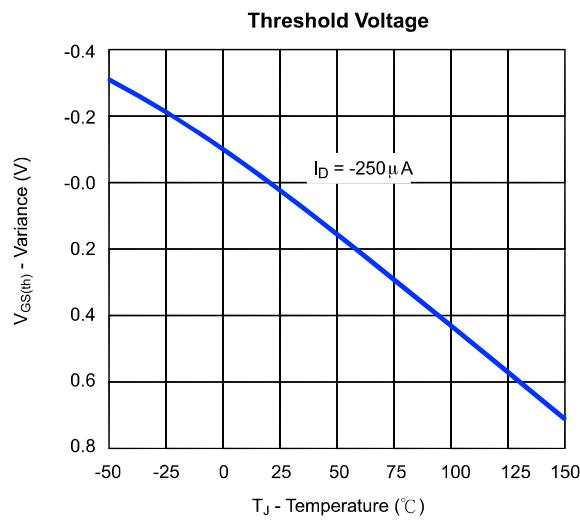
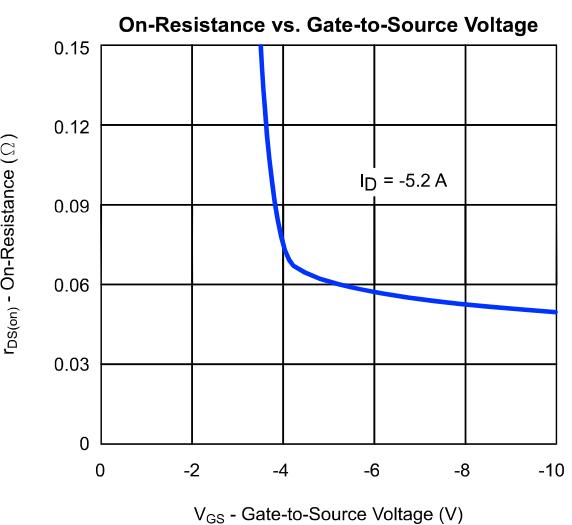
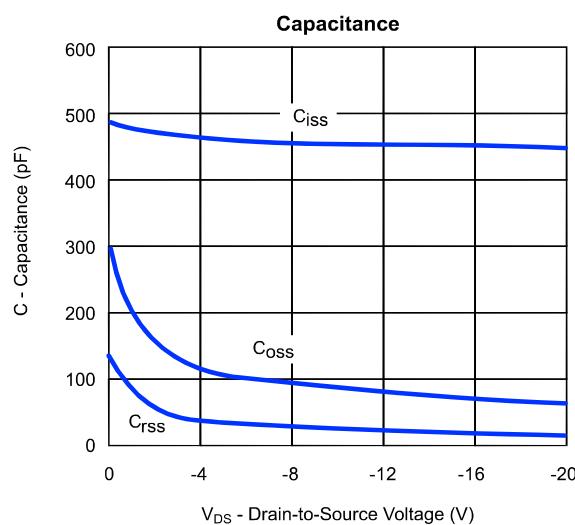
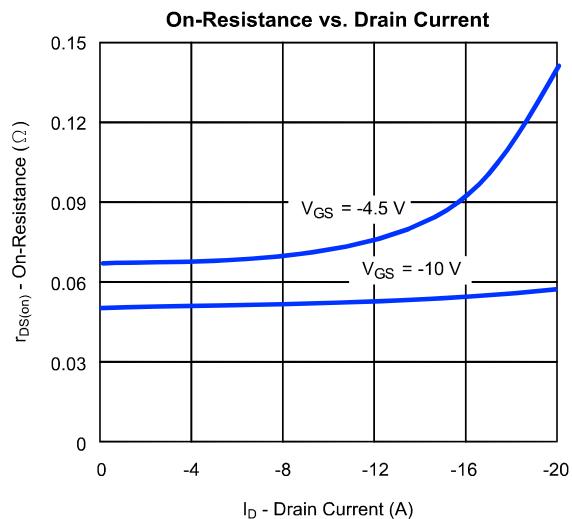
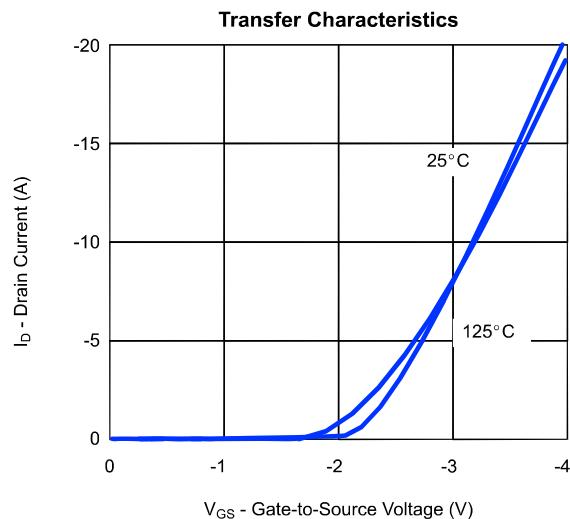
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μA	-1	-1.4	-3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V			-1	μA
		V _{DS} =-30V, V _{GS} =0V T _J =55			-25	
R _{DSON}	Drain-Source On-Resistance	V _{GS} =-10V, I _D = -5.3A		50	60	m
		V _{GS} =-4.5V, I _D = -4.2A		69	90	
V _{SD}	Diode Forward Voltage	I _S =-1.7A, V _{GS} =0V		-0.8	-1.2	V
DYNAMIC						
R _G	Gate resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		3.5		Ω
C _{ISS}	Input capacitance	V _{DS} =-15V, V _{GS} =0V, f=1.0MHz		450	490	pF
C _{OSS}	Output Capacitance			70		
C _{rss}	Reverse Transfer Capacitance			20		
Q _G	Total Gate Charge	V _{DS} =-15V, V _{GS} =-10V, I _D =-5.3A		14	17	nC
Q _{GS}	Gate-Source Charge			4		
Q _{GD}	Gate-Drain Charge			3		
t _{d(on)}	Turn-On Delay Time	V _{DD} =-15V, R _L =15Ω I _D =-1.0A, V _{GEN} =-10V R _G =6Ω		27	33	ns
t _r	Turn-On Rise Time			11	15	
t _{d(off)}	Turn-Off Delay Time			40	52	
t _f	Turn-Off Fall Time			4	6	

Notes: a. Pulse test; pulse width 300us, duty cycle 2%



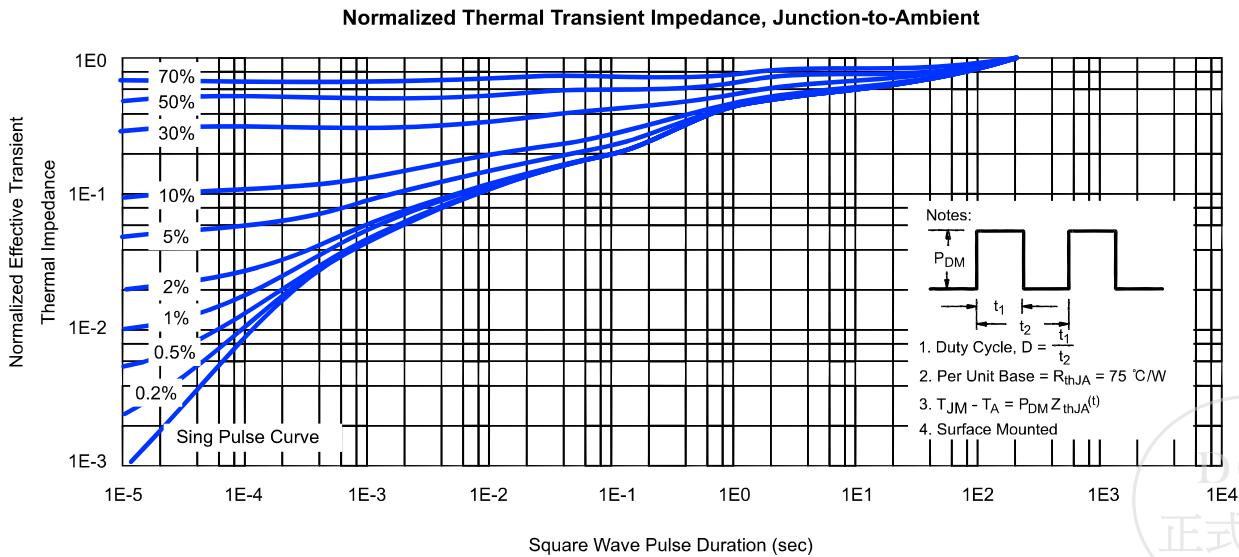
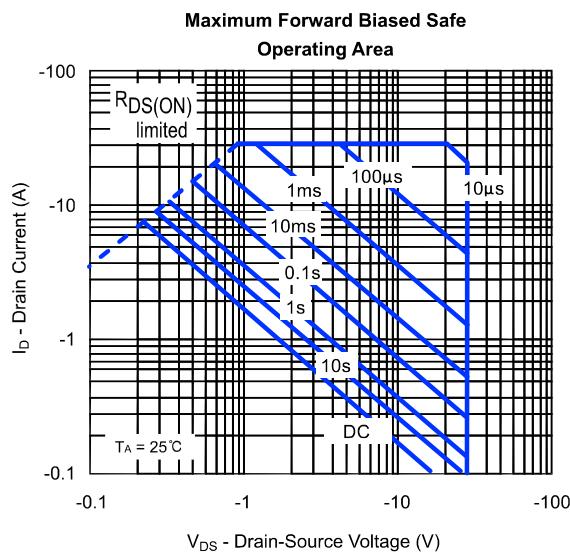
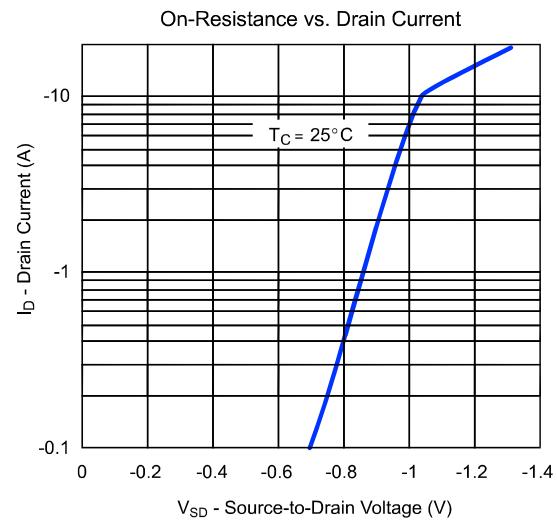
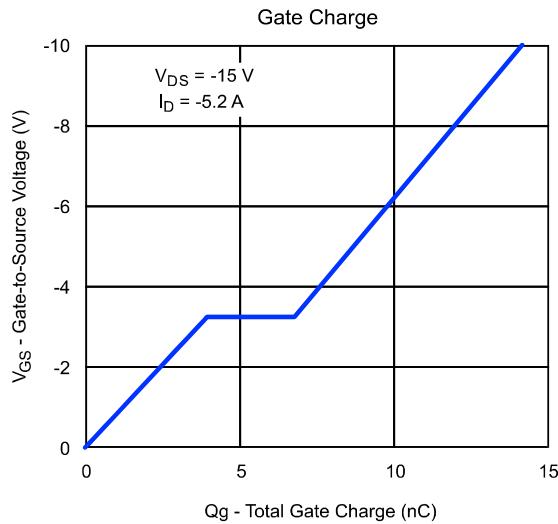
Dual P-Channel 30V (D-S) MOSFET

Typical Characteristics (T_J =25 Noted)

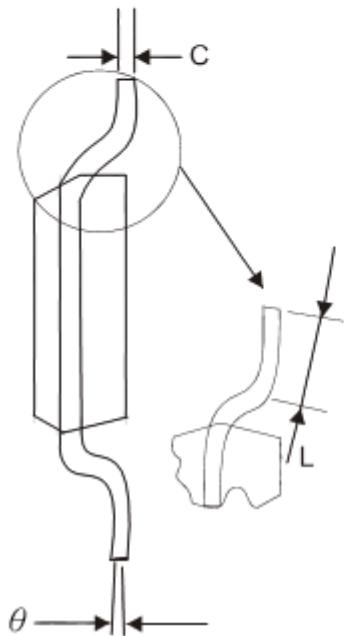
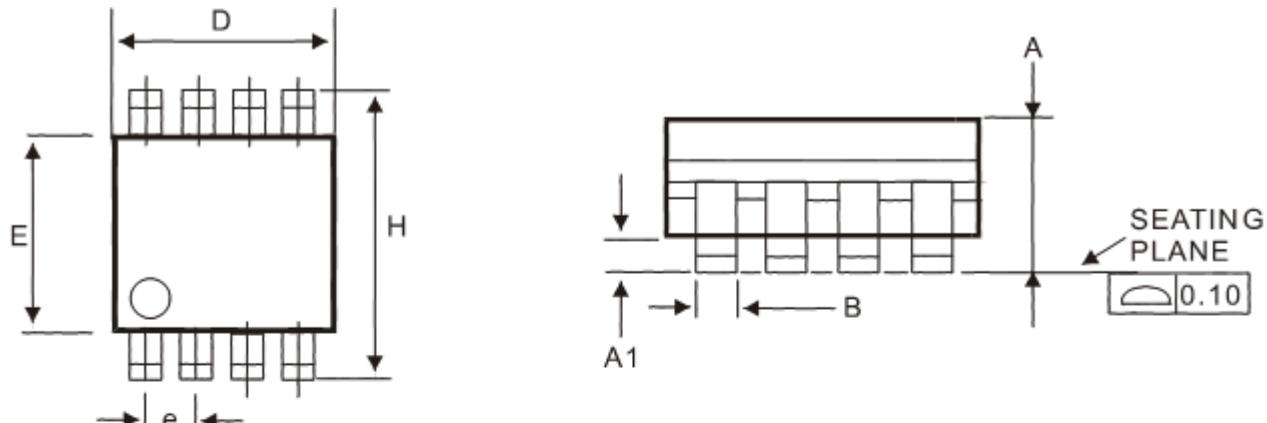


Dual P-Channel 30V (D-S) MOSFET

Typical Characteristics (T_J =25 °C Noted)



SOP-8 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.



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