ME4954/ME4954-G

Dual N- Channel 100V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4954 is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 80m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 98m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

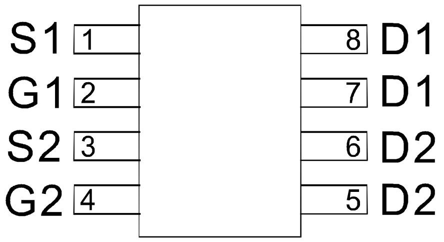
APPLICATIONS

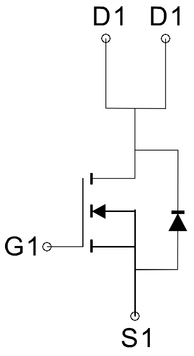
- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

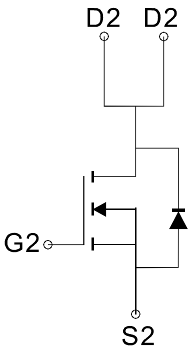
(SOP-8)

Top View





N-Channel MOSFET



N-Channel MOSFET

Ordering Information: ME4954 (Pb-free)

ME4954-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current*	T_A=25℃	I_D	4	A
	T_A=70℃		3.2	
Pulsed Drain Current		I_{DM}	16	A
Maximum Power Dissipation*	T_A=25℃	P_D	2	W
	T_A=70℃		1.3	
Operating Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	62.5	℃/W

*The device mounted on $1in^2$ FR4 board with 2 oz copper

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Electrical Characteristics (T$_A$ =25℃ Unless Otherwise Specified)

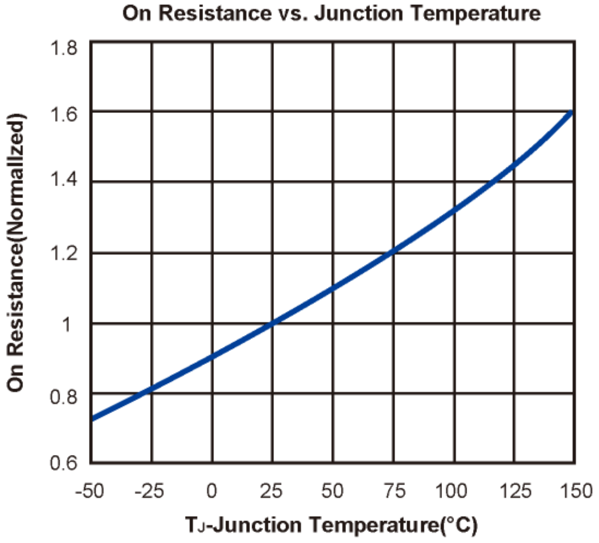
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		2.5	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=80V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D= 4A		65	80	mΩ
		V_{GS}=4.5V, I_D= 3.2A		75	98	
V_{SD}	Diode Forward Voltage	I_S=12A, V_{GS}=0V			1.3	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=80V, V_{GS}=10V, I_D=4A		28.8		nC
Qg	Total Gate Charge	V_{DS}=80V, V_{GS}=5V, I_D=4A		17.4		
Qgs	Gate-Source Charge			9.9		
Qgd	Gate-Drain Charge			5.6		
Ciss	Input capacitance	V_{DS}=20V, V_{GS}=0V, F=1MHz		1106		pF
Coss	Output Capacitance			73		
Crss	Reverse Transfer Capacitance			46		
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		2		Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=50V, R_L =12.5Ω V_{GEN}=5V, R_G=4.7Ω I_D=4A		27.3		ns
t_r	Turn-On Rise Time			89.9		
$t_{d(off)}$	Turn-Off Delay Time			36.8		
t_f	Turn-Off Fall Time			11		

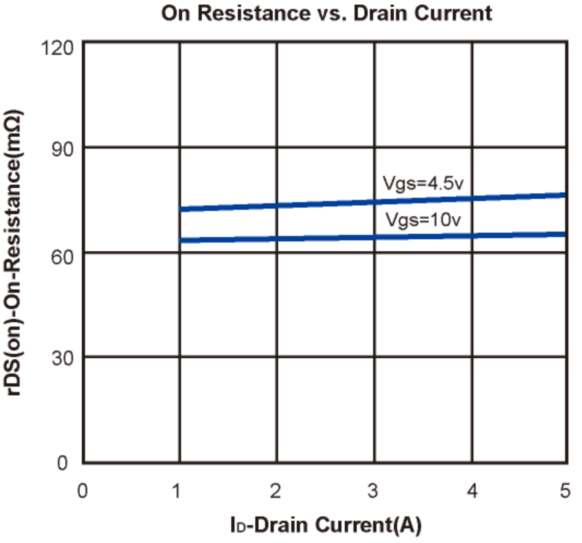
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

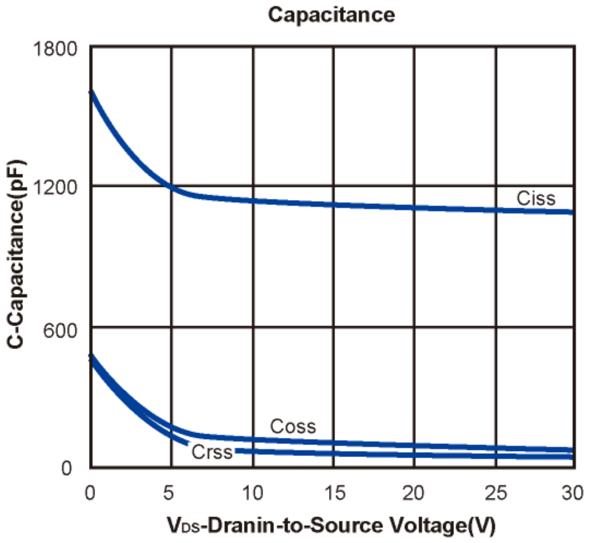
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

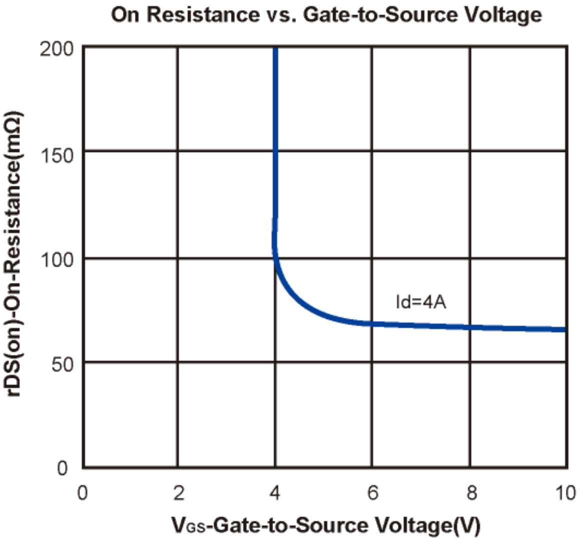
Dual N- Channel 100V (D-S) MOSFET

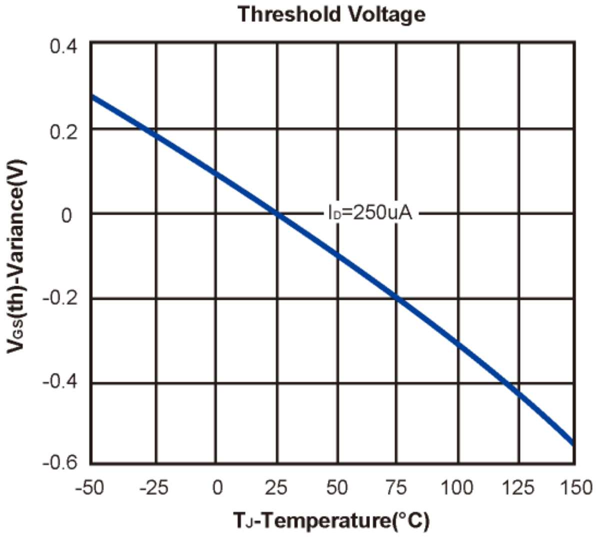
Typical Characteristics (T_J =25℃ Noted)

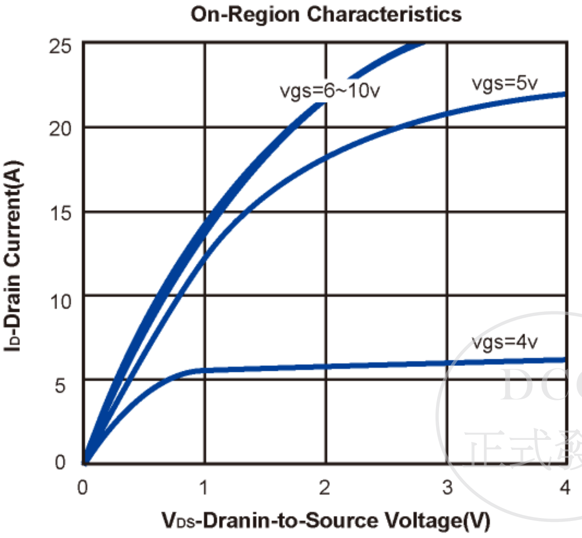












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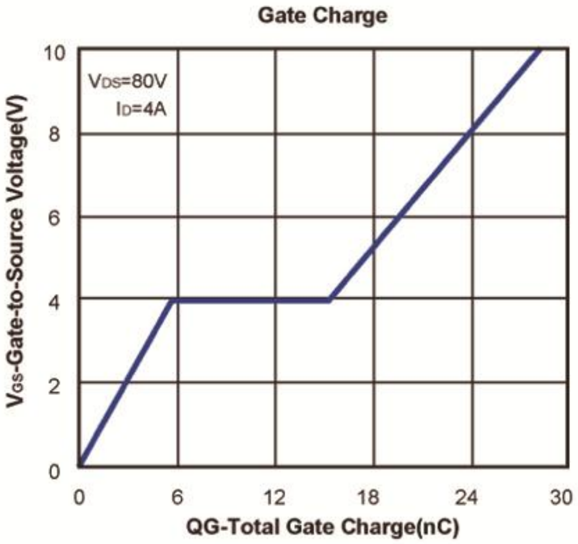
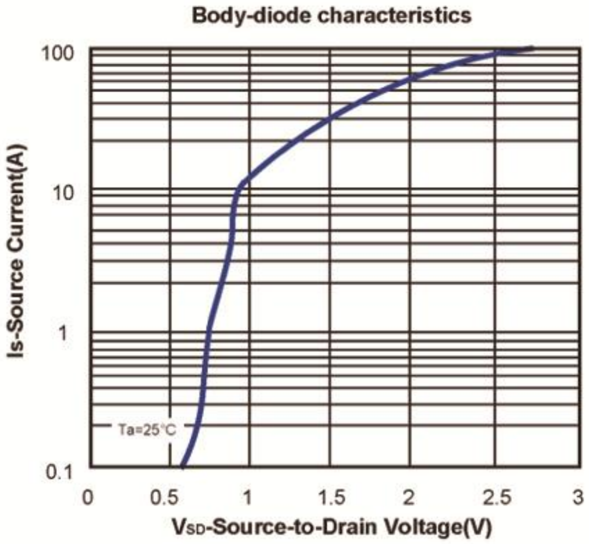
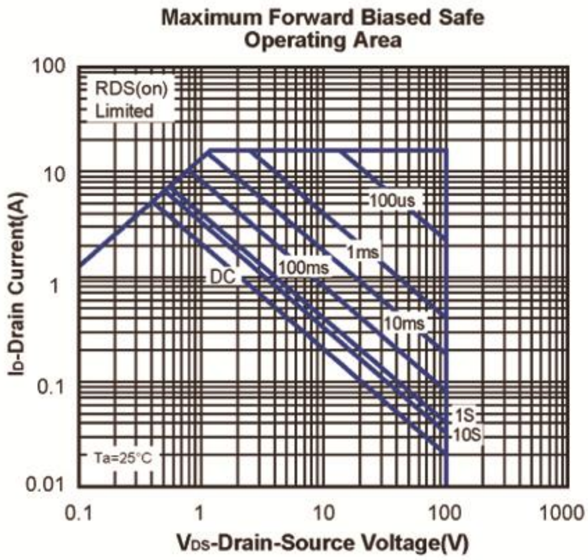
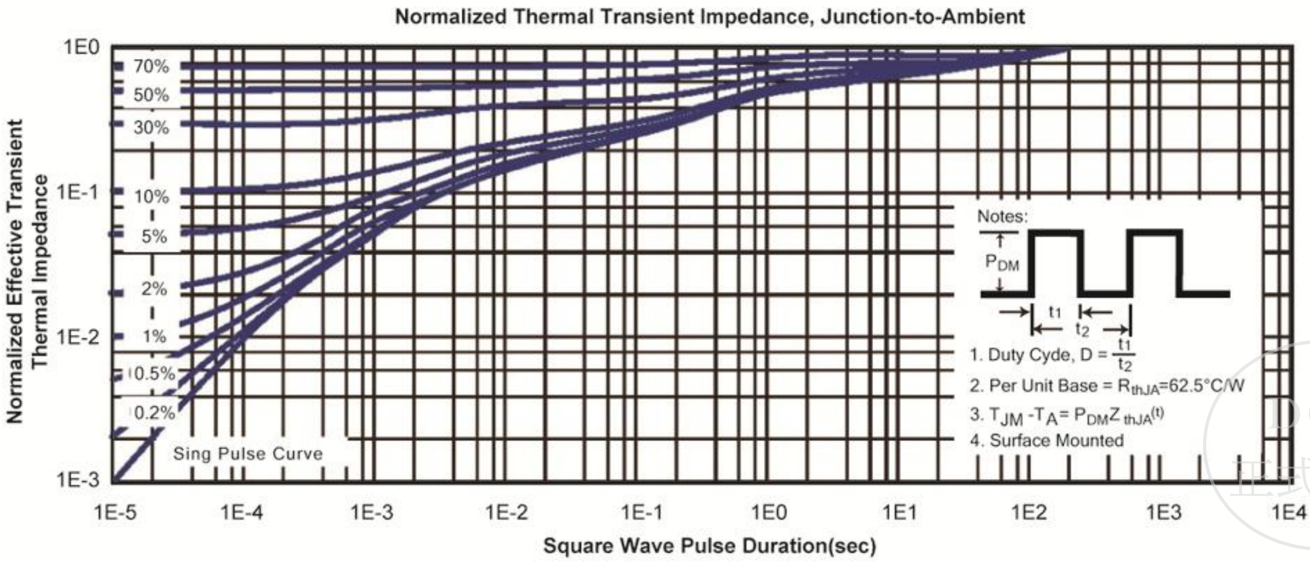

Gate Charge


Body-diode characteristics

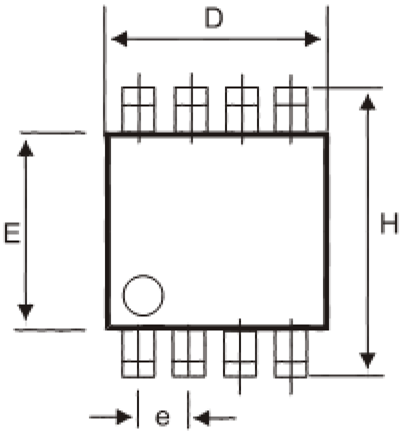

Maximum Forward Biased Safe Operating Area

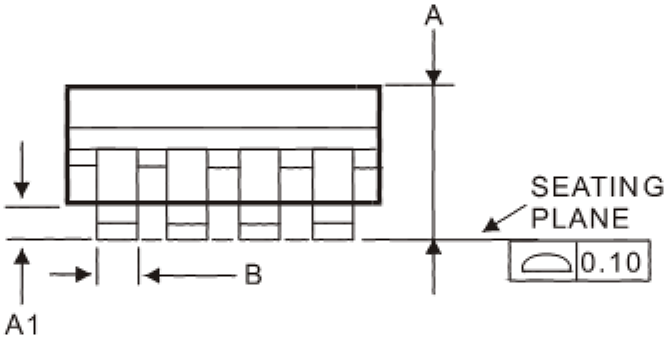

Normalized Thermal Transient Impedance, Junction-to-Ambient

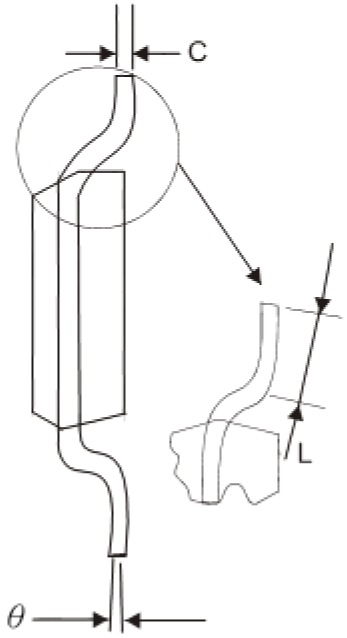
Notes:

1. Duty Cyde, D = $\frac{t_1}{t_2}$
2. Per Unit Base = R_{thJA}=62.5°C/W
3. T_{JM} -T_A= $P_{DM}Z_{thJA}(t)$
4. Surface Mounted

SOP-8 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension “D” does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.