

## 25V N-Channel Enhancement Mode MOSFET

$V_{DS}=25V$

$R_{DS(ON)}, V_{GS}@10V, I_{DS}@30A \leq 9m\Omega$

$R_{DS(ON)}, V_{GS}@5V, I_{DS}@15A \leq 18m\Omega$

### FEATURES

Advanced trench process technology

High density cell design for ultra low on-resistance

Specially designed for DC/DC converters and motor drivers

Fully characterized avalanche voltage and current

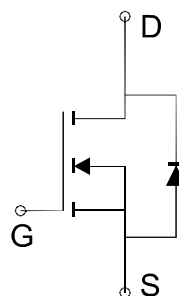
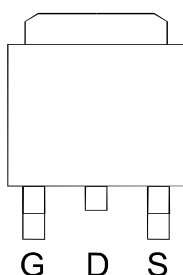
### APPLICATIONS

- Motherboard (V-Core)
- DC/DC Converter
- Load Switch
- LCD Display inverter
- IPC

### PIN CONFIGURATION

(TO-252-3L)

Top View



**Ordering Information:** ME60N03AS (Pb-free)

ME60N03AS-G (Green product-Halogen free)

### Absolute Maximum Ratings ( $T_A=25^\circ C$ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DSS}$	25	V
Gate-Source Voltage		$V_{GSS}$	$\pm 20$	V
Continuous Drain Current( $T_J=150^\circ C$ )*	$T_C=25^\circ C$	$I_D$	53	A
Pulsed Drain Current		$I_{DM}$	100	A
Maximum Power Dissipation	$T_C=25^\circ C$	$P_D$	40	W
	$T_C=70^\circ C$		25	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 150	$^\circ C$
Avalanche Energy with Single Pulse( $L=0.1mH, R_g=25\Omega$ )		$E_{AS}$	50	mJ
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	$T \leq 10$ sec	15	$^\circ C/W$
		Steady State	40	
Thermal Resistance-Junction to Case		$R_{\theta JC}$	3.1	$^\circ C/W$

\*The device mounted on  $1in^2$  FR4 board with 2 oz copper

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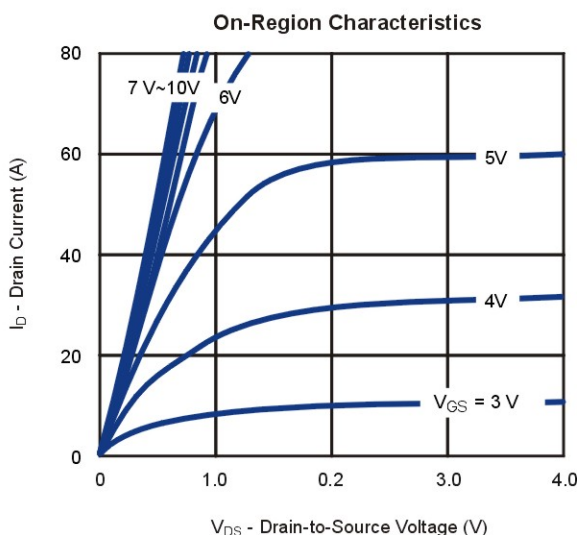
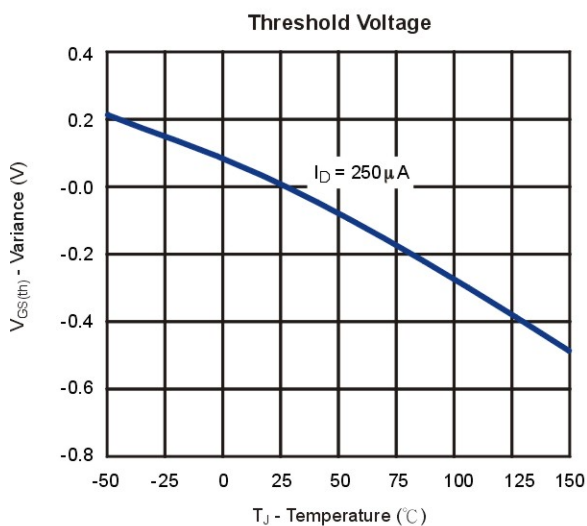
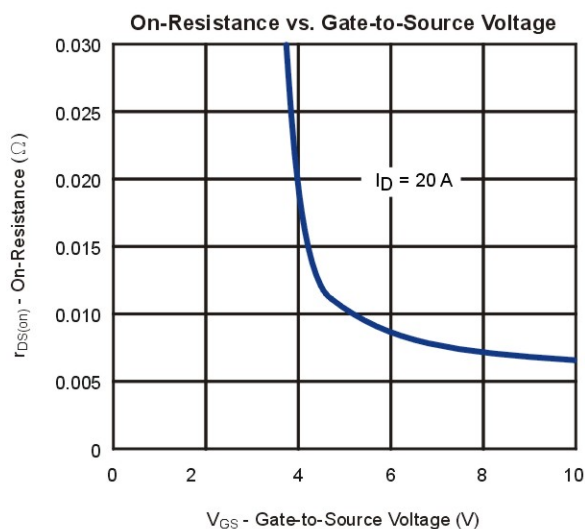
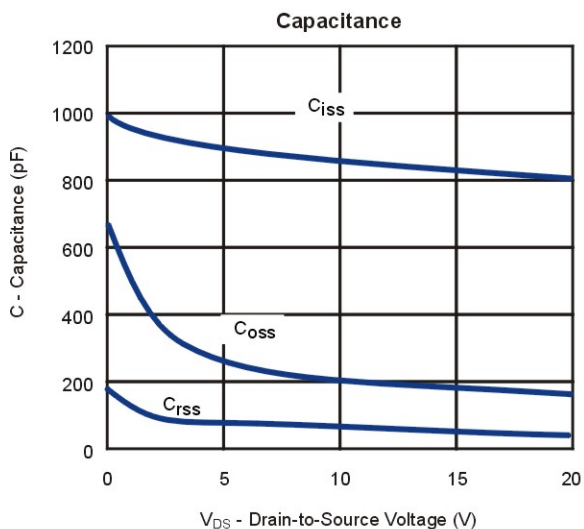
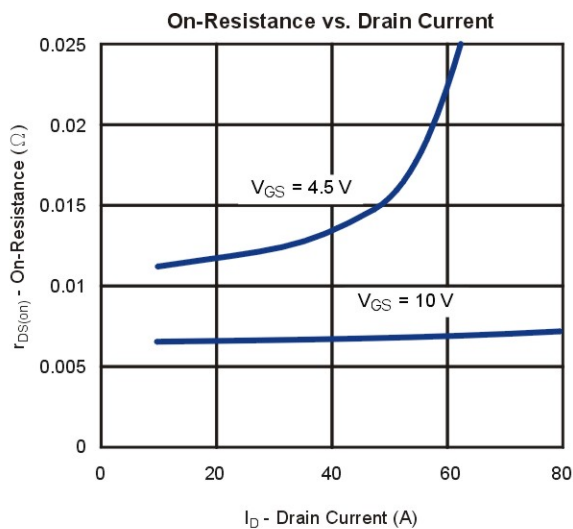
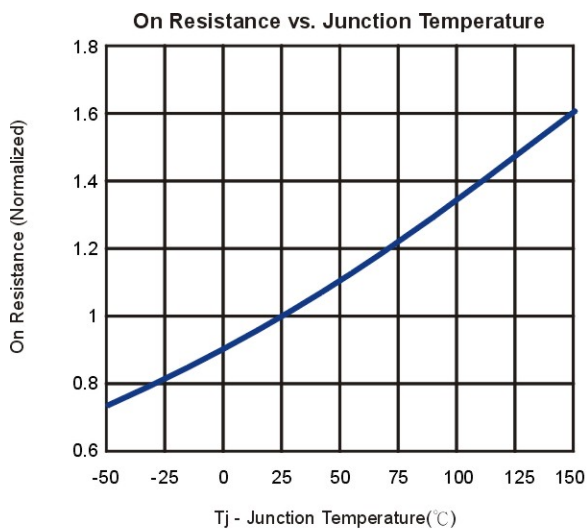
Electrical Characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250 μA	25			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 μA	1		3	V
I <sub>GSS</sub>	Gate-Body Leakage	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V			1	μA
R <sub>DS(ON)</sub>	Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =30A		6.7	9	mΩ
		V <sub>GS</sub> = 5V, I <sub>D</sub> =15A		13	18	
<b>DYNAMIC</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =15V, V <sub>GS</sub> =10V, I <sub>D</sub> =25A		22		nC
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =15V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =25A		11		
Q <sub>gs</sub>	Gate-Source Charge			5.4		
Q <sub>gd</sub>	Gate-Drain Charge			5.5		
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz		840		pF
C <sub>oss</sub>	Output Capacitance			180		
C <sub>rss</sub>	Reverse Transfer Capacitance			55		
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz		1		Ω
t <sub>d(on)</sub>	Turn-On Delay Time	R <sub>L</sub> =15Ω, V <sub>GEN</sub> =10V, I <sub>D</sub> =1A V <sub>DD</sub> =15V, R <sub>G</sub> =3Ω		13.5		ns
t <sub>r</sub>	Turn-On Rise Time			13		
t <sub>d(off)</sub>	Turn-Off Delay Time			42		
t <sub>f</sub>	Turn-Off Fall Time			4		
<b>SOURCE-DRAIN DIODE</b>						
I <sub>s</sub>	Max.Diode Forward Current				20	A
V <sub>SD</sub>	Diode Forward Voltage	I <sub>s</sub> =20A, V <sub>GS</sub> =0V		0.87	1.5	V

Note: Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%

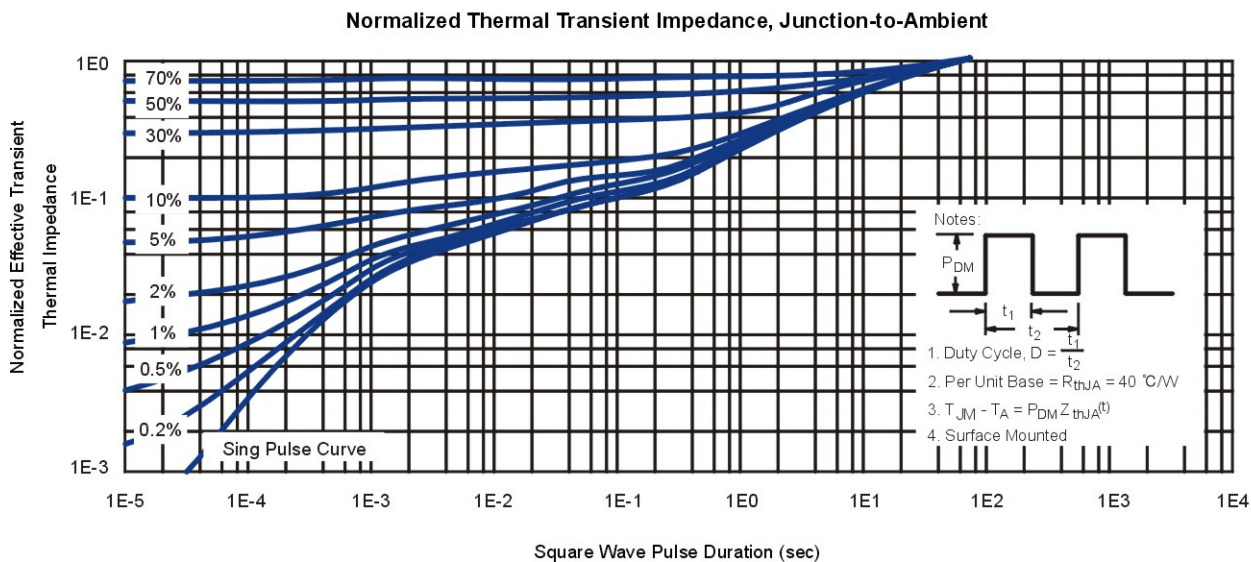
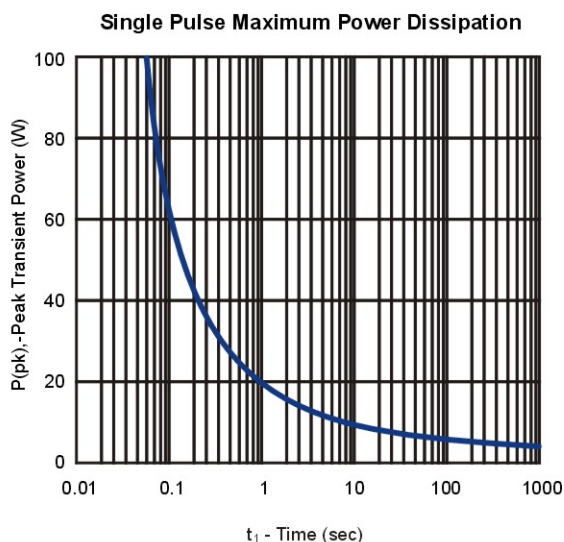
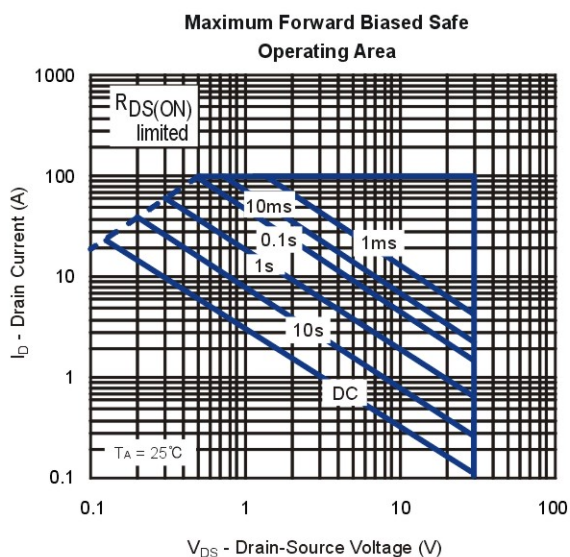
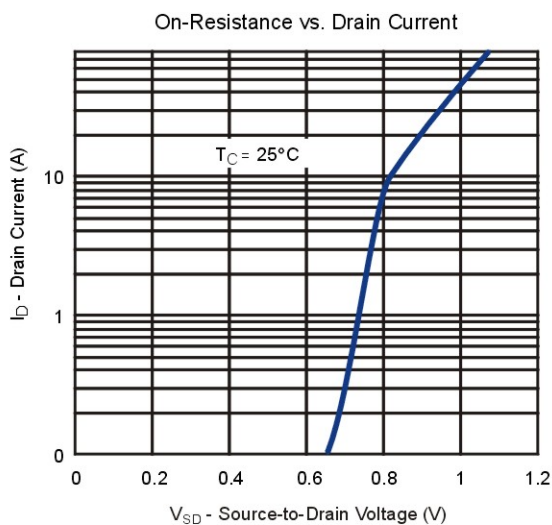
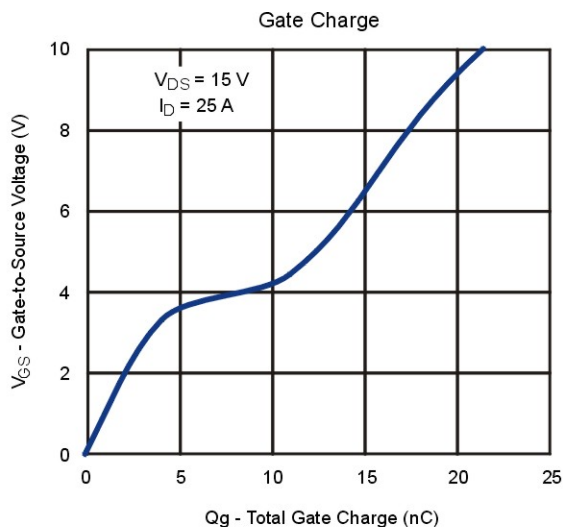
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### Typical Characteristics (T<sub>J</sub> = 25°C Noted)

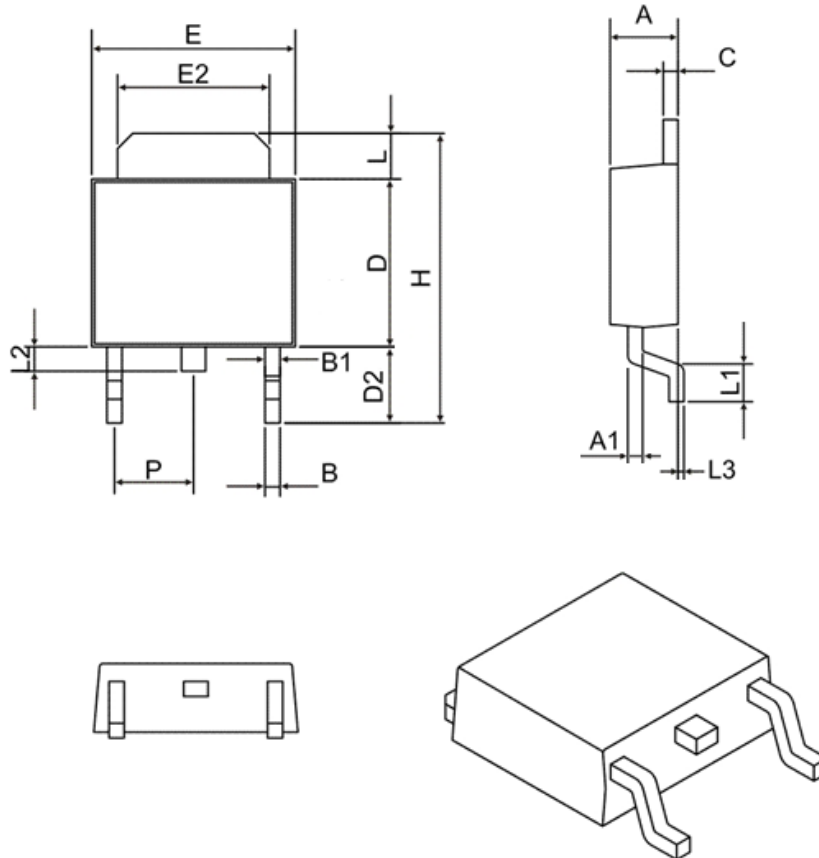


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### Typical Characteristics (T<sub>J</sub> = 25°C Noted)



### TO-252-3L Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	2.00	2.50
A1	0.45	0.60
B	0.50	0.88
B1	0.50	1.14
C	0.40	0.60
D	5.20	6.23
D2	2.743 REF	
H	9.40	10.50
E	6.30	6.80
E2	4.50	5.50
L	0.89	1.70
L1	0.90	1.77
L2	0.50	1.10
L3	0	0.30
P	2.286 BSC	

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