

**N- Channel 40-V (D-S) MOSFET**

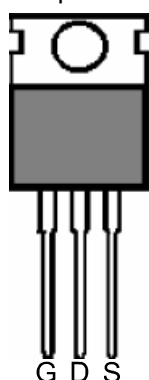
**GENERAL DESCRIPTION**

The ME66N04T is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

**PIN CONFIGURATION**

(TO-220FB-3L)

Top View

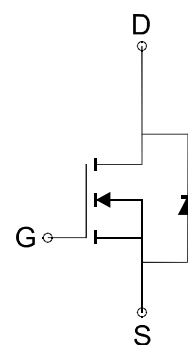


**FEATURES**

- $R_{DS(ON)}=10.5m\Omega@V_{GS}=10V$
- $R_{DS(ON)}=13.5m\Omega@V_{GS}=4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

**APPLICATIONS**

- Power Management
- DC/DC Converter
- Load Switch



N-Channel MOSFET

**Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)**

Parameter		Symbol	Steady	Unit
Drain-Source Voltage		$V_{DS}$	40	V
Gate-Source Voltage		$V_{GS}$	$\pm 25$	V
Continuous Drain Current	$T_c=25^\circ C$	$I_D$	55	A
	$T_c=100^\circ C$		38	
Pulsed Drain Current		$I_{DM}$	220*	A
Maximum Power Dissipation	$T_c=25^\circ C$	$P_D$	100	W
	$T_c=100^\circ C$		50	
Operating Junction Temperature		$T_J$	-55 to 175	$^\circ C$
Thermal Resistance-Junction to Case**		$R_{\theta JC}$	1.5	$^\circ C/W$

\* Drain current is limited by junction temperature

\*\* The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper.

**N- Channel 40-V (D-S) MOSFET**
**Electrical Characteristics (TA=25°C Unless Otherwise Specified)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>STATIC</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>DS</sub> =250 μA	40			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>DS</sub> =250 μA	1	1.6	3	V
I <sub>GSS</sub>	Gate-Body Leakage	V <sub>DS</sub> =0V, V <sub>GS</sub> =±25V			±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			1	μA
R <sub>DS(ON)</sub>	Drain-Source On-Resistance*	V <sub>GS</sub> =10V, I <sub>DS</sub> = 28A		10.5	13.5	mΩ
		V <sub>GS</sub> =4.5V, I <sub>DS</sub> = 28A		13.5	15	
V <sub>SD</sub>	Diode Forward Voltage *	I <sub>SD</sub> =28A, V <sub>GS</sub> =0V		0.8	1.1	V
<b>DYNAMIC</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =48V, V <sub>GS</sub> =10V, I <sub>DS</sub> =28A		62		nC
Q <sub>gs</sub>	Gate-Source Charge			6		
Q <sub>gd</sub>	Gate-Drain Charge			11		
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz		1.2		Ω
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1.0MHz		3522		pF
C <sub>oss</sub>	Output Capacitance			666		
C <sub>rss</sub>	Reverse Transfer Capacitance			172		
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =30V, I <sub>DS</sub> =28A V <sub>GS</sub> =10V, R <sub>G</sub> =4Ω		21	39	ns
t <sub>r</sub>	Turn-On Rise Time			25	48	
t <sub>d(off)</sub>	Turn-Off Delay Time			27	52	
t <sub>f</sub>	Turn-On Fall Time			31	58	

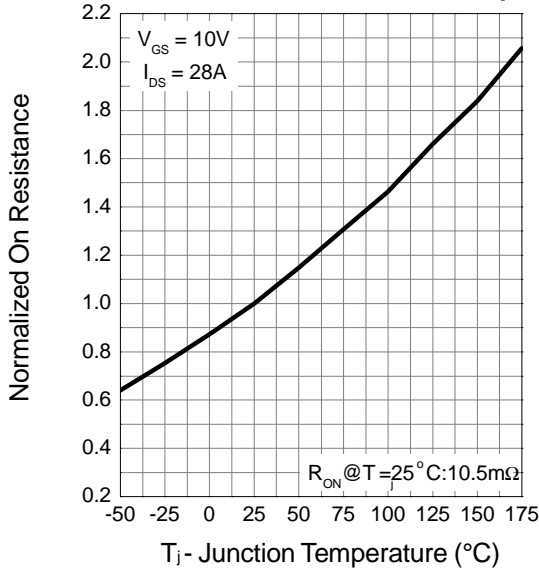
Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

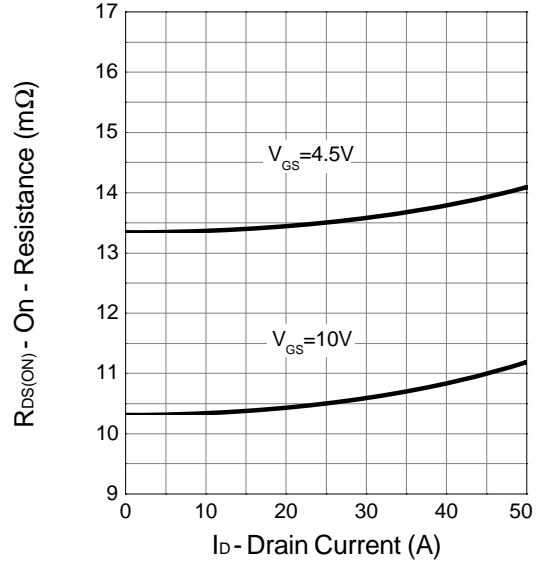
**N- Channel 40-V (D-S) MOSFET**

**Typical Characteristics (T<sub>J</sub> =25°C Noted)**

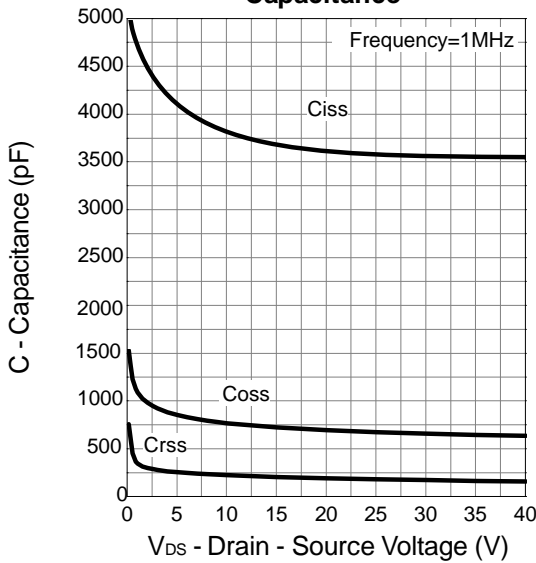
**On Resistance vs. Junction Temperature**



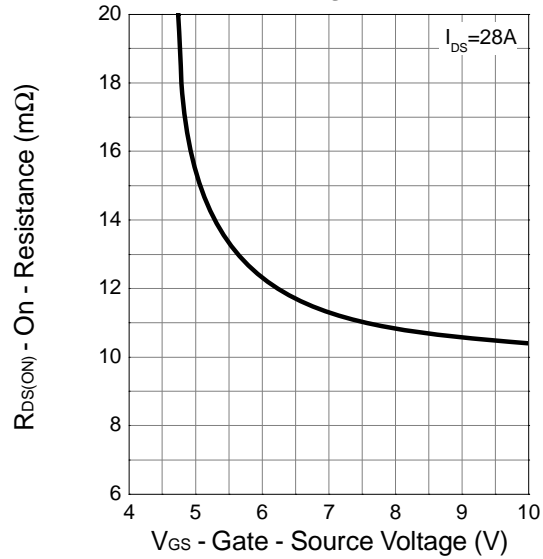
**On Resistance vs. Drain Current**



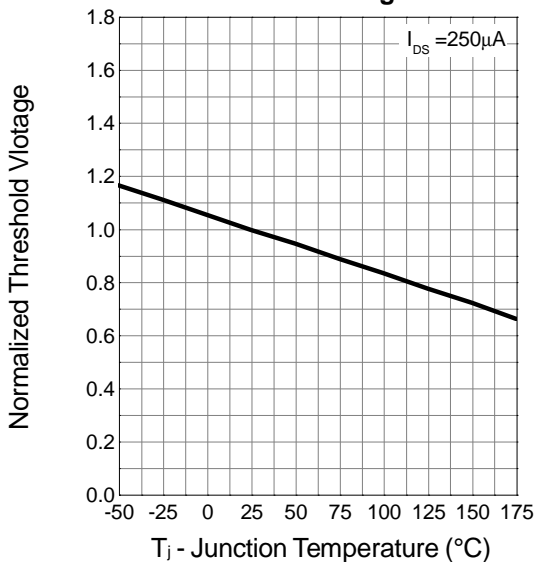
**Capacitance**



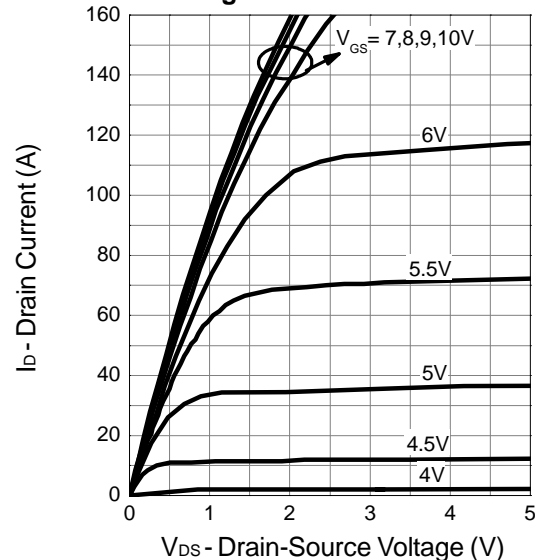
**On Resistance vs. Gate-Source Voltage**



**Threshold Voltage**



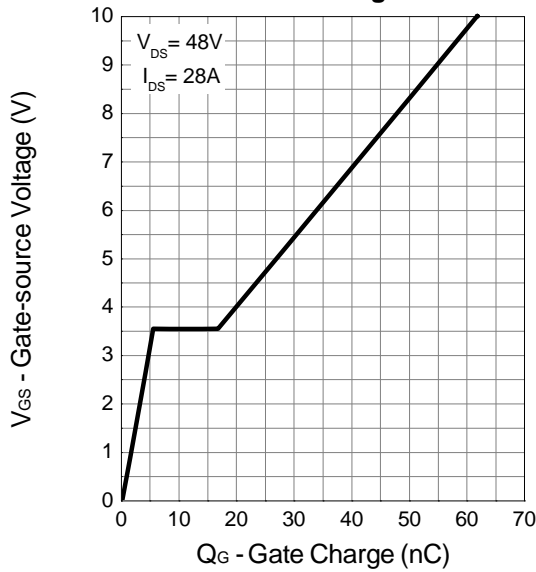
**On-Region Characteristics**



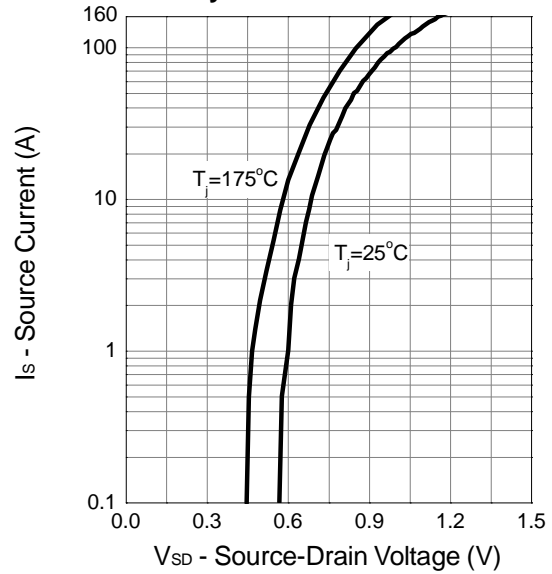
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Typical Characteristics (T<sub>J</sub> = 25°C Noted)

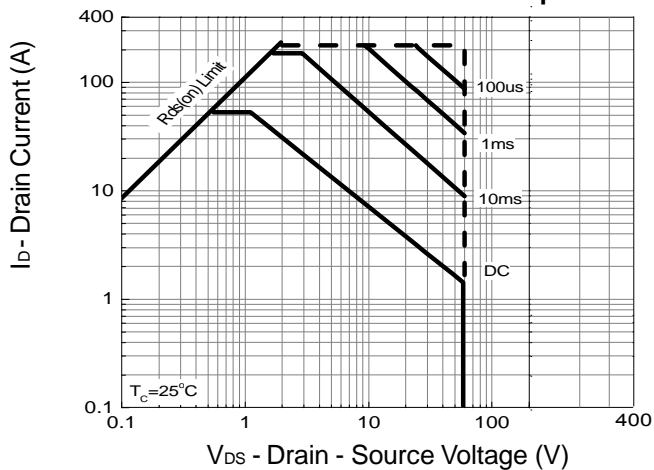
**Gate Charge**



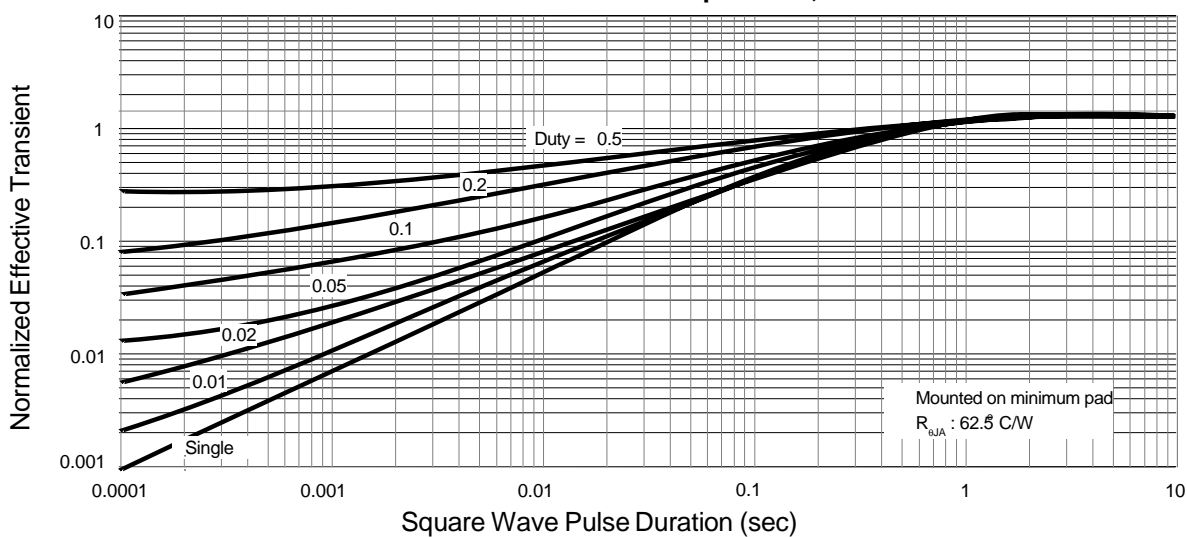
**Body-diode characteristics**



**Maximum Forward Biased Safe Operation Area**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



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