

Dual N-Channel 20V(D-S) Enhancement Mode Mosfet

GENERAL DESCRIPTION

The ME6968ED Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leq 25m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 27m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leq 32m\Omega @ V_{GS}=2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

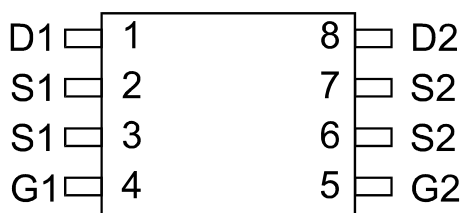
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION

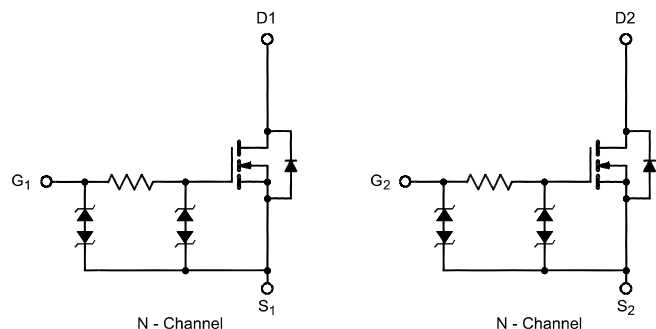
(TSSOP-8)

Top View



Ordering Information: ME6968ED (Pb-free)

ME6968ED-G (Green product)



*Typical value by design

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter		Symbol	10 secs	Maximum	Unit
Drain-Source Voltage		V_{DSS}	20		V
Gate-Source Voltage		V_{GSS}	±12		V
Continuous Drain Current (tJ=150°C)	TA=25°C	I_D	6.5	5.2	A
	TA=70°C		5.5	3.5	
Pulsed Drain Current		I_{DM}	30		A
Continuous Source Current (Diode Conduction)		I_S	1.5	1.0	A
Maximum Power Dissipation	TA=25°C	P_D	1.5	1.0	W
	TA=70°C		0.96	0.64	
Operating Junction Temperature		T_J	-55 to 150		°C
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	70	100	°C/W

* The device mounted on 1in² FR4 board with 2 oz copper

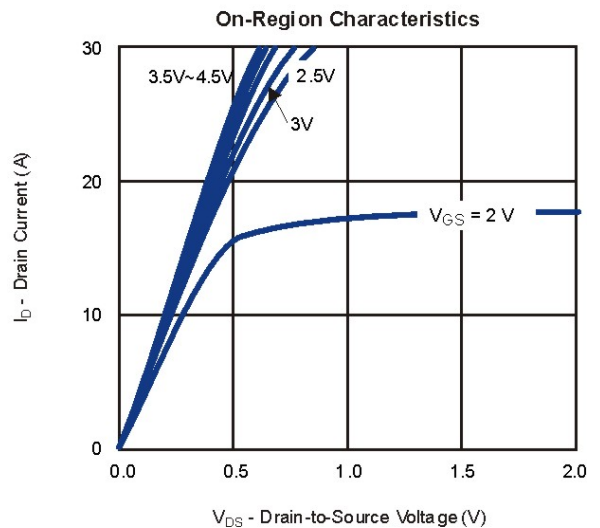
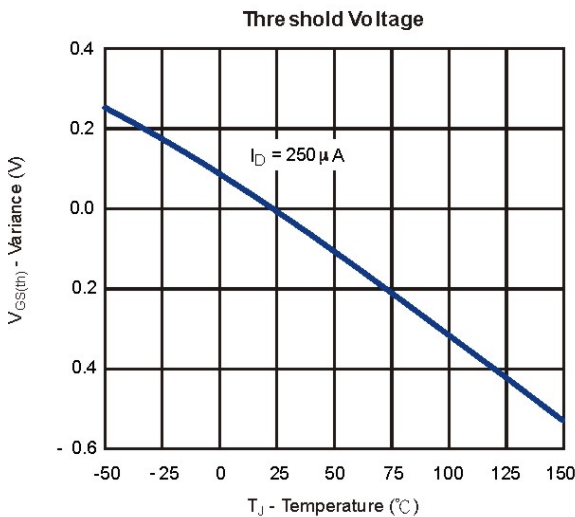
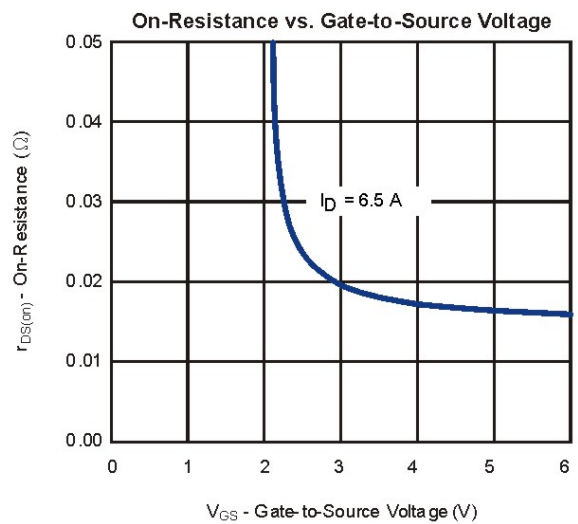
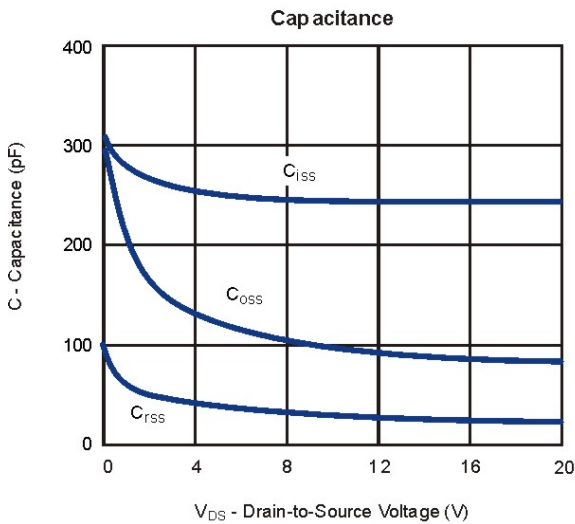
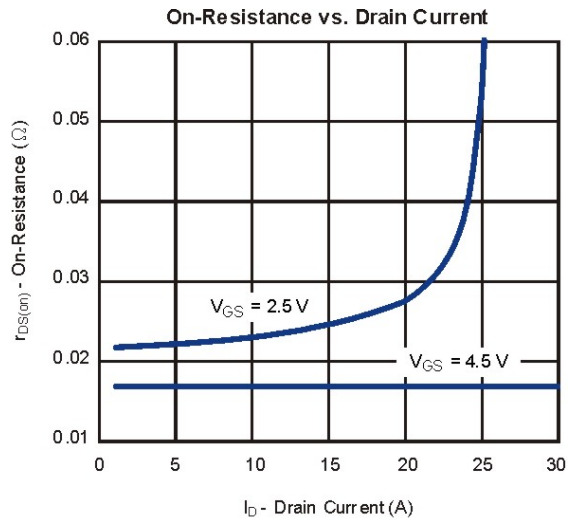
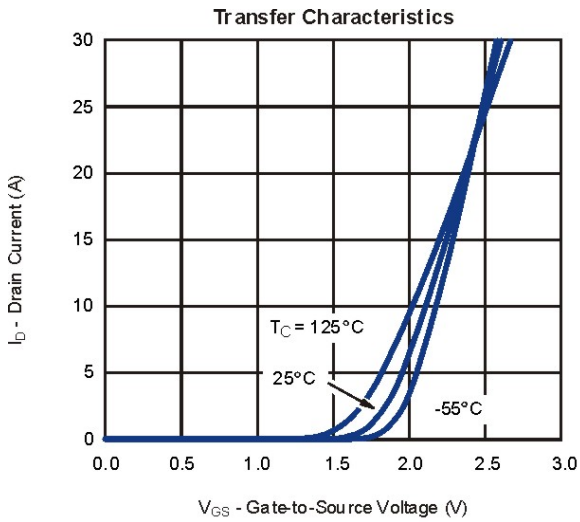
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Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

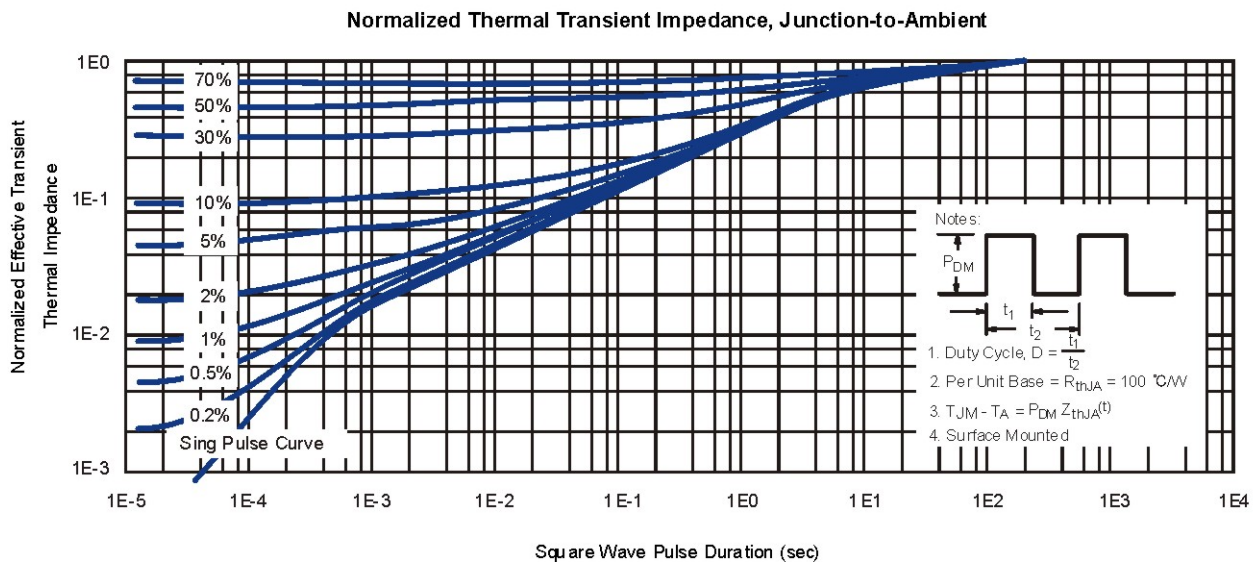
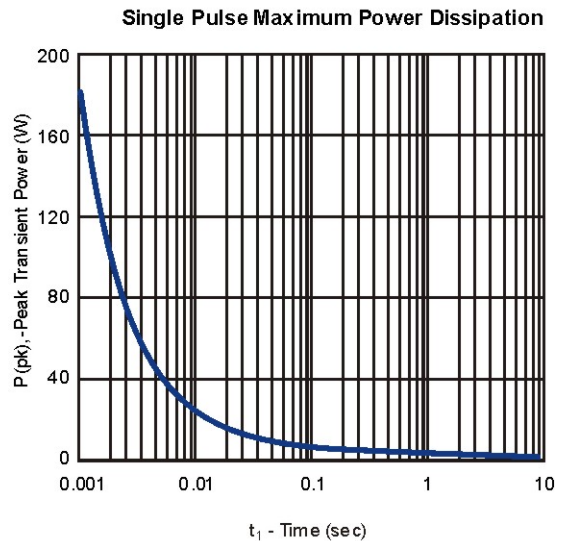
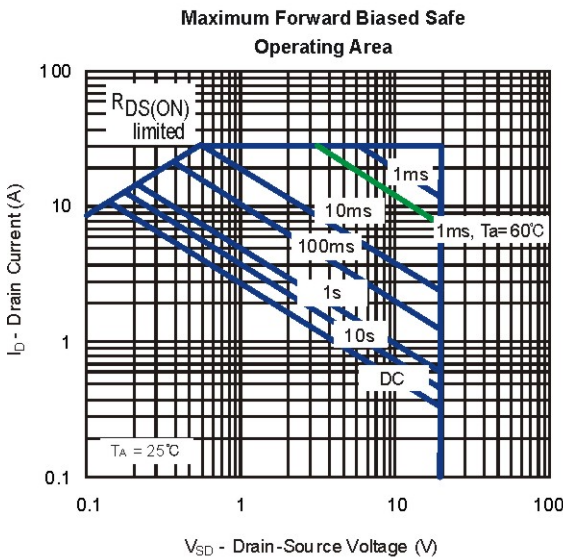
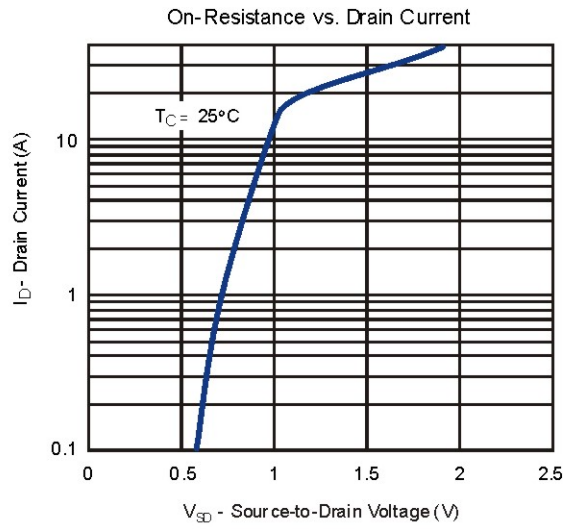
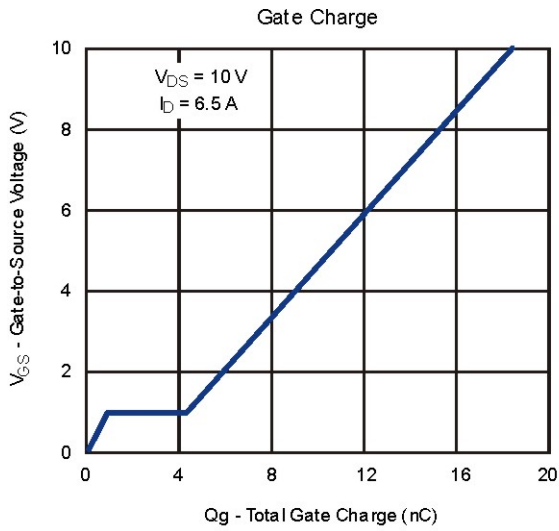
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	0.6	0.8	1.0	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±12V			±10	μA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V			1	μA
		V _{DS} =20V, V _{GS} =0V T _J =70°C			25	
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =10V, I _D = 6.5A		19	25	mΩ
		V _{GS} =8V, I _D = 6.5A		19.5	25.5	
		V _{GS} =6V, I _D = 6.5A		20	26	
		V _{GS} =4.5V, I _D = 6.0A		21	27	
		V _{GS} =4V, I _D = 6.0A		22	28	
		V _{GS} =3V, I _D = 6.0A		24	27.2	
V _{SD}	Diode Forward Voltage	I _S =1.5A, V _{GS} =0V		0.73	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =10V, V _{GS} =10V, I _D =6.5A		18	22	nC
Q _g	Total Gate Charge	V _{DS} =10V, V _{GS} =4.5V, I _D =6.5A		10	12	
Q _{gs}	Gate-Source Charge			2.2		
Q _{gd}	Gate-Drain Charge			3.6		
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		245	300	pF
C _{oss}	Output Capacitance			90		
C _{rss}	Reverse Transfer Capacitance			26		
t _{d(on)}	Turn-On Delay Time	V _{DD} =10V, R _L =10Ω I _D =1A, V _{GEN} =4.5V R _G =6Ω		140	200	ns
t _r	Turn-On Rise Time			210	250	
t _{d(off)}	Turn-Off Delay Time			390	450	
t _f	Turn-Off Fall Time			220	260	

Notes: a. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%

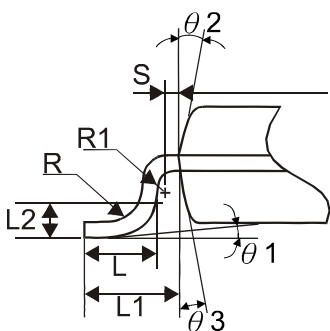
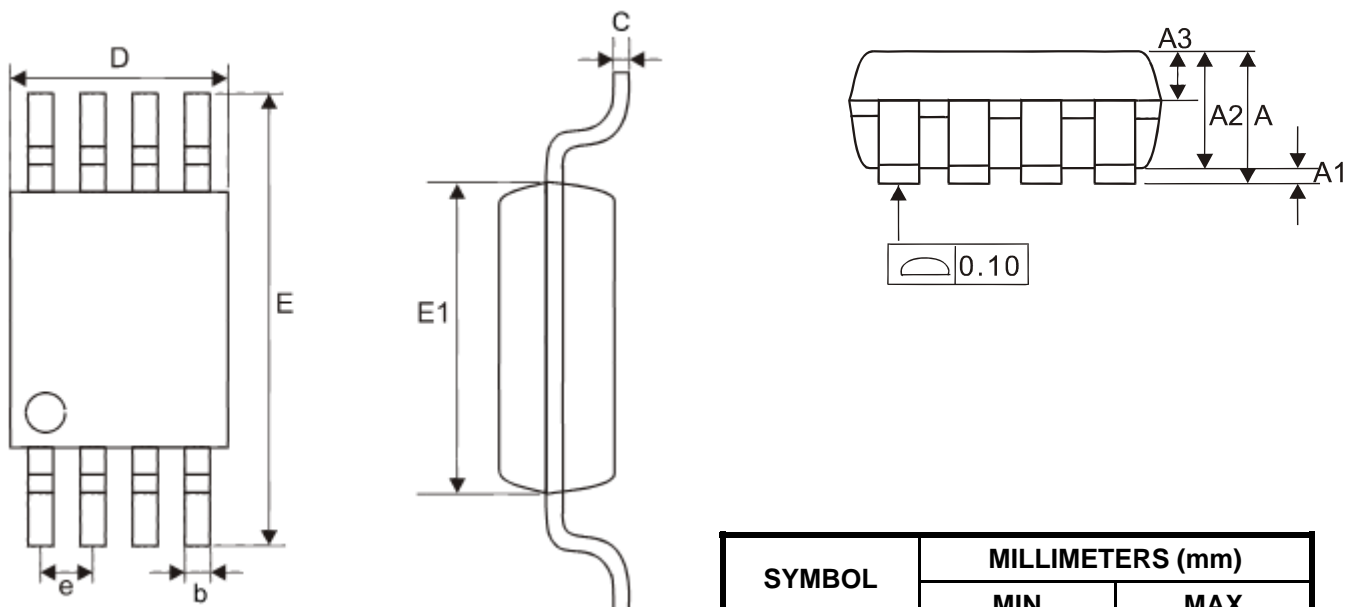
Typical Characteristics (T_J = 25°C Noted)



Typical Characteristics (T_J = 25°C Noted)



TSSOP-8 Package



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	-	1.20
A1	0.05	0.15
A2	0.90	1.05
A3	0.34	0.54
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.20	6.60
E1	4.30	4.50
e	0.65BSC	
L	0.45	0.75
L1	1.00REF	
L2	0.25BSC	
R	0.09	-

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

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