

N-Channel 30V (D-S) MOSFET, ESD Protected
GENERAL DESCRIPTION

The ME7804-G N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leq 16m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 25m\Omega @ V_{GS}=4.5V$

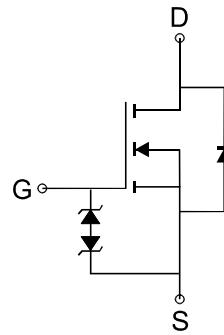
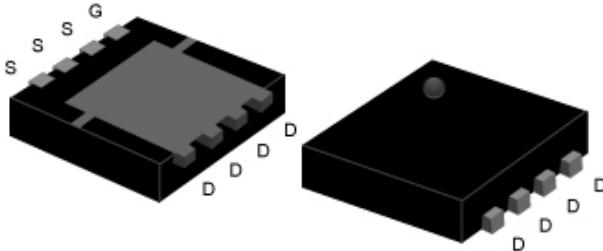
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC
- ESD Protected

PIN CONFIGURATION

(DFN 3.3x3.3)

Top View



Ordering Information: ME7804S-G (Green product-Halogen free)

Absolute Maximum Ratings ($T_j=25^\circ C$ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_A=25^\circ C$	I_D	12.2	A
	$T_A=70^\circ C$		9.7	
Pulsed Drain Current		I_{DM}	50	A
Maximum Power Dissipation	$T_A=25^\circ C$	P_D	3.8	W
	$T_A=70^\circ C$		2.4	
Operating Junction Temperature		T_J	150	$^\circ C$
Storage Temperature Range		T_{STG}	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient*		$R_{\Theta JA}$	33	$^\circ C/W$

*The device mounted on 1in² FR4 board with 2 oz copper

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Electrical Characteristics (TA = 25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BVDSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1		3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±16V			±10	μA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V			1	μA
R _{DSON}	Drain-Source On-State Resistance ^a	V _{GS} =10V, I _D = 10A		13	16	mΩ
		V _{GS} =4.5V, I _D = 5A		19	25	
V _{SD}	Diode Forward Voltage	I _S =9A, V _{GS} =0V		0.8		V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =10V, I _D =10A		18		nC
Q _g	Total Gate Charge			8.8		
Q _{gs}	Gate-Source Charge	V _{DS} =15V, V _{GS} =4.5V, I _D =10A		4.2		
Q _{gd}	Gate-Drain Charge			3.7		
C _{iss}	Input Capacitance			729		pF
C _{oss}	Output Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		94		
C _{rss}	Reverse Transfer Capacitance			29		
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		0.9		Ω
t _{d(on)}	Turn-On Delay Time			14		ns
t _r	Turn-On Rise Time	V _{DS} =25V, R _L =25Ω		9.5		
t _{d(off)}	Turn-Off Delay Time	R _{GEN} =6Ω, V _{GS} =10V		44		
t _f	Turn-Off Fall Time			5.7		

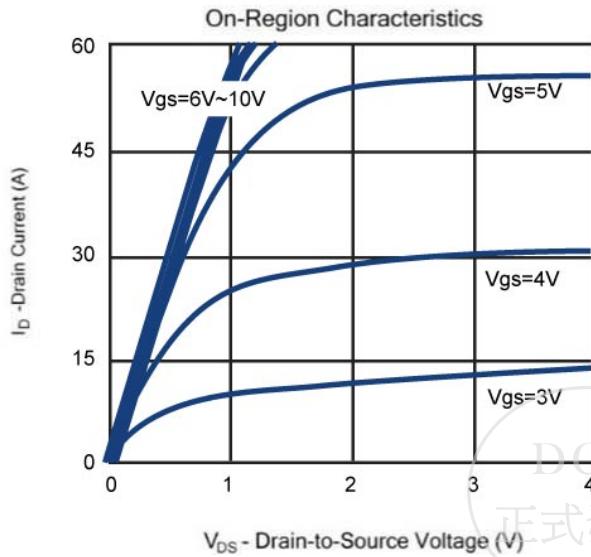
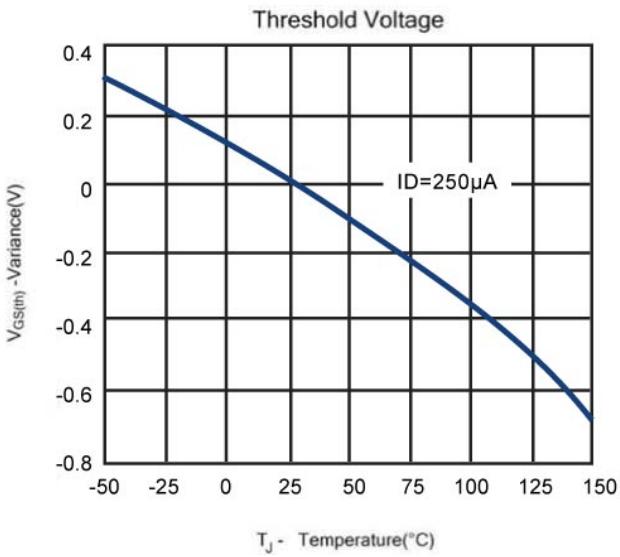
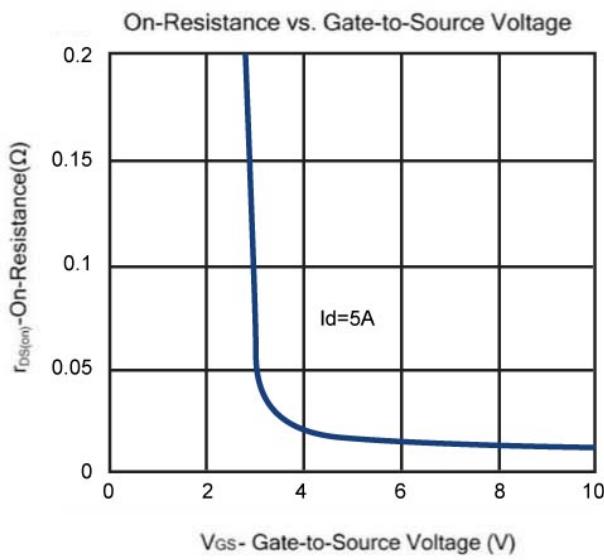
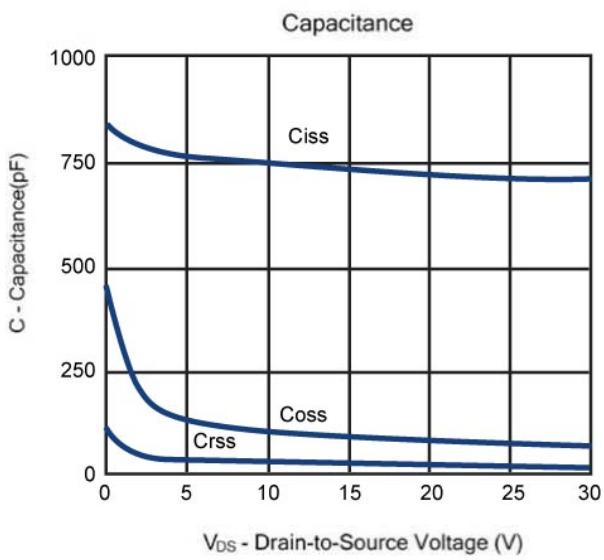
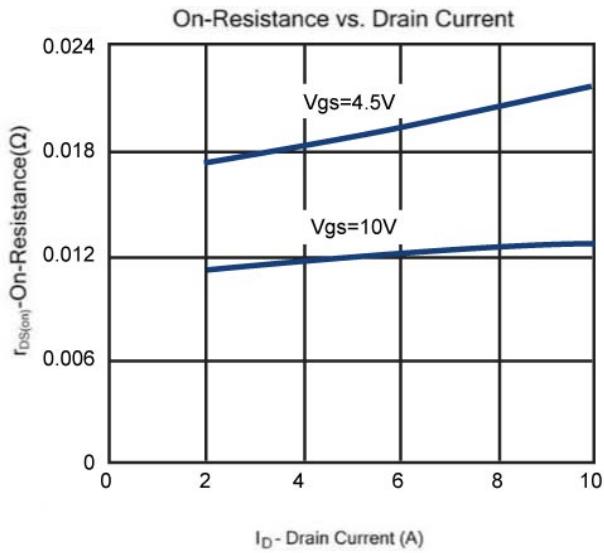
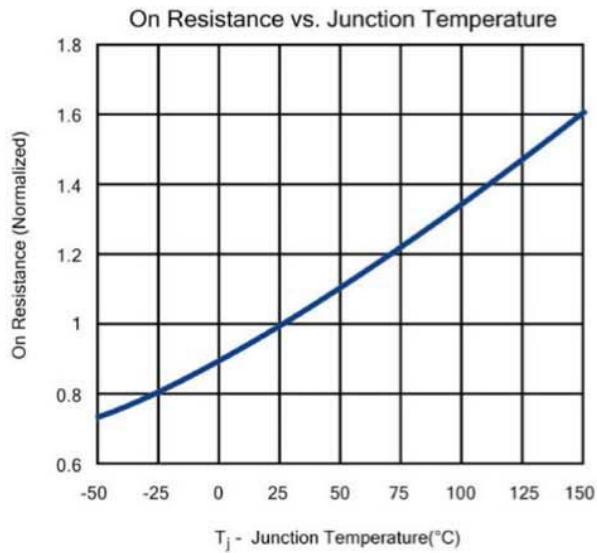
Notes: a. Pulse test: pulse width≤ 300us, duty cycle≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



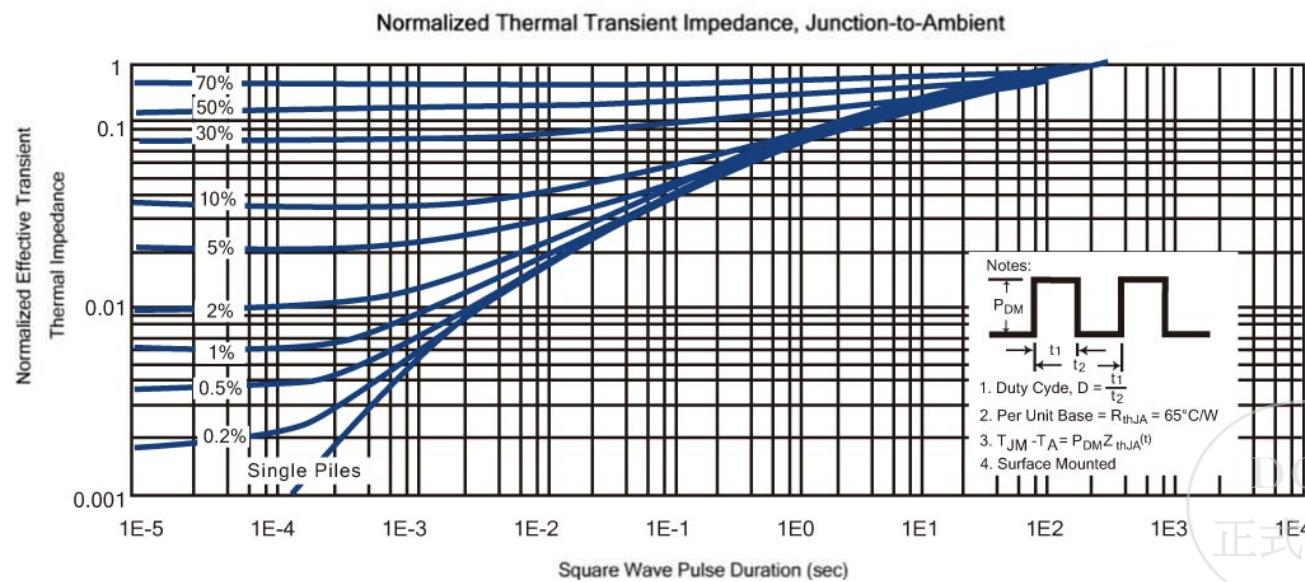
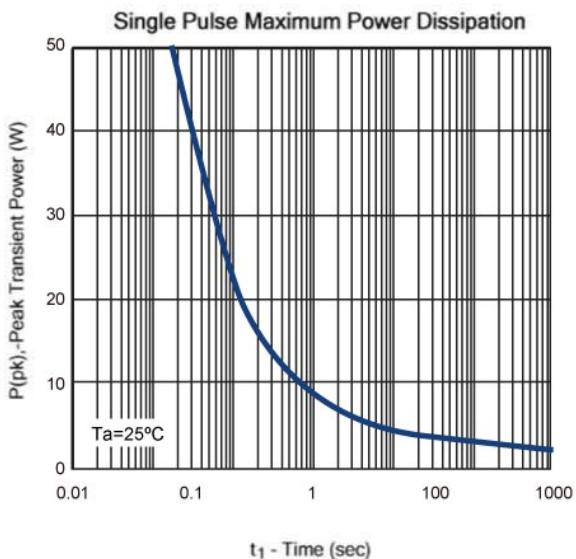
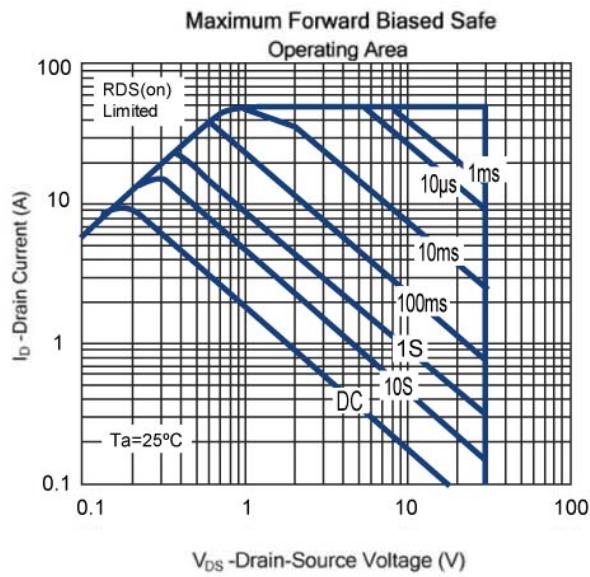
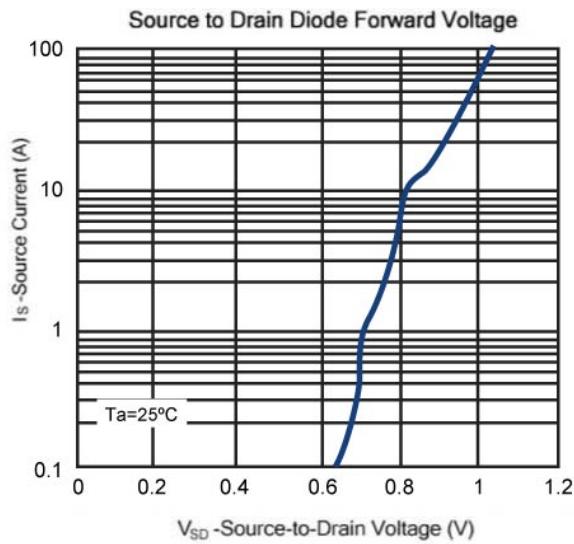
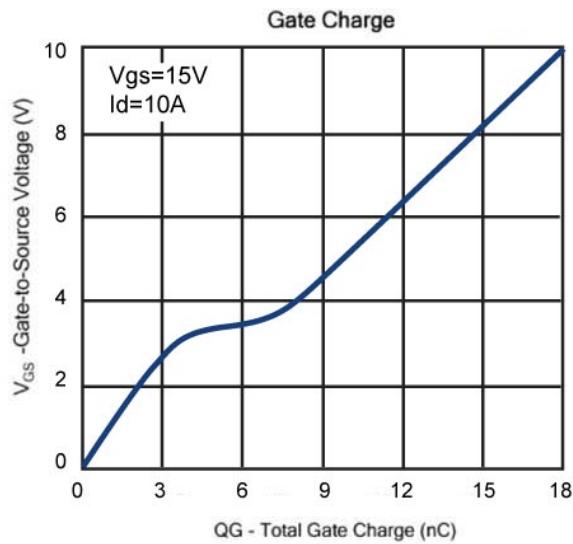
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Typical Characteristics ($T_J = 25^\circ\text{C}$ Noted)

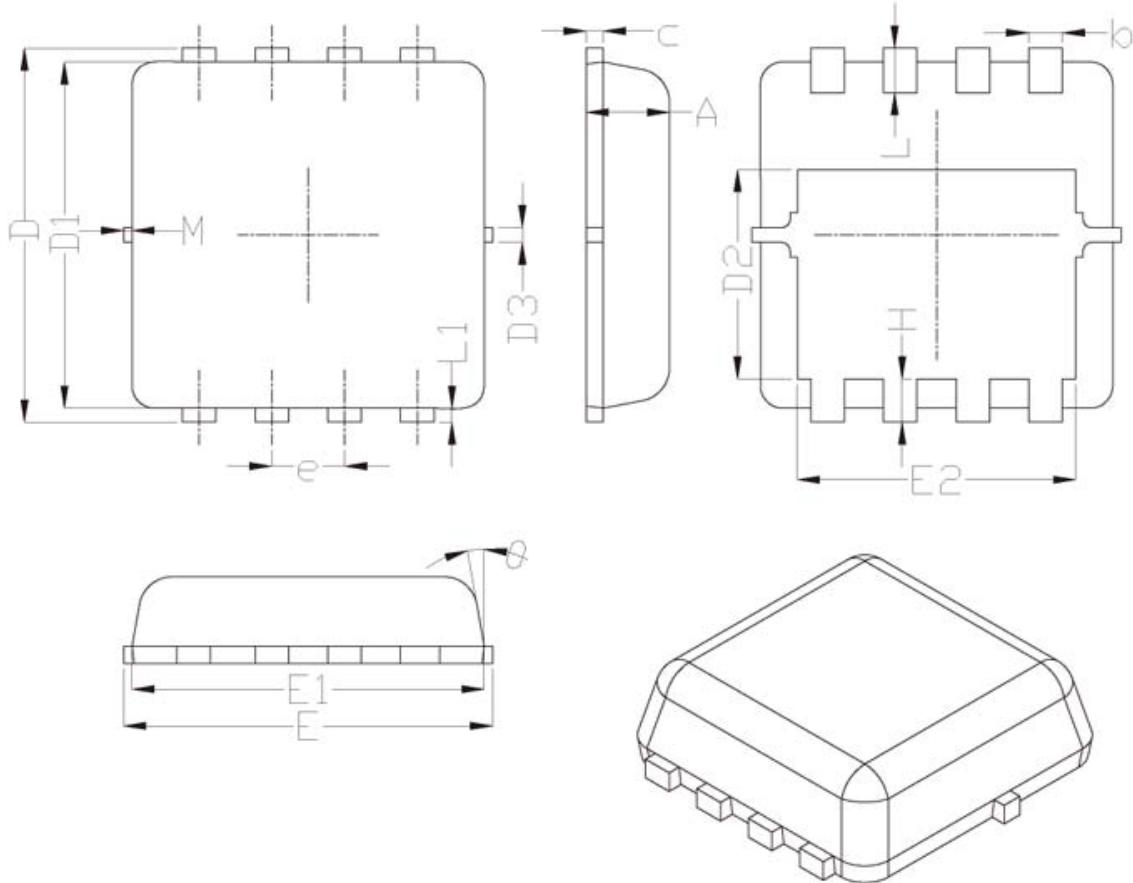


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Typical Characteristics (T_J = 25°C Noted)



DFN(S) 3.3x3.3 Package Outline



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	---	0.13	---
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
theta	---	10°	12°
M	*	*	0.15
* Not specified			

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