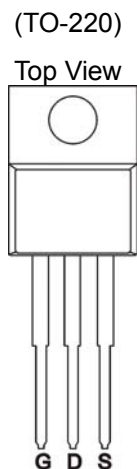


N- Channel 75-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME80N75T is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

PIN CONFIGURATION

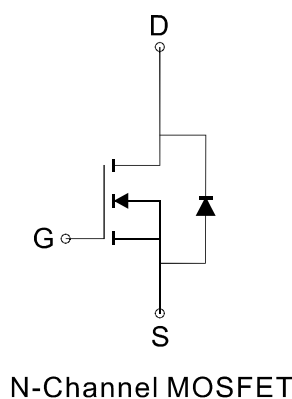


FEATURES

- $R_{DS(ON)} \leq 10m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management
- DC/DC Converter
- Load Switch



Ordering Information: ME80N75T (Pb-free)
ME80N75T-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DSS}	75	V
Gate-Source Voltage		V_{GSS}	±25	V
Continuous Drain Current*	Tc=25°C	I_D	93	A
	Tc=70°C		78	
Pulsed Drain Current		I_{DM}	372	A
Maximum Power Dissipation	Tc=25°C	P_D	200	W
	Tc=70°C		140	
Operating Junction and Storage Temperature Range		T_J	-55 to 175	°C
Thermal Resistance-Junction to Case**		$R_{\theta JC}$	0.75	°C/W

* Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 80A.

** The device mounted on 1in² FR4 board with 2 oz copper.



N- Channel 75-V (D-S) MOSFET

Electrical Characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	75			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	2.0		4.0	V
I _{GSS}	Gate-Body Leakage	V _{DS} =0V, V _{GS} =±25V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =75V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-Resistance*	V _{GS} =10V, I _D =40A		8	10	mΩ
V _{SD}	Diode Forward Voltage *	I _S =40A, V _{GS} =0V		0.9	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DD} =60V, V _{GS} =10V, I _D =75A		134		nC
Q _g	Total Gate Charge	V _{DD} =60V, V _{GS} =4.5V, I _D =75A		27		
Q _{gs}	Gate-Source Charge			36		
Q _{gd}	Gate-Drain Charge			50		
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		0.8		Ω
C _{iss}	Input Capacitance	V _{DS} =20V, V _{GS} =0V, f=1MHz		6200		pF
C _{oss}	Output Capacitance			437		
C _{rss}	Reverse Transfer Capacitance			144		
t _{d(on)}	Turn-On Delay Time	V _{GS} =10V, R _L =15Ω V _{DD} =30V, R _G =10Ω		60		ns
t _r	Turn-On Rise Time			43		
t _{d(off)}	Turn-Off Delay Time			159		
t _f	Turn-Off Fall Time			47		

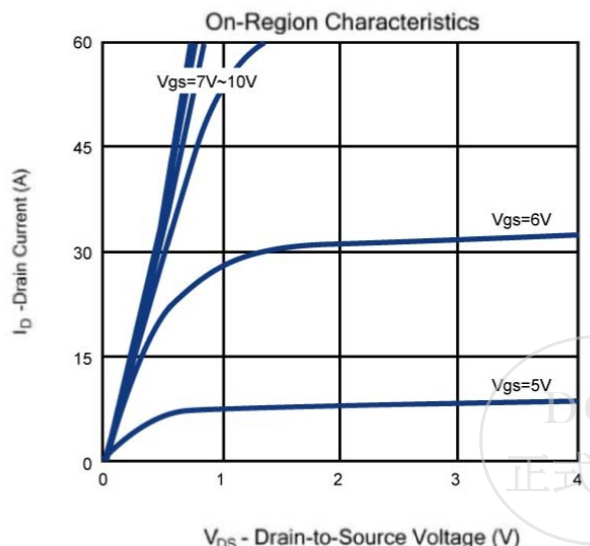
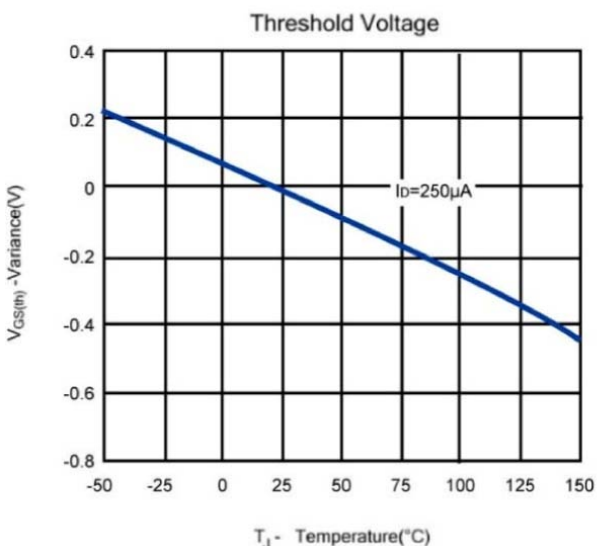
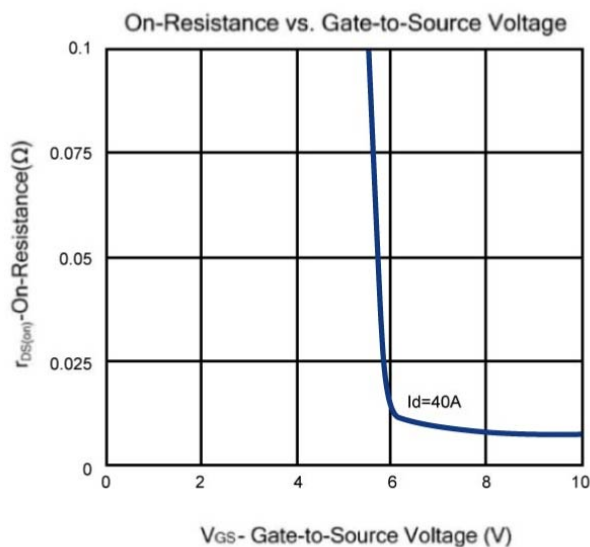
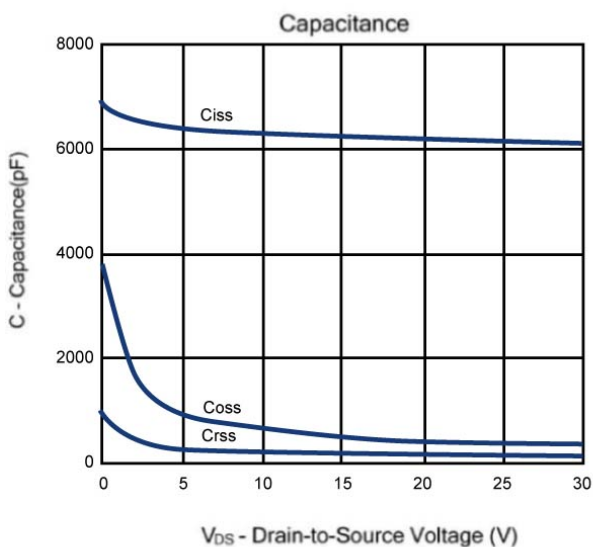
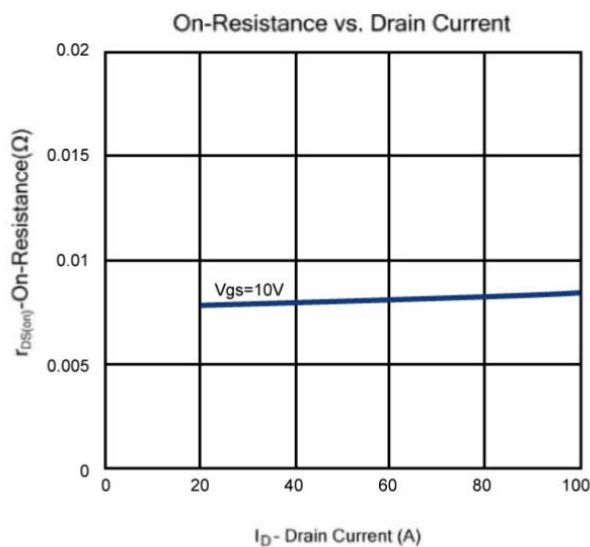
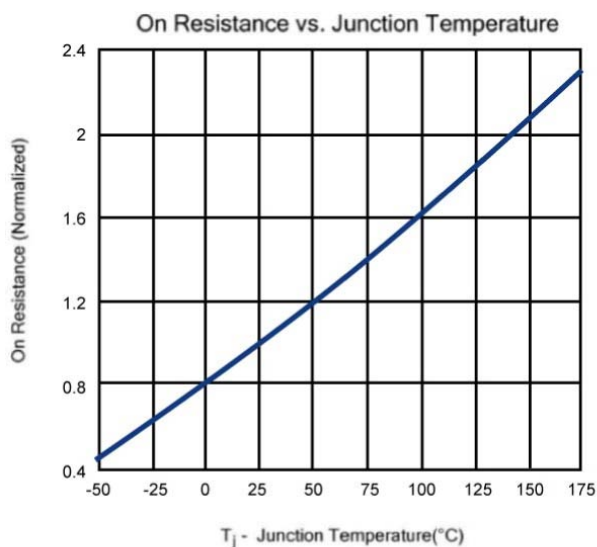
Notes: a. pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



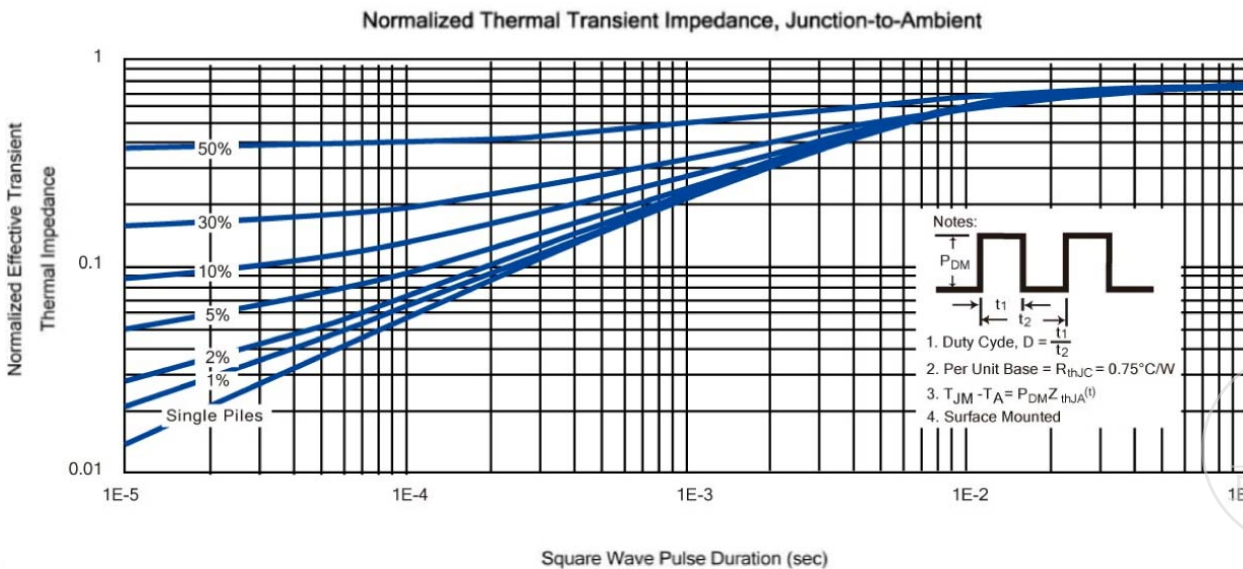
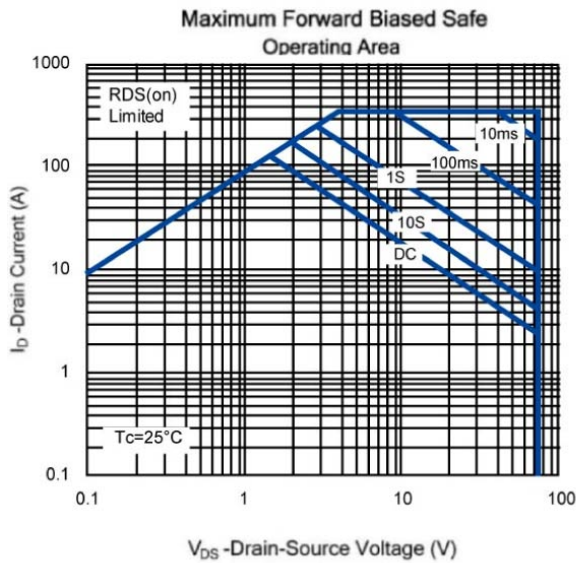
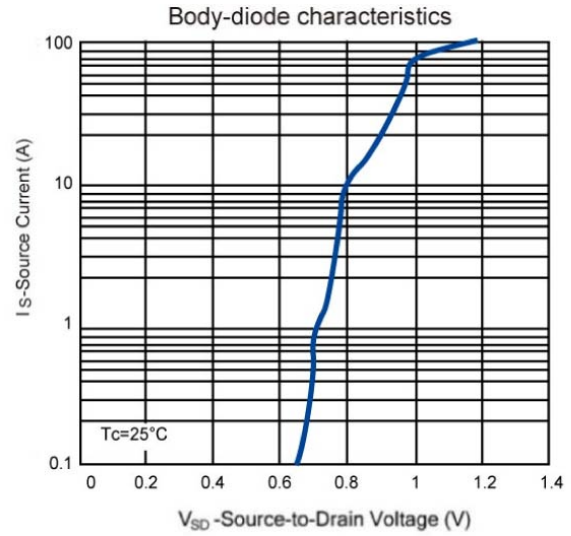
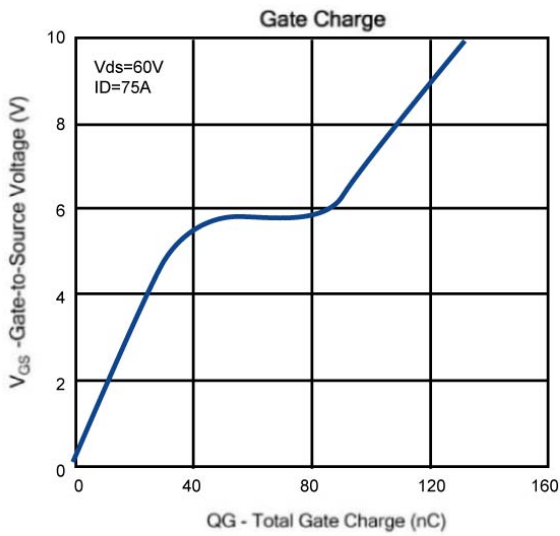
N- Channel 75-V (D-S) MOSFET

Typical Characteristics (T_J =25°C Noted)

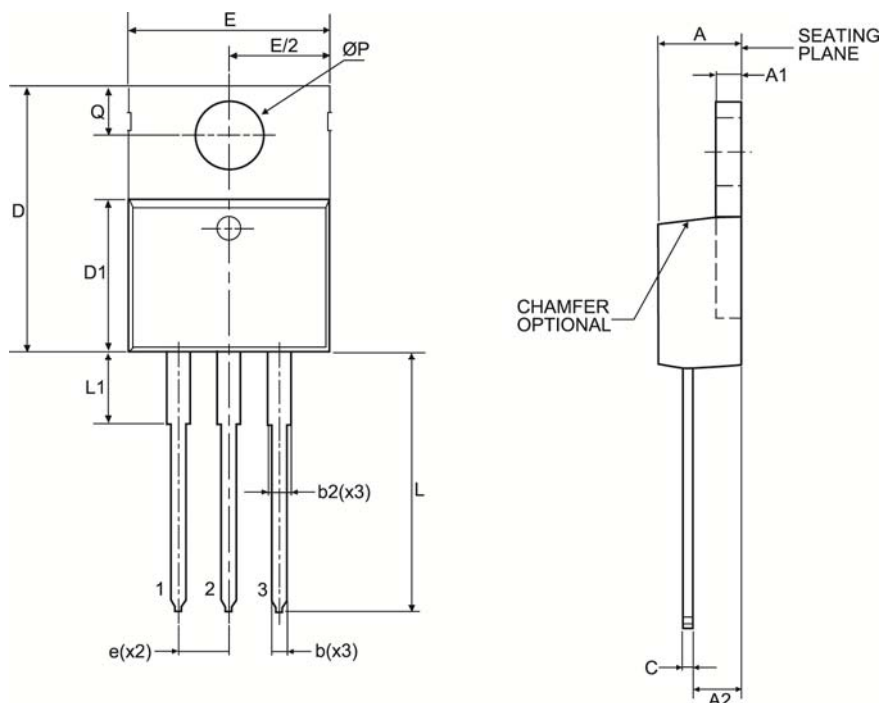


N- Channel 75-V (D-S) MOSFET

Typical Characteristics (T_J =25°C Noted)



TO-220 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	3.50	4.90
A1	1.00	1.40
A2	2.00	3.00
b	0.70	1.40
c	0.35	0.65
D	14.00	16.50
D1	8.30	9.50
E	9.60	10.70
e	2.54 BSC	
L	12.50	15.00
ØP	3.60 TYP	
Q	2.50	3.10
b2	1.10	1.80
L1	2.40	3.20



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