

**P-Channel 35V (D-S) MOSFET, ESD Protected**

**GENERAL DESCRIPTION**

The ME8107-G is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

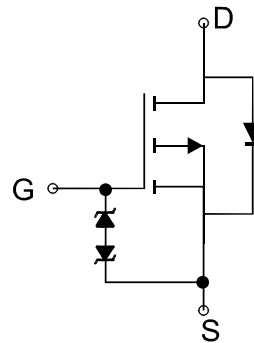
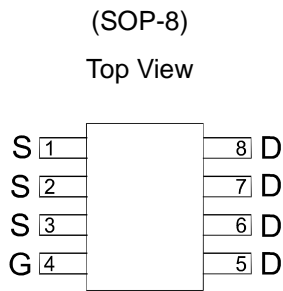
**FEATURES**

- $R_{DS(ON)} \leq 7.2m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 12m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

**APPLICATIONS**

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- LCD Display inverter

**PIN CONFIGURATION**



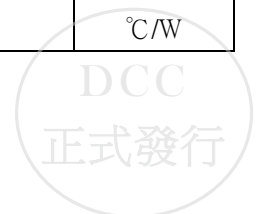
Ordering Information: ME8107(Pb-free)

ME8107-G (Green product-Halogen free)

**Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)**

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	$V_{DS}$	-35	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_A = 25^\circ C$	-14
		$T_A = 70^\circ C$	-11
Pulsed Drain Current	$I_{DM}$	-59	A
Maximum Power Dissipation*	$P_D$	$T_A = 25^\circ C$	2.5
		$T_A = 70^\circ C$	1.6
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	50	$^\circ C/W$

\* The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper



## P-Channel 35V (D-S) MOSFET, ESD Protected

Electrical Characteristics (T<sub>A</sub>=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
V <sub>BR(DSS)</sub>	Drain-source breakdown voltage	I <sub>D</sub> =-10mA, V <sub>GS</sub> =0V	-35			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> =-250 μA	-1		-3.0	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±16V			±10	μA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V			-1	μA
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance <sup>a</sup>	V <sub>GS</sub> =-10V, I <sub>D</sub> = -7A		5.5	7.2	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> = -6.5A		8	12	
V <sub>SD</sub>	Diode Forward Voltage	I <sub>DR</sub> =-7A, V <sub>GS</sub> =0V		0.78	1.2	V
<b>DYNAMIC</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DD</sub> =-24V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-13A		58		nC
Q <sub>g</sub>	Total Gate Charge	V <sub>DD</sub> =-24V, V <sub>GS</sub> =-10V, I <sub>D</sub> =-13A		120		
Q <sub>gs</sub>	Gate-Source Charge			26		
Q <sub>gd</sub>	Gate-Drain Charge			33		
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =-15V, R <sub>L</sub> =15Ω V <sub>GS</sub> =-10V, R <sub>G</sub> =6Ω		77		ns
t <sub>r</sub>	Turn-On Rise Time			32		
t <sub>d(off)</sub>	Turn-Off Delay Time			213		
t <sub>f</sub>	Turn-Off Fall Time			64		
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=-1MHZ		5330		pF
C <sub>oss</sub>	Output Capacitance			710		
C <sub>rss</sub>	Reverse Transfer Capacitance			242		

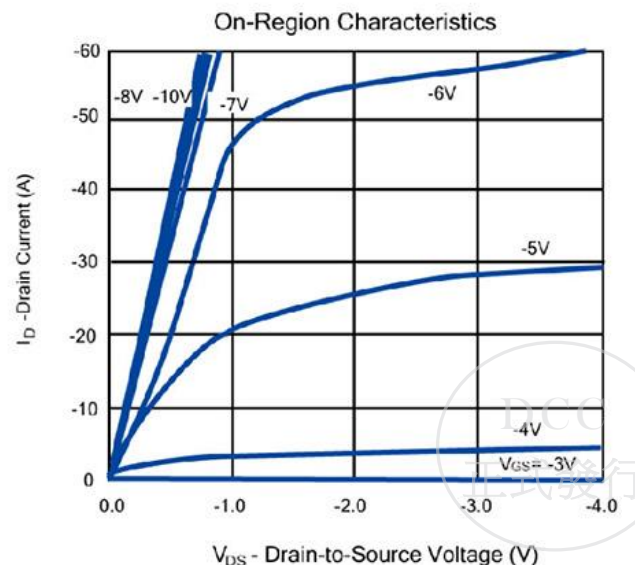
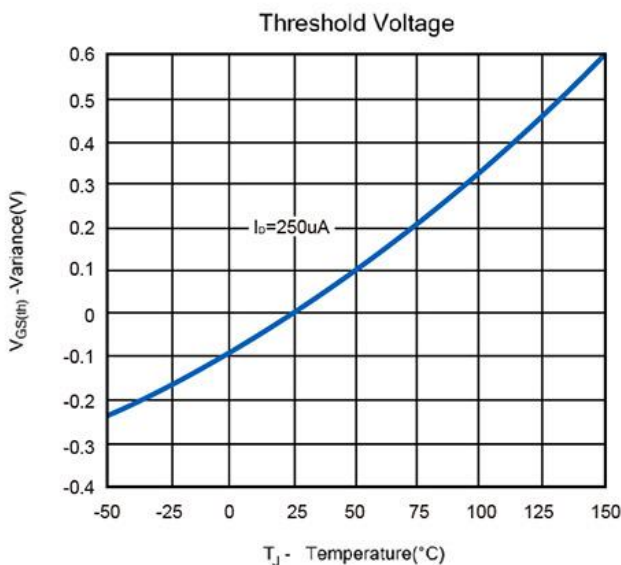
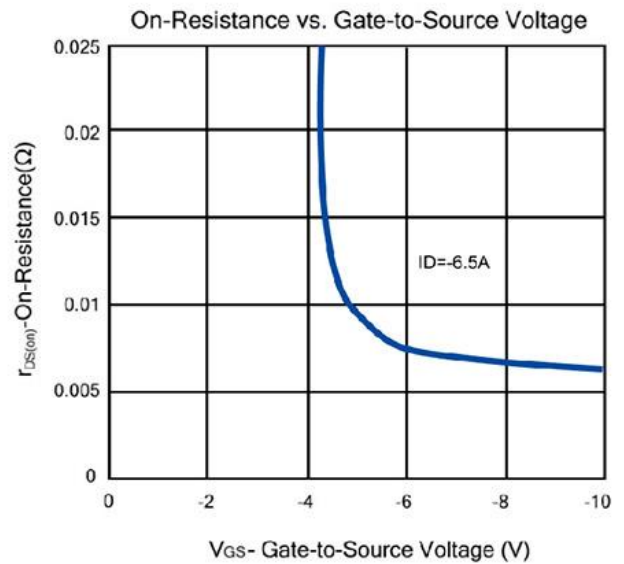
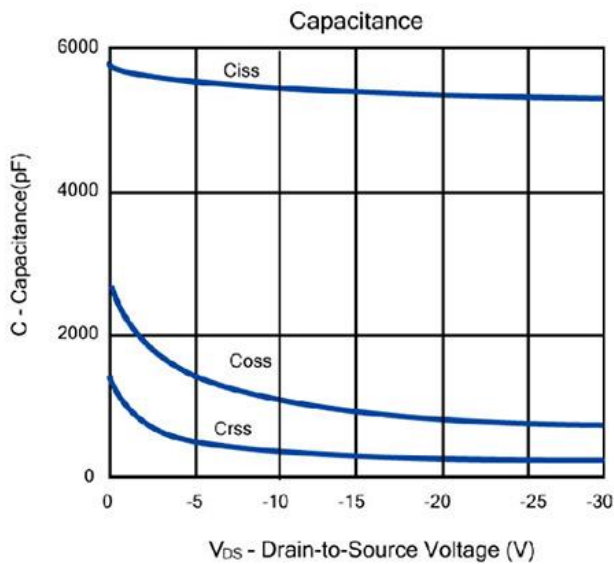
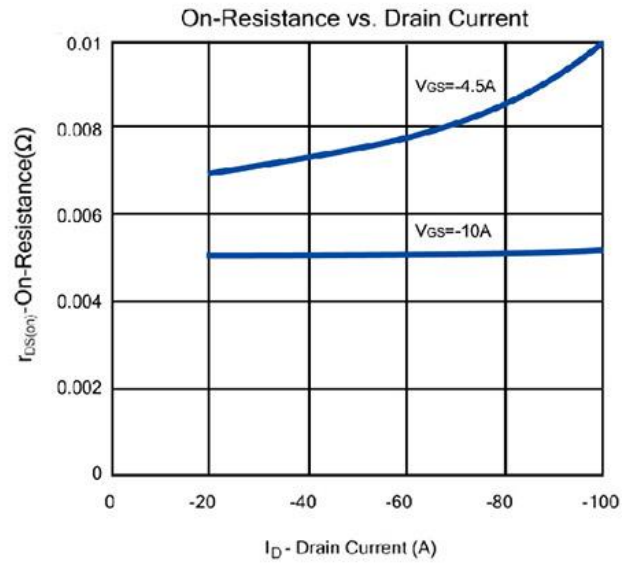
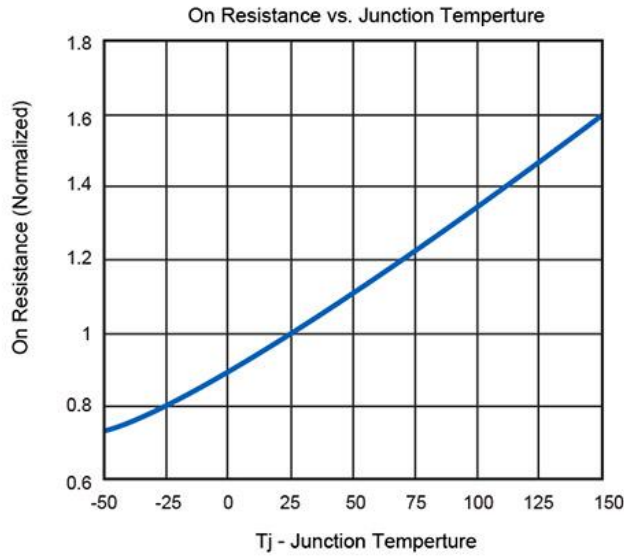
Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



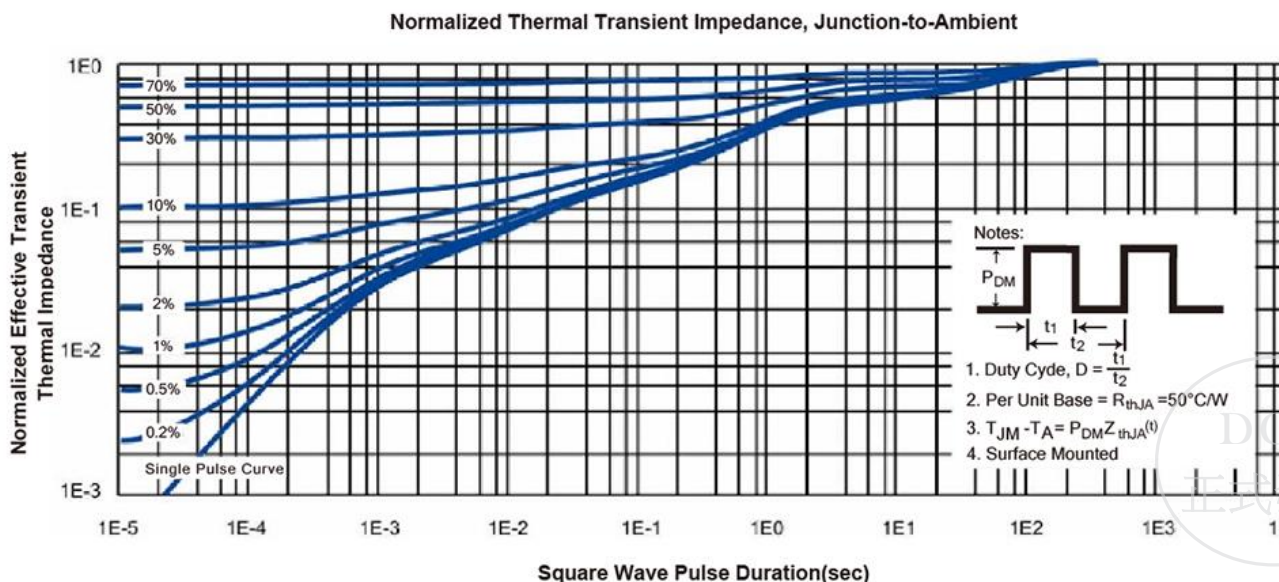
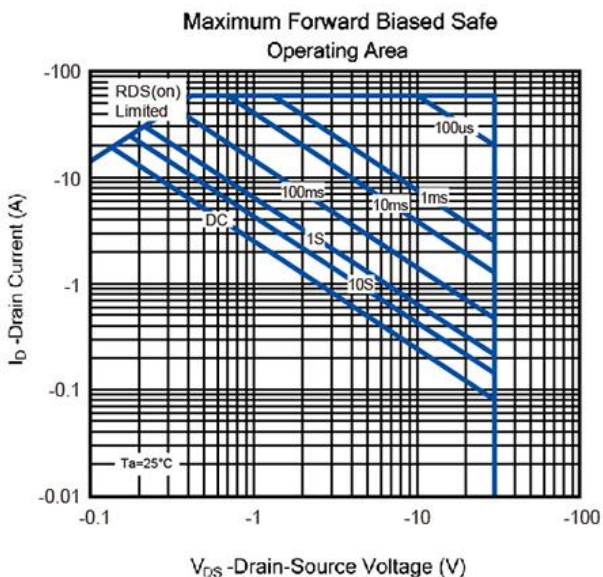
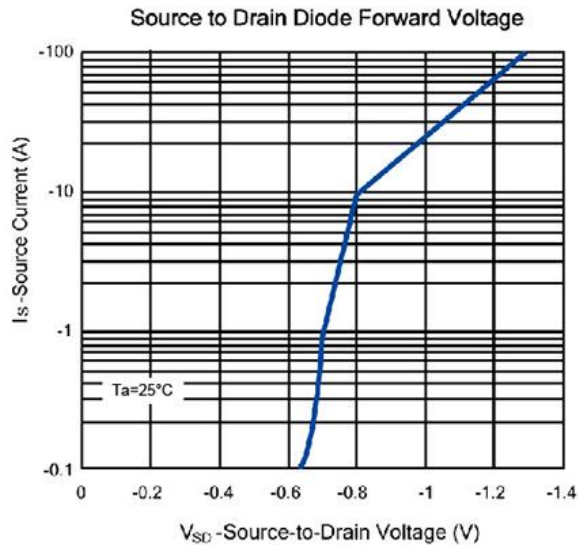
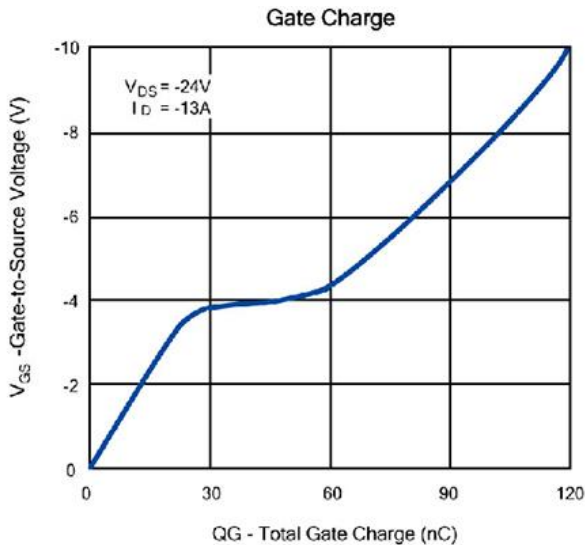
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**Typical Characteristics (T<sub>J</sub> =25°C Noted)**

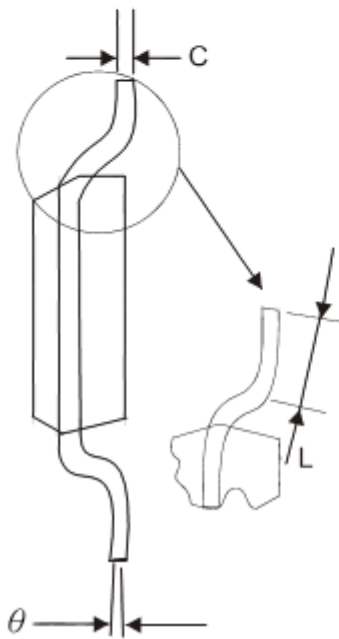
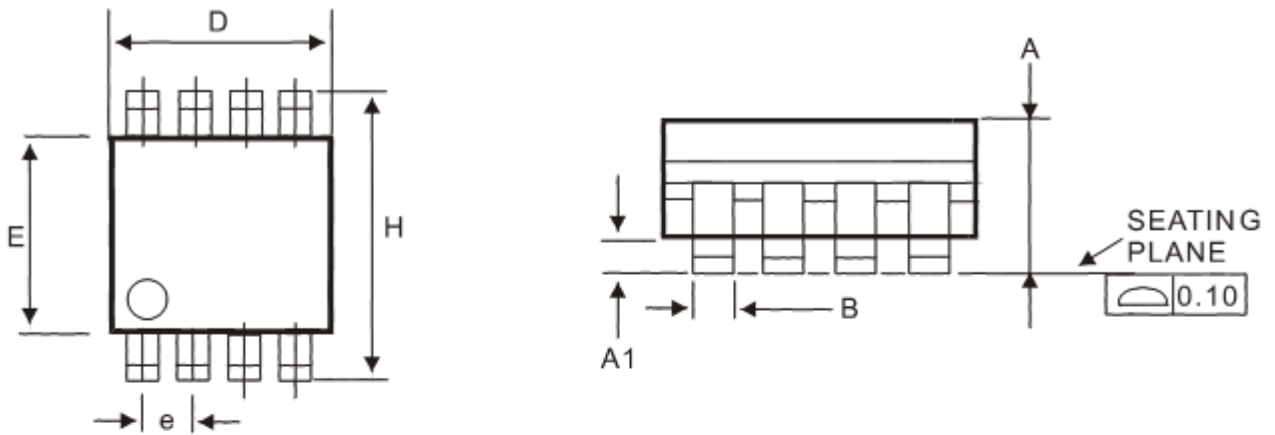


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**Typical Characteristics (T<sub>J</sub> =25°C Noted)**



**SOP-8 Package Outline**



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
$\theta$	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.





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