Preliminary-MEE15N10-G

N-Channel 100-V (D-S) MOSFET

GENERAL DESCRIPTION

The MEE15N10-G is a N-Channel enhancement mode power field effect transistors, using Force-MOS patented Extended Trench Gate(ETG) technology. This advanced technology is especially tailored to minimize on state resistance and gate charge, and enhance avalanche capability. These devices are particularly suited for medium voltage application such as charger, adapter, notebook computer power management and other lighting dimming powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 100m\Omega$ @V_{GS}=10V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

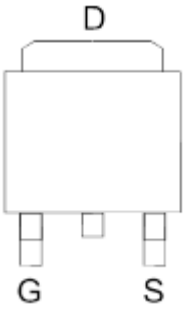
APPLICATIONS

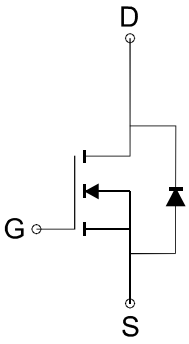
- Power Management
- Synchronous Rectification
- Load Switch

PIN CONFIGURATION

(TO-252-3L)

Top View





N-Channel MOSFET

Ordering Information: MEE15N10-G (Green product-Halogen free)

Absolute Maximum Ratings (T_C=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25℃	I_D	15.4	A
	T_C=70℃		12.3	
Pulsed Drain Current		I_{DM}	62	A
Maximum Power Dissipation	T_C=25℃	P_D	37.9	W
	T_C=70℃		24.2	
Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	℃
Thermal Resistance-Junction to Case *		$R_{\theta JC}$	3.3	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

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N-Channel 100-V (D-S) MOSFET

Electrical Characteristics (T_C =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance [a]	V_{GS}=10V, I_D= 8A		80	100	mΩ
V_{SD}	Diode Forward Voltage	I_S=8A, V_{GS}=0V		0.9	1.1	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=50V, V_{GS}=10V, I_D=8A		15.5		nC
Qgs	Gate-Source Charge			2.6		
Qgd	Gate-Drain Charge			3.6		
Ciss	Input Capacitance	V_{DS}=15V,V_{GS}=0V,f=1MHz		314		pF
Coss	Output Capacitance			119		
Crss	Reverse Transfer Capacitance			15		
td(on)	Turn-On Delay Time	V_{DS}=50V, R_L =50Ω, V_{GS}=10V, R_G=1Ω I_D=1A		8.4		ns
tr	Turn-On Rise Time			24.8		
td(off)	Turn-Off Delay Time			30.7		
tf	Turn-Off Fall Time			2.5		
Trr	Reverse Recovery Time	I_D=7A,V_{GS}=0V,di/dt=100A/us		25		ns
Qrr	Reverse Recovery Charge			24		nC

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed b7y design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve produc2.6t design, functions and reliability without notice.

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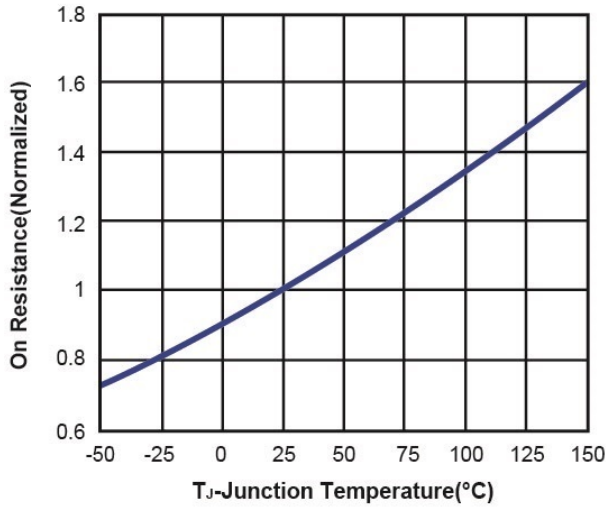
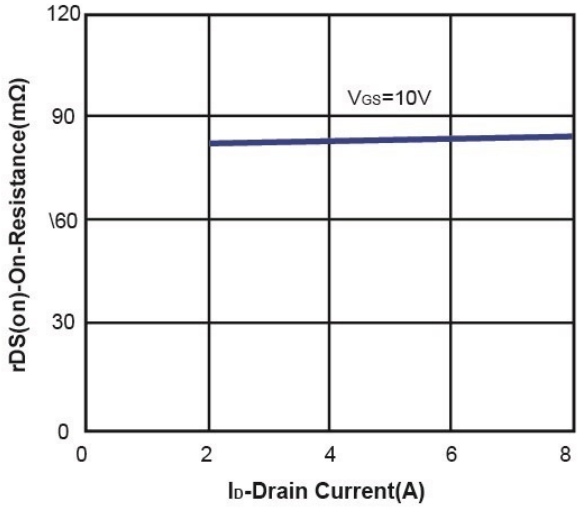
Typical Characteristics (T_J =25℃ Noted)

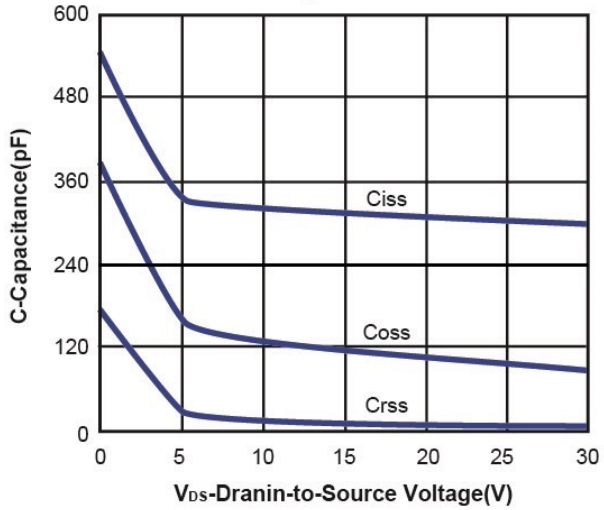
On Resistance vs. Junction Temperature



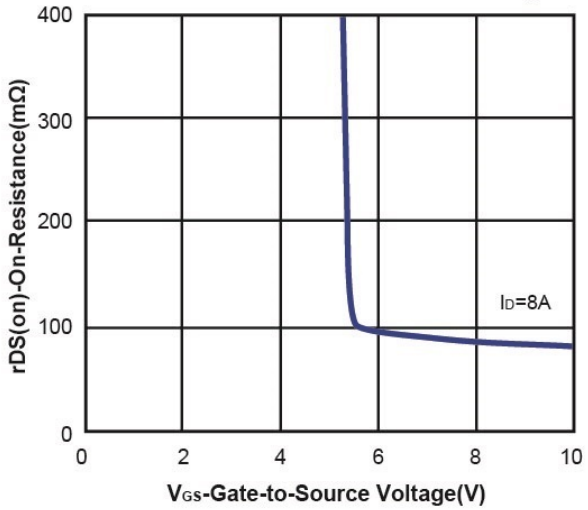
On Resistance vs. Drain Current



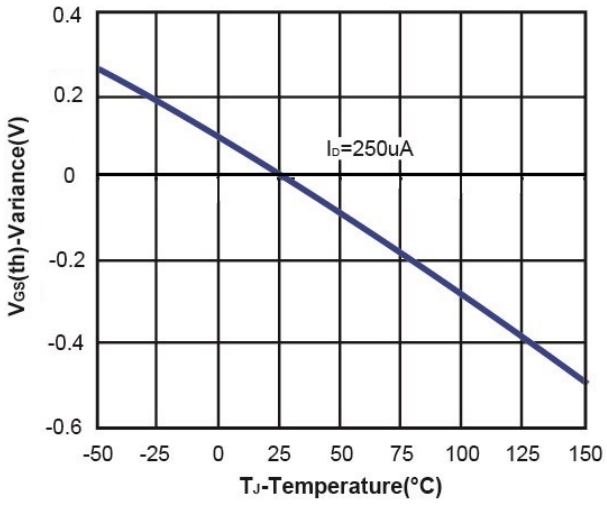
Capacitance



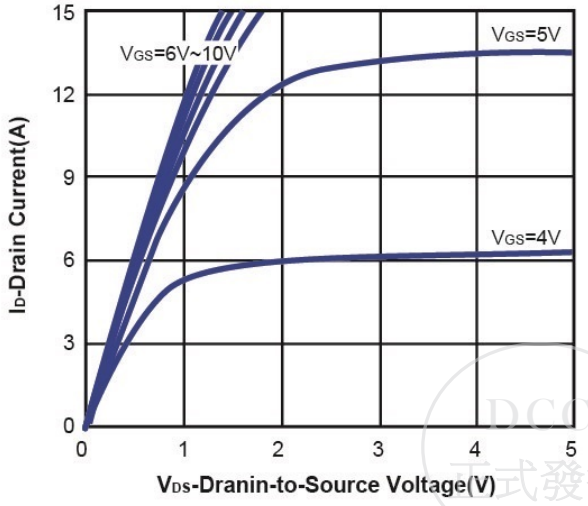
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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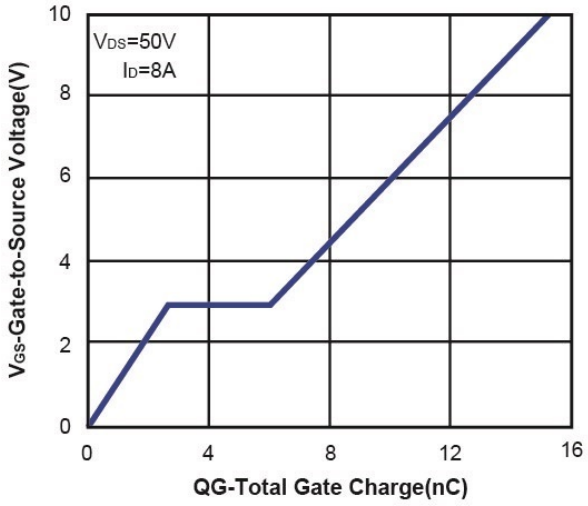
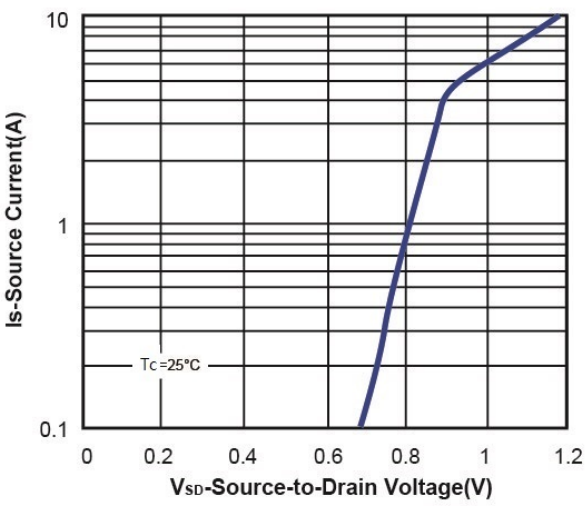
N-Channel 100-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

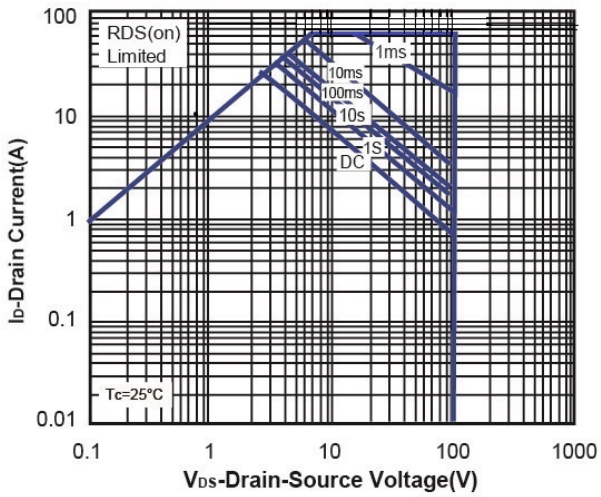
Gate Charge



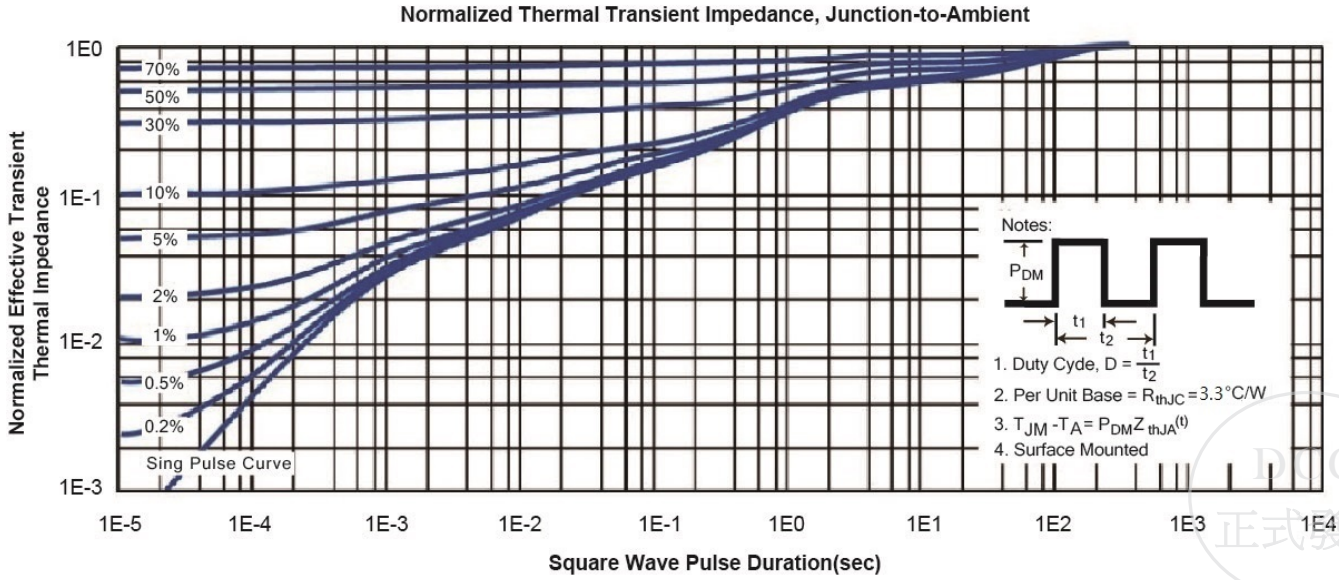
Body-diode characteristics



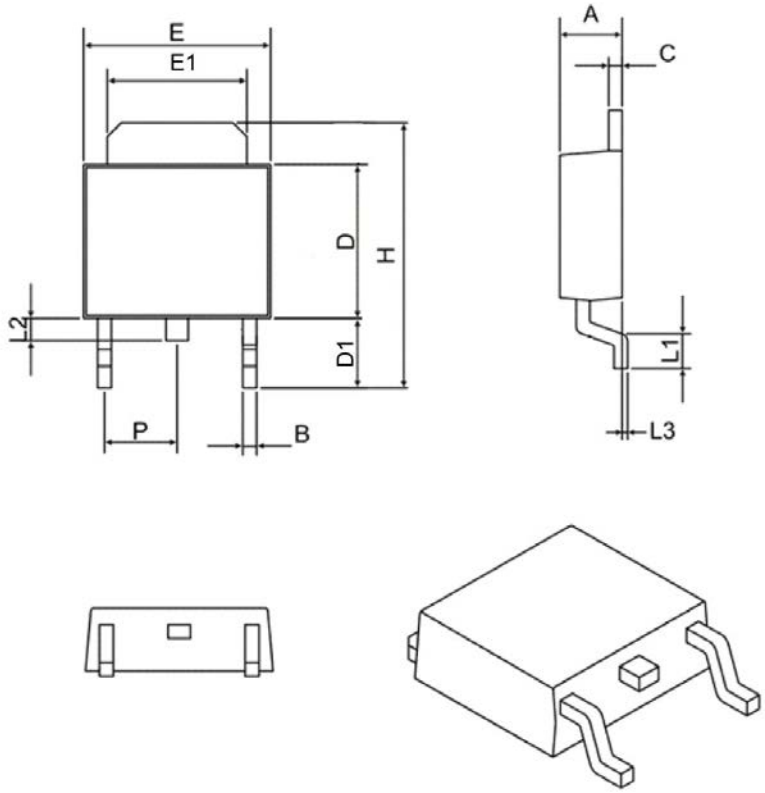
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



TO252-3L Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	

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