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SEMICONDUCTOR



ESD



TVS



TSS



MOV



GDT



PLED

74HC4052-MS

产品规格手册

概述

74HC4052-MS 是一款采用先进 CMOS 技术设计的两路差分四通道多路复用器。是一个单刀四掷配置形式的模拟开关。具有两个二进制通道控制输入(A 和 B) 以及一个使能输入 INH。两个二进制输入信号, 同时控制每路开关四个通道中的一个通道开启, 其余通道关闭。


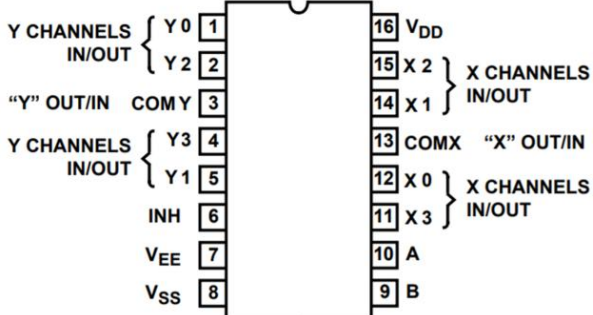
产品用途

- 模拟和数字多路复用与解复用
- 数字寻址信号的逻辑电平转换
- 信号选通
- 其它应用领域

特征

- 低输入电流: $I_{IN} \leq 1\mu A$, @ $V_{IN}=V_{DD}-V_{SS}=15V$, $T_a=25^\circ C$
- 低静态功耗: $I_{DD}=0.2\mu A$ (典型) @ $V_{DD}-V_{SS}=15V$, $T_a=25^\circ C$
- 低通电阻: 60Ω (典型) @ $V_{DD}-V_{SS}=V_{DD}-V_{EE}=15V$, $T_a=25^\circ C$
- 通道漏电流: $\pm 100nA$ (典型) @ $V_{DD}-V_{EE}=15V$
- 宽工作电压 $V_{DD}-V_{SS}$ 范围: $3V \sim 15V$
- 先断后通切换消除了通道重迭开启
- 单刀四掷配置形式的模拟开关

参考信息

封装图	脚位信息
	
SOP-16	管脚功能定义

封装形式和管脚功能定义

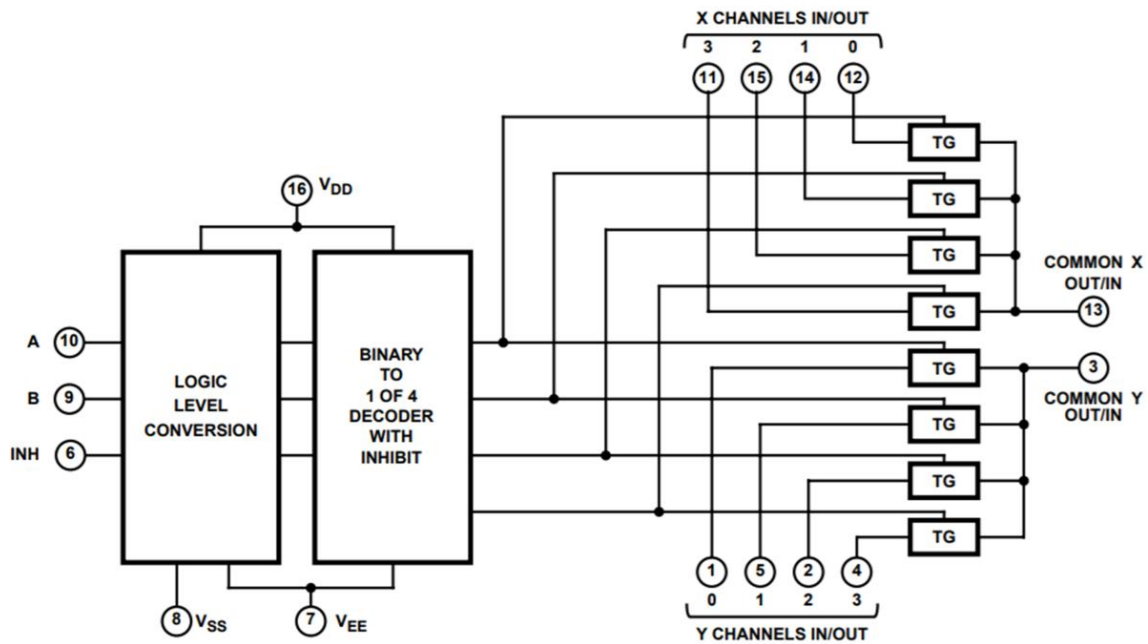
管脚序号	管脚定义	说明	管脚序号	管脚定义	说明
1	Y0	Y0 通道	16	V _{DD}	电源正
2	Y2	Y2 通道	15	X2	X2 通道
3	COM _Y	Y 通道公共端	14	X1	X1 通道
4	Y3	Y3 通道	13	COM _X	X 通道公共端
5	Y1	Y1 通道	12	X0	X0 通道
6	INH	使能控制	11	X3	X3 通道
7	V _{EE}	模拟开关负电源	10	A	地址输入 A
8	V _{SS}	电源地	9	B	地址输入 B

极限值

参数	符号	极限值	单位
直流电源电压	$V_{DD}-V_{SS}$	-0.5~18	V
模拟电源电压	$V_{DD}-V_{EE}$	18	V
直流输入电压	V_{IN}	-0.5+ V_{SS} ~ $V_{DD}+0.5V$	V
功耗	P_D	500	mW
工作温度	T_A	-40~85	°C
存储温度	T_S	-65~150	°C
引脚焊接温度	T_W	260, 10s	°C

注: 极限参数是指无论在任何条件下都不能超过的极限值。如果超过此极限值, 将有可能造成产品劣化等物理性损伤; 同时在接近极限参数下, 不能保证芯片可以正常工作。

原理逻辑图



真值表

INPUTS			OUTPUTS
INH	B	A	“ON” CHANNEL(S)
0	0	0	X0、Y0
0	0	1	X1、Y1
0	1	0	X2、Y2
0	1	1	X3、Y3
1	×	×	None

×:任意值

推荐工作条件

项目	符号	最小值	典型值	最大值	单位
直流电源电压	$V_{DD}-V_{SS}$	3		15	V
控制输入电压	V_{IS}	0		$V_{DD}-V_{SS}$	V
模拟电源电压	$V_{DD}-V_{EE}$	0		15	V
模拟输入输出电压	V_{IN} 、 V_{OUT}	0		$V_{DD}-V_{EE}$	V
工作温度	T_A	-40		85	°C

电学特性

直流电学特性: ($V_{IS}=V_{IN}-V_{SS}$, $V_{EE}=V_{SS}$, $R_L = 3k\Omega$, $T_A=25^\circ C$ 除非特别指定)

符号	项目	测试条件		VDD (V)	最小值	典型值	最大值	单位
V_{IH}	高电平有效 输入电压	$V_{IH}=V_{DD}$ through 1k	$V_{EE}=V_{SS}$, $R_L=1k\Omega$ to V_{SS} ,	5	3.5			V
				10	7			V
				15	11			V
V_{IL}	低电平有效 输入电压	$V_{IL}=V_{DD}$ through 1k	$I_{IS}<2\mu A$ on all OFF Channels	5			1.5	V
				10			3	V
				15			4	V
R_{ON}	导通电阻	$0 \leq V_{IS} \leq V_{DD}$		5		155		Ω
				10		85		
				15		60		
ΔR_{ON}	相邻通道导通电 阻差			5		15		Ω
				10		10		
				15		5		
I_{OFF}	漏电流	输入输出通道关闭, $INH=V_{DD}$		18			± 100	nA
I_{IN}	输入电流	$V_{IN}=V_{DD}$ or V_{SS}		18		0.01	± 0.1	μA
I_{DD}	静态电流	$V_{IN}=V_{DD}$ or V_{SS}		5		0.01	5	μA
				10		0.01	10	μA
				15		0.01	20	μA
C_{IN}	输入电容	任意输入端				5	7.5	pF
C_{IS}	通道输入电容					5		pF
C_{OS}	输出电容					9		pF
C_{IOS}	导通电容					0.2		pF

交流电学特性: ($V_{SS}=V_{EE}$, $T_A=25^\circ C$, $t_r=t_f=20ns$, t_{pd} 包含 t_{PHL} 、 t_{PLH} , 见测试方法, 除非特别指定)

项目	符号	测试条件	VDD	最小值	典型值	最大值	单位
传输延迟时间 Signal Input to Output	t_{pd}	$V_{IS}=V_{DD}$, $R_L=200k$, $CL=50pF$	5		15		ns
			10		10		ns
			15		7		ns
传输延迟时间 Address-to-Signal OUT (Channels ON or OFF)	t_{pd}	$CL=50pF$, $R_L=10k$	5		100		ns
			10		80		ns
			15		50		ns

交流电学特性: (Continues,)

项目	符号	测试条件	VDD	最小值	典型值	最大值	单位
传输延迟时间 Inhibit-to-Signal OUT (Channel Turning ON)	t _{pd}	C _L =50pF, R _L =1k	5		100		ns
			10		50		ns
			15		30		ns
传输延迟时间 Inhibit-to-Signal OUT (Channel Turning OFF)	t _{pd}	C _L =50pF, R _L =10k	5		100		ns
			10		50		ns
			15		30		ns

测试方法

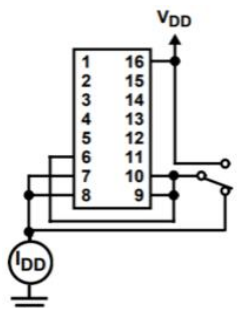


Fig.1 静态电流

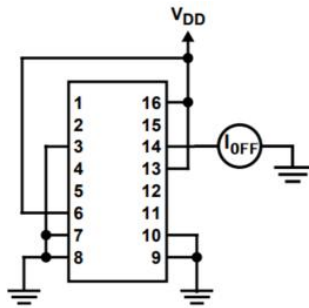


Fig.2 相邻通道关闭漏电流

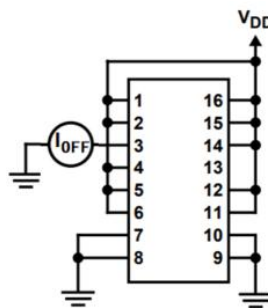


Fig.3 所有通道关闭漏电流

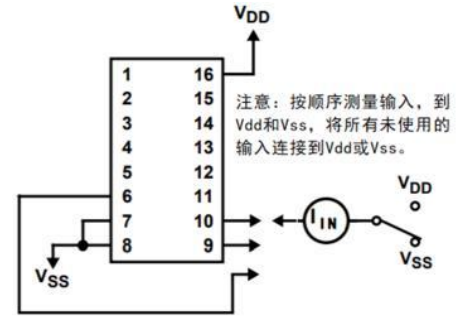


Fig.4 输入电流

注意：按顺序测量输入，到VDD和VSS，将所有未使用的输入连接到VDD或VSS。

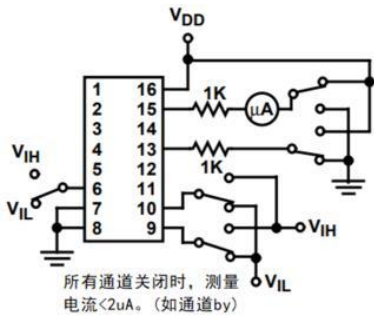


Fig.5 输入逻辑电平电压

所有通道关闭时，测量电流<2uA。(如通道by)

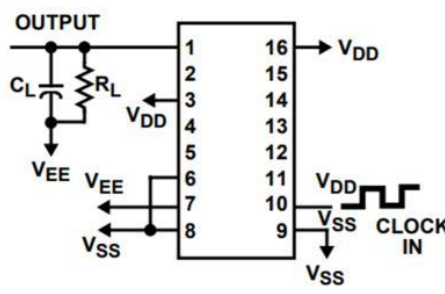


Fig.6 传播延迟-通道控制输入 to 开关输出

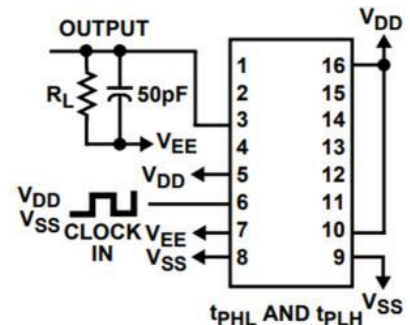


Fig.7 传播延迟-使能输入 to 开关输出

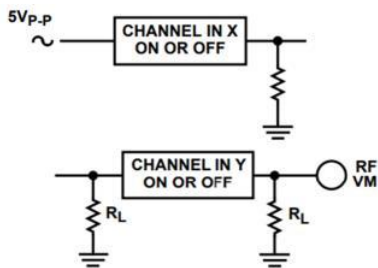


Fig.8 相邻通道之间信号串扰

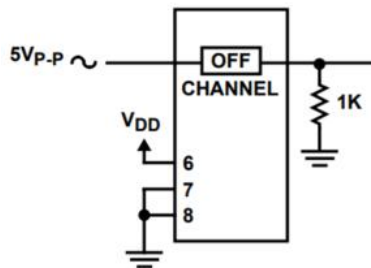


Fig.8 所有通道关闭信号串扰

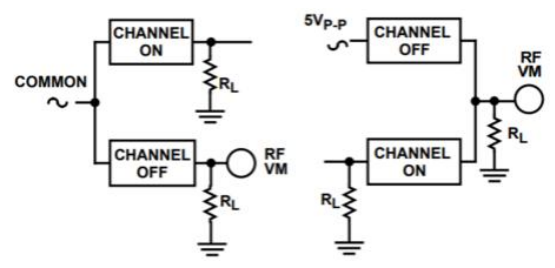
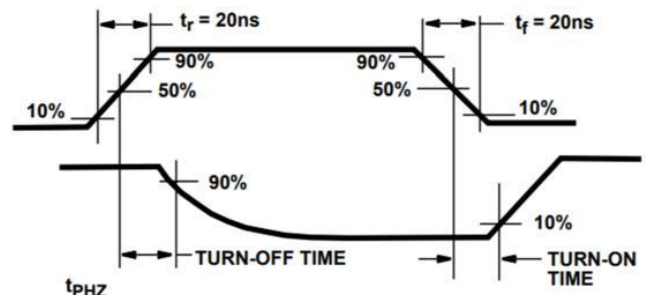
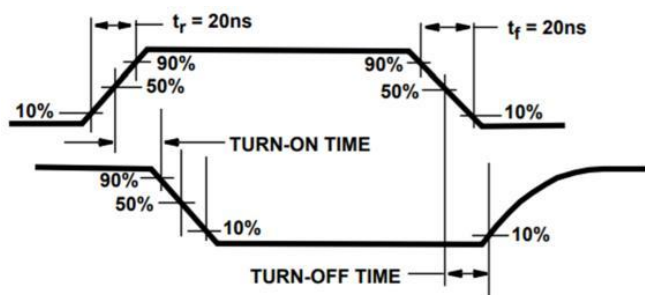


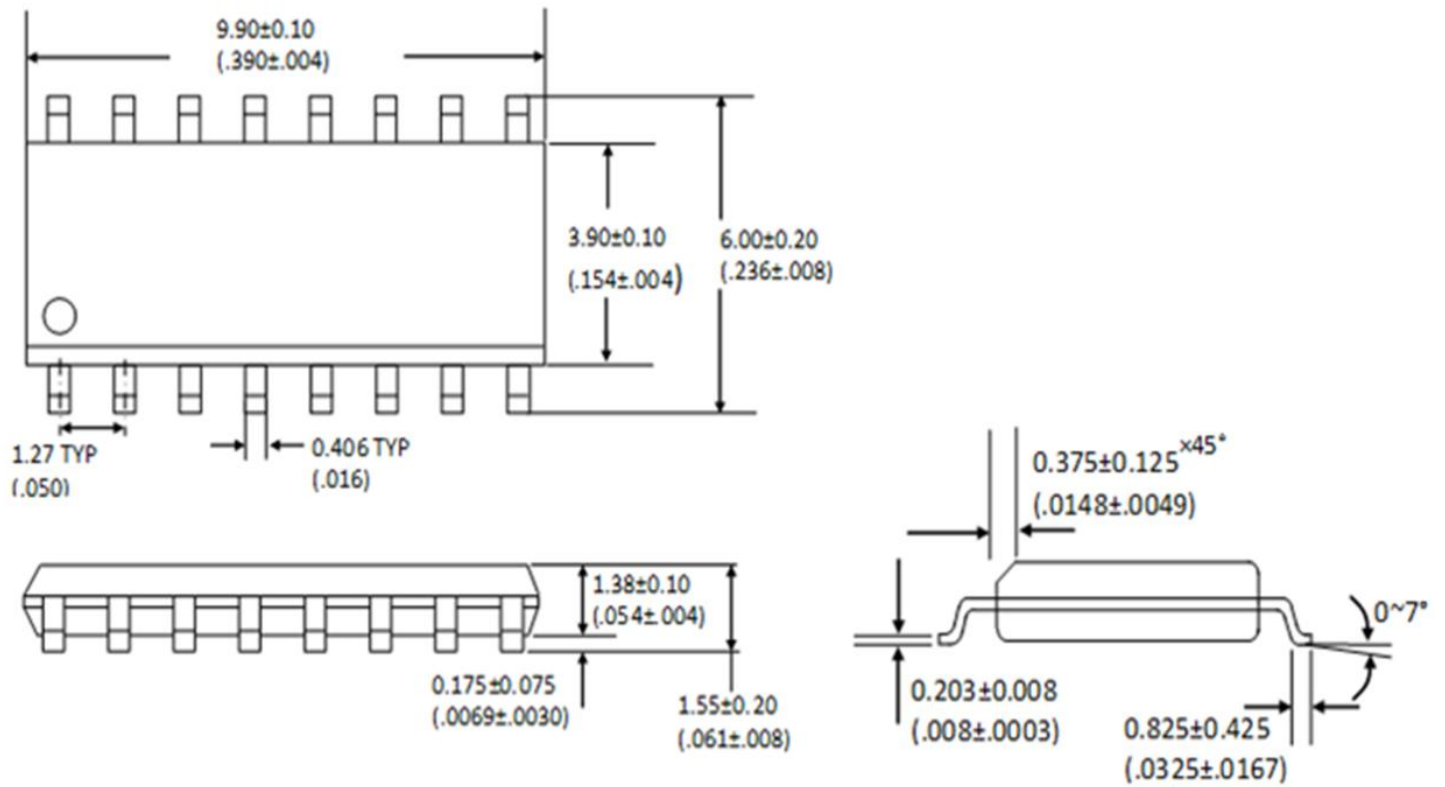
Fig.9 同一通道信号串扰

波形测量示意图



SOP-16 包装数据

单位：毫米 / 英寸



卷轴规格

P/N	PKG	QTY
74HC4052-MS	SOP-16	2500

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