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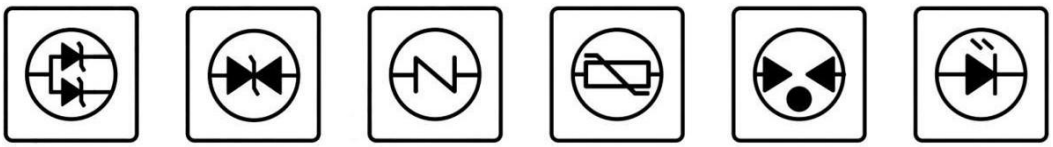
SEMICONDUCTOR



74HC4053-MS

产品规格手册

概述

74HC4053-MS 是一款采用先进 CMOS 技术设计的 3 路双通道多路模拟复用器。是一个单刀双掷配置形式的模 拟开关。具有三个独立的通道控制输入 A、B、C 和一个使能输入 INH。通道控制输入信号 A、B、C，分别 控制 3 路开关两个通道中的一个通道开启，另一通道关闭。

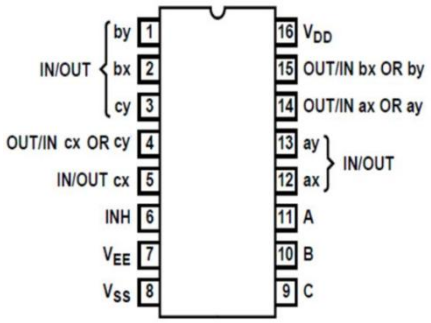
特征

- 低输入电流：IIN ≤1uA, @VIN=VDD-VSS=15V,Ta=25℃
- 低静态功耗：IDD=0.2uA(典型)@VDD-VSS=15V,Ta=25℃
- 低通电阻： 90Ω (典型)@VDD-VSS=VDD-VEE=15V,Ta=25℃
- 通道漏电流： ±100pA(典型) @VDD-VEE=15V
- 宽工作电压 VDD-VSS 范围： 3V~15V
- 先断后通切换消除了通道重迭开启
- 单刀双掷配置形式的模拟开关

产品用途

- 模拟和数字多路复用与解复用
- 数字寻址信号的逻辑电平转换
- 路复用与解复用
- 其它应用领域

参考信息

封装图	脚位信息
	
SOP-16	管脚功能定义

封装形式和管脚功能定义

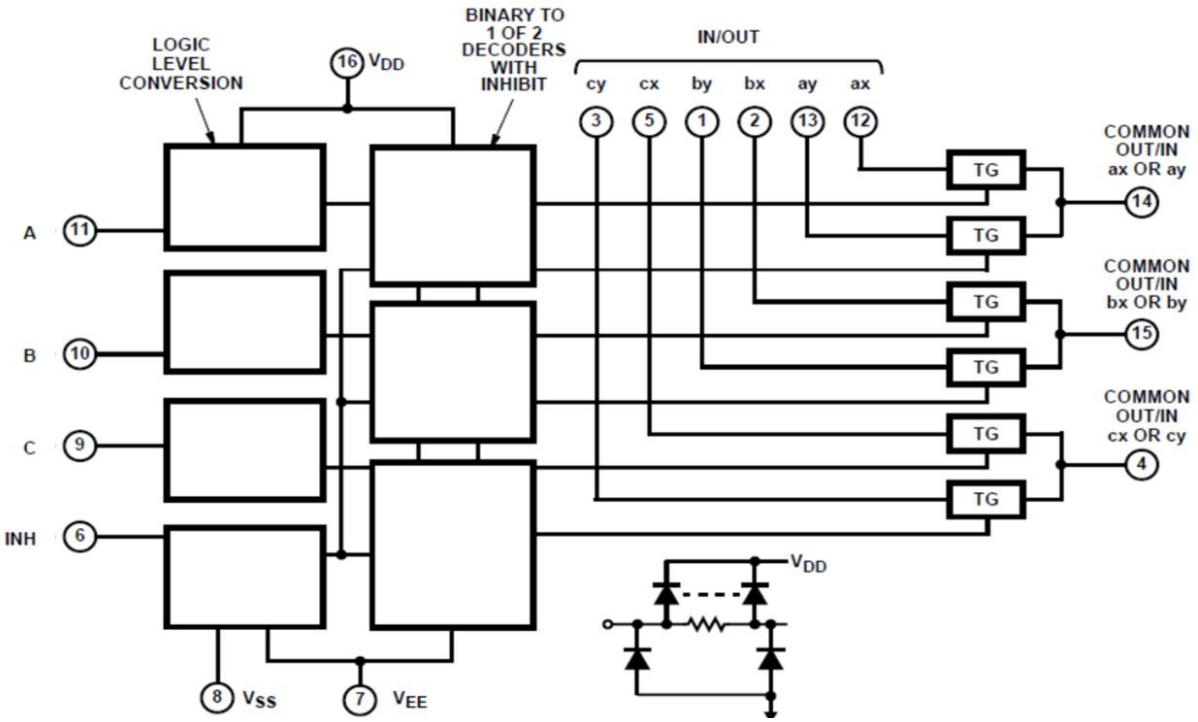
管脚序号	管脚定义	说明	管脚序号	管脚定义	说明
1	IN/OUT by	by 通道	16	VDD	电源正
2	IN/OUT bx	bx 通道	15	OUT/IN bx OR by	b 通道公共端
3	IN/OUT cy	cy 通道	14	OUT/IN ax OR ay	a 通道公共端
4	OUT/IN cx OR cy	c 通道公共端	13	IN/OUT ay	ay 通道
5	IN/OUT cx	cx 通道	12	IN/OUT ax	ax 通道
6	INH	使能控制	11	A	通道控制输入 A
7	VEE	模拟开关负电源	10	B	通道控制输入 B
8	VSS	电源地	9	C	通道控制输入 C

极限值

参数	符号	极限值	单位
直流电源电压	V_{DD}-V_{SS}	-0.5~18	V
模拟电源电压	V_{DD}-V_{EE}	18	V
直流输入电压	V_{IN}	-0.5+V_{SS}~V_{DD}+0.5V	V
功耗	P_D	500	mW
工作温度	T_A	-40~85	℃
存储温度	T_S	-65-150	℃
引脚焊接温度	T_W	260,10s	℃

注：极限参数是指无论在任何条件下都不能超过的极限值。如果超过此极限值，将有可能造成产品劣化等物理性损伤； 同时在接近极限参数下，不能保证芯片可以正常工作。

原理逻辑图



真值表

INPUTS		OUTPUTS
INH	A or B or C	“ON” CHANNEL
0	0	ax or bx or cx
0	1	ay or by or cy
1	×	None

×:任意值

推荐工作条件

项目	符号	最小值	典型值	最大值	单位
直流电源电压	$V_{DD}-V_{SS}$	3		15	V
控制输入电压	V_{IS}	0		$V_{DD}-V_{SS}$	V
模拟电源电压	$V_{DD}-V_{EE}$	0		15	V
模拟输入输出电压	V_{IN}、V_{OUT}	0		$V_{DD}-V_{EE}$	V
工作温度	T_A	-40		85	℃

电学特性

直流电学特性： ($V_{IS}=V_{IN}-V_{SS}$, $V_{EE}=V_{SS}$, RL = 3kΩ, T_A=25℃ 除非特别指定)

符号	项目	测试条件		VDD (V)	最小值	典型值	最大值	单位
V_{IH}	高电平有效输入电压	$V_{IH}=V_{DD}$ through 1k	$V_{EE}=V_{SS}$, RL=1kΩ to V_{SS}, I_{IS}<2uA on all OFF Channels	5	3.5			V
				10	7			V
				15	11			V
V_{IL}	低电平有效输入电压	$V_{IL}=V_{DD}$ through 1k		5			1.5	V
				10			3	V
				15			4	V
R_{ON}	导通电阻	0≤V_{IS}≤V_{DD}		5		180		Ω
				10		115		
				15		90		
△R_{ON}	相邻通道导通电阻差			5		15		Ω
				10		10		
				15		5		
I_{OFF}	漏电流	输入输出通道关闭, INH=V_{DD}		18			±100	nA
I_{IN}	输入电流	$V_{IN}=V_{DD}$ or V_{SS}		18		0.01	±0.1	uA
I_{DD}	静态电流	$V_{IN}=V_{DD}$ or V_{SS}		5		0.01	5	uA
				10		0.01	10	uA
				15		0.01	20	uA
C_{IN}	输入电容	任意输入端				5	7.5	pF
C_{IS}	通道输入电容					5		pF
C_{OS}	输出电容					9		pF
C_{IOS}	导通电容					0.2		pF

交流电学特性： ($V_{SS}=V_{EE}$, Ta=25℃, tr=tf=20ns, tpd 包含 t_{PHL}、t_{PLH}, 见测试方法, 除非特别指定

项目	符号	测试条件	VDD	最小值	典型值	最大值	单位
传输延迟时间 Signal Input to Output	tpd	$V_{IS}=V_{DD}$, RL=200k, CL=50pF	5		15		ns
			10		10		ns
			15		7		ns
传输延迟时间 Address-to-Signal OUT (Channels ON or OFF)	tpd	CL=50pF, RL=10k	5		100		ns
			10		80		ns
			15		50		ns

交流电学特性：　(Continues,)

项目	符号	测试条件	VDD	最小值	典型值	最大值	单位
传输延迟时间 Inhibit-to-Signal OUT (Channel Turning ON)	tpd	C_L=50pF, R_L=1k	5		100		ns
			10		50		ns
			15		30		ns
传输延迟时间 Inhibit-to-Signal OUT (Channel Turning OFF)	tpd	C_L=50pF, R_L=10k	5		100		ns
			10		50		ns
			15		30		ns

测试方法

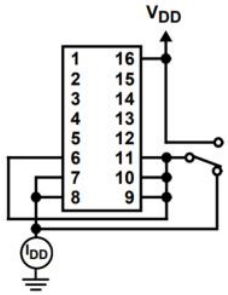


Fig.1 静态电流

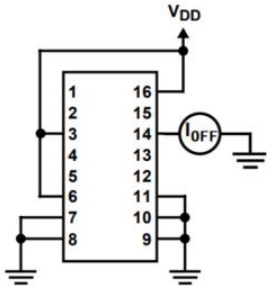


Fig.2 相邻通道关闭漏电流

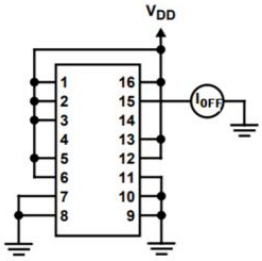


Fig.3 所有通道关闭漏电流

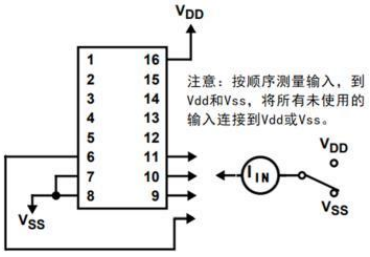


Fig.4 输入电流

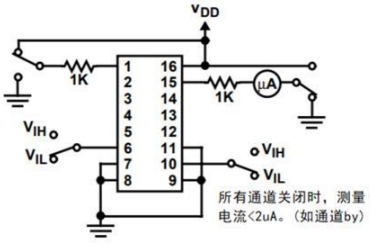


Fig.5 输入逻辑电平电压

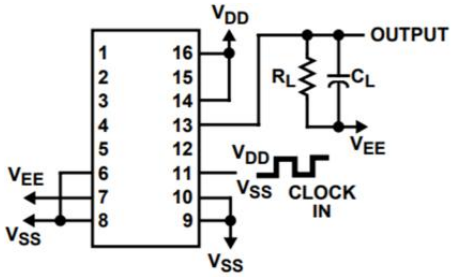


Fig.6 传播延迟-通道控制输入 to 开关输出

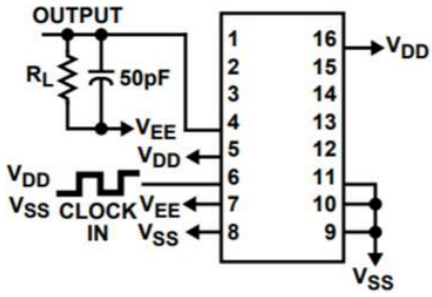


Fig.7 传播延迟-使能输入 to 开关输出

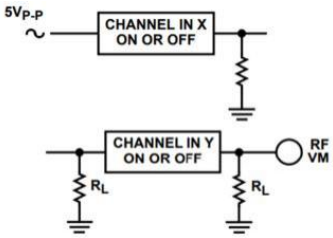


Fig.8 相邻通道之间信号串扰

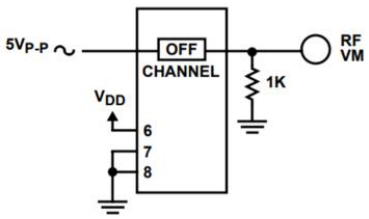


Fig.9 所有通道关闭信号串扰

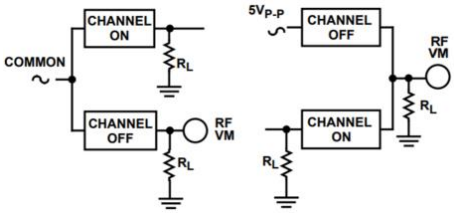
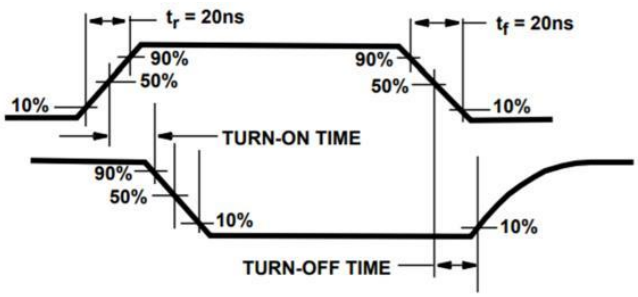
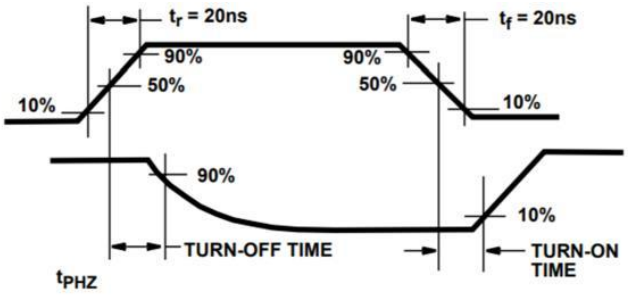


Fig.10 同一通道信号串扰

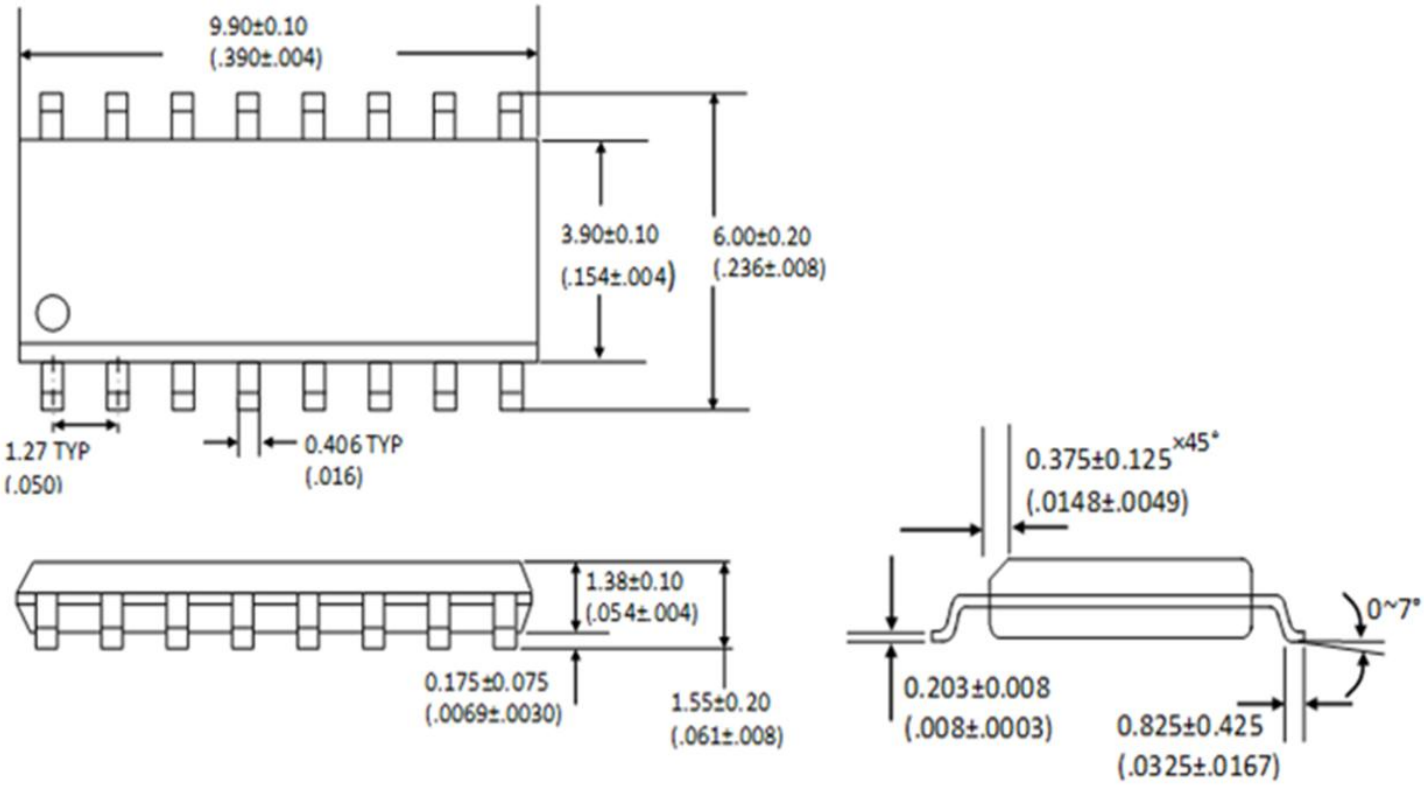
波形测量示意图





SOP-16 包装数据

单位：毫米 / 英寸



卷轴规格

P/N	PKG	QTY
74HC4053-MS	SOP-16	2500

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