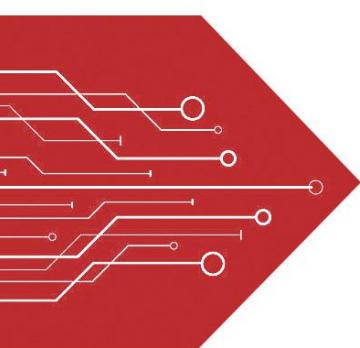


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SEMICONDUCTOR



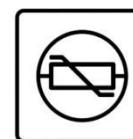
ESD



TVS



TSS



MOV



GDT



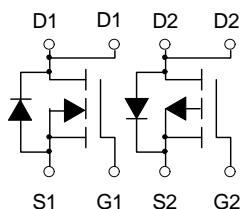
PLED

Product data sheet

Description



SOP-8



N-Channel and P-Channel

The AO4612-MS is the high performance complementary N-ch and P-ch MOSFETs with high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The AO4612-MS meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

BVDSS	RDSON	ID
60V	60mΩ	5.0A
-60V	100mΩ	-4.0A

- ★ Super Low Gate Charge
- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Channel	P-Channel	
V _{DS}	Drain-Source Voltage	60	-60	V
V _{GS}	Gate-Source Voltage	±20	±20	V
I _D @T _A =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	5.0	-4.0	A
I _D @T _A =70°C	Continuous Drain Current, V _{GS} @ 10V ¹	3.8	-3	A
I _{DM}	Pulsed Drain Current ²	9.6	-7.5	A
EAS	Single Pulse Avalanche Energy ³	25.5	35.3	mJ
I _{AS}	Avalanche Current	22.6	-26.6	A
P _D @T _A =25°C	Total Power Dissipation ⁴	1.5	1.5	W
T _{STG}	Storage Temperature Range	-55 to 150	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	85	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	36	°C/W

N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$\text{V}_{\text{GS}}=0\text{V}$, $\text{I}_D=250\mu\text{A}$	60	---	---	V
$\Delta \text{BV}_{\text{DSS}}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $\text{I}_D=1\text{mA}$	---	0.063	---	$\text{V}/^\circ\text{C}$
$\text{R}_{\text{DS(ON)}}$	Static Drain-Source On-Resistance ²	$\text{V}_{\text{GS}}=10\text{V}$, $\text{I}_D=4\text{A}$	---	60	80	$\text{m}\Omega$
		$\text{V}_{\text{GS}}=4.5\text{V}$, $\text{I}_D=2\text{A}$	---	80	100	
$\text{V}_{\text{GS(th)}}$	Gate Threshold Voltage	$\text{V}_{\text{GS}}=\text{V}_{\text{DS}}$, $\text{I}_D=250\mu\text{A}$	1.2	---	2.5	V
$\Delta \text{V}_{\text{GS(th)}}$	$\text{V}_{\text{GS(th)}}$ Temperature Coefficient		---	-5.24	---	$\text{mV}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$\text{V}_{\text{DS}}=48\text{V}$, $\text{V}_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	uA
		$\text{V}_{\text{DS}}=48\text{V}$, $\text{V}_{\text{GS}}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$\text{V}_{\text{GS}}=\pm 20\text{V}$, $\text{V}_{\text{DS}}=0\text{V}$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$\text{V}_{\text{DS}}=5\text{V}$, $\text{I}_D=4\text{A}$	---	21	---	S
R_{g}	Gate Resistance	$\text{V}_{\text{DS}}=0\text{V}$, $\text{V}_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	3.2	---	Ω
Q_{g}	Total Gate Charge (4.5V)	$\text{V}_{\text{DS}}=12\text{V}$, $\text{V}_{\text{GS}}=10\text{V}$, $\text{I}_D=4\text{A}$	---	5.5	---	nC
Q_{gs}	Gate-Source Charge		---	1.8	---	
Q_{gd}	Gate-Drain Charge		---	2.4	---	
$\text{T}_{\text{d(on)}}$	Turn-On Delay Time	$\text{V}_{\text{DD}}=12\text{V}$, $\text{V}_{\text{GS}}=10\text{V}$, $\text{R}_{\text{G}}=3.3\Omega$, $\text{I}_D=4\text{A}$	---	6	---	ns
T_{r}	Rise Time		---	10	---	
$\text{T}_{\text{d(off)}}$	Turn-Off Delay Time		---	15	---	
T_{f}	Fall Time		---	7	---	
C_{iss}	Input Capacitance	$\text{V}_{\text{DS}}=15\text{V}$, $\text{V}_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	695	---	pF
C_{oss}	Output Capacitance		---	148	---	
C_{rss}	Reverse Transfer Capacitance		---	7	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{s}	Continuous Source Current ^{1,5}	$\text{V}_{\text{G}}=\text{V}_{\text{D}}=0\text{V}$, Force Current	---	---	5.0	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	9.6	A
V_{SD}	Diode Forward Voltage ²	$\text{V}_{\text{GS}}=0\text{V}$, $\text{I}_{\text{s}}=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $\text{V}_{\text{DD}}=25\text{V}$, $\text{V}_{\text{GS}}=10\text{V}$, $\text{L}=0.1\text{mH}$, $\text{I}_{\text{AS}}=5\text{A}$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_{D} and I_{DM} , in real applications , should be limited by total power dissipation.

P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$\text{V}_{\text{GS}}=0\text{V}$, $\text{I}_D=-250\mu\text{A}$	-60	---	---	V
$\Delta \text{BV}_{\text{DSS}}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $\text{I}_D=-1\text{mA}$	---	-0.049	---	$\text{V}/^\circ\text{C}$
$\text{R}_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance ²	$\text{V}_{\text{GS}}=-10\text{V}$, $\text{I}_D=-3\text{A}$	---	100	115	$\text{m}\Omega$
		$\text{V}_{\text{GS}}=-4.5\text{V}$, $\text{I}_D=-2\text{A}$	---	115	130	
$\text{V}_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$\text{V}_{\text{GS}}=\text{V}_{\text{DS}}$, $\text{I}_D=-250\mu\text{A}$	-1.2	---	-2.5	V
$\Delta \text{V}_{\text{GS}(\text{th})}$	$\text{V}_{\text{GS}(\text{th})}$ Temperature Coefficient		---	4.56	---	$\text{mV}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$\text{V}_{\text{DS}}=-48\text{V}$, $\text{V}_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	uA
		$\text{V}_{\text{DS}}=-48\text{V}$, $\text{V}_{\text{GS}}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$\text{V}_{\text{GS}}=\pm 20\text{V}$, $\text{V}_{\text{DS}}=0\text{V}$	---	---	$\pm 10_0$	nA
g_{fs}	Forward Transconductance	$\text{V}_{\text{DS}}=-5\text{V}$, $\text{I}_D=-3\text{A}$	---	5.8	---	S
R_g	Gate Resistance	$\text{V}_{\text{DS}}=0\text{V}$, $\text{V}_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	13.5	---	Ω
Q_g	Total Gate Charge (-4.5V)	$\text{V}_{\text{DS}}=-20\text{V}$, $\text{V}_{\text{GS}}=-4.5\text{V}$, $\text{I}_D=-3\text{A}$	---	5.9	---	nC
Q_{gs}	Gate-Source Charge		---	2.9	---	
Q_{gd}	Gate-Drain Charge		---	1.8	---	
$\text{T}_{\text{d(on)}}$	Turn-On Delay Time	$\text{V}_{\text{DD}}=-12\text{V}$, $\text{V}_{\text{GS}}=-10\text{V}$, $\text{R}_g=3.3\Omega$, $\text{I}_D=-3\text{A}$	---	10	---	ns
T_r	Rise Time		---	17	---	
$\text{T}_{\text{d(off)}}$	Turn-Off Delay Time		---	22	---	
T_f	Fall Time		---	21	---	
C_{iss}	Input Capacitance	$\text{V}_{\text{DS}}=-15\text{V}$, $\text{V}_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	715	---	pF
C_{oss}	Output Capacitance		---	51	---	
C_{rss}	Reverse Transfer Capacitance		---	34	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_s	Continuous Source Current ^{1,5}	$\text{V}_G=\text{V}_D=0\text{V}$, Force Current	---	---	-4.0	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	-7.5	A
V_{SD}	Diode Forward Voltage ²	$\text{V}_{\text{GS}}=0\text{V}$, $\text{I}_s=-1\text{A}$, $T_J=25^\circ\text{C}$	---	---	-1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $\text{V}_{\text{DD}}=-25\text{V}$, $\text{V}_{\text{GS}}=-10\text{V}$, $L=0.1\text{mH}$, $\text{I}_{\text{AS}}=-20.0\text{A}$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Channel Typical Characteristics

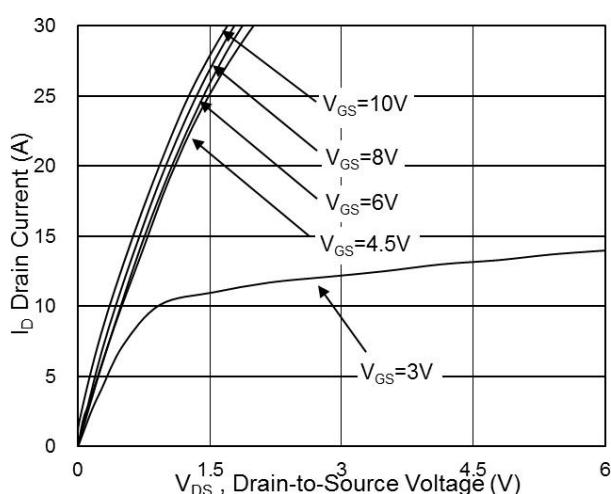


Fig.1 Typical Output Characteristics

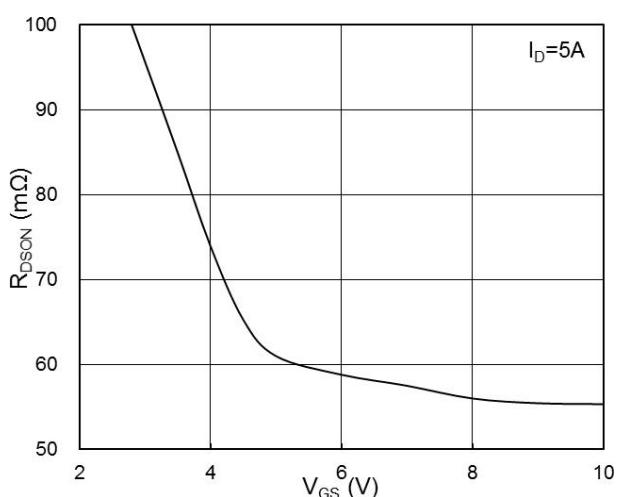


Fig.2 On-Resistance v.s Gate-Source

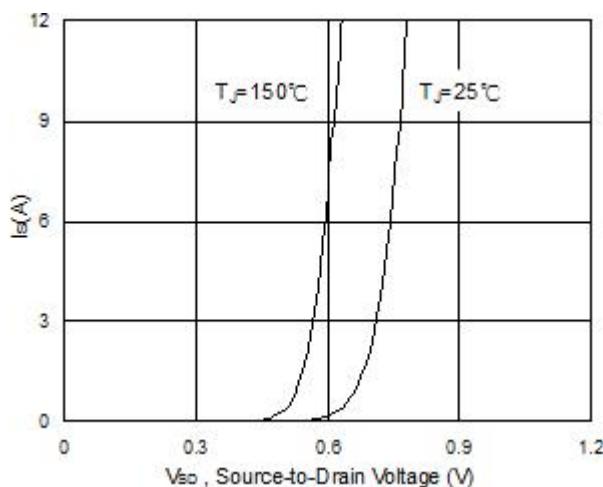


Fig.3 Forward Characteristics of Reverse

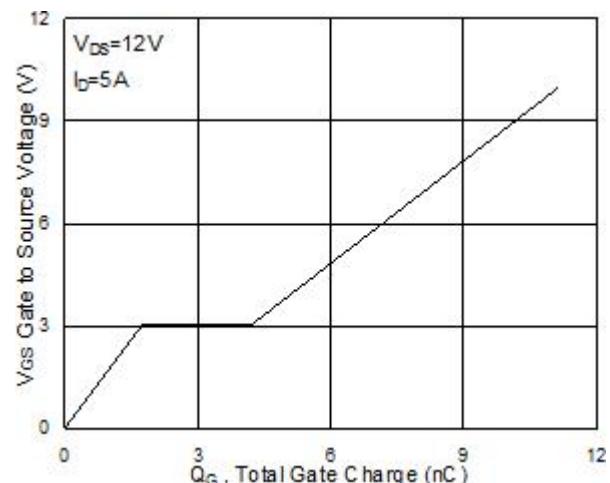


Fig.4 Gate-Charge Characteristics

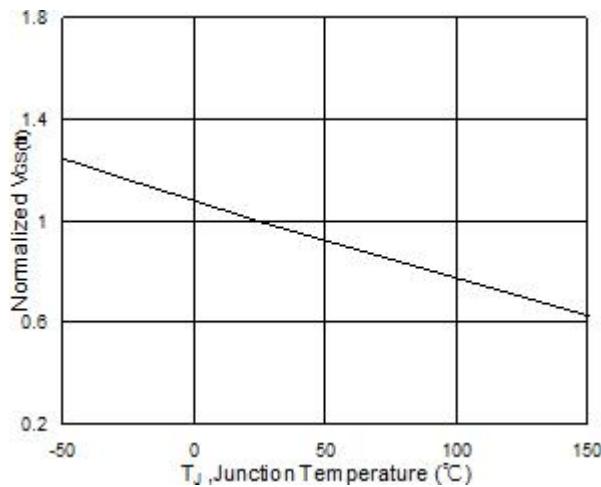


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

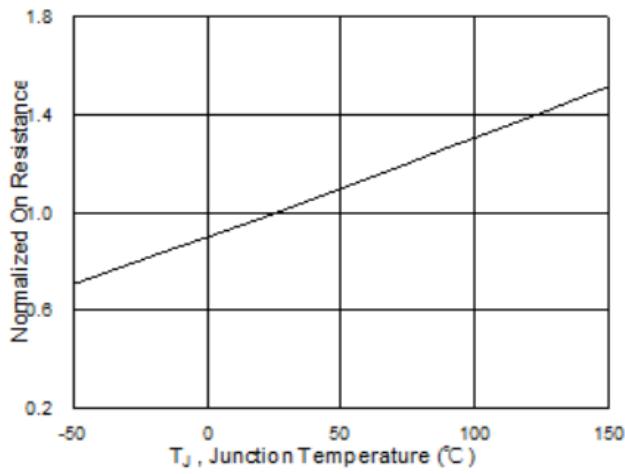


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

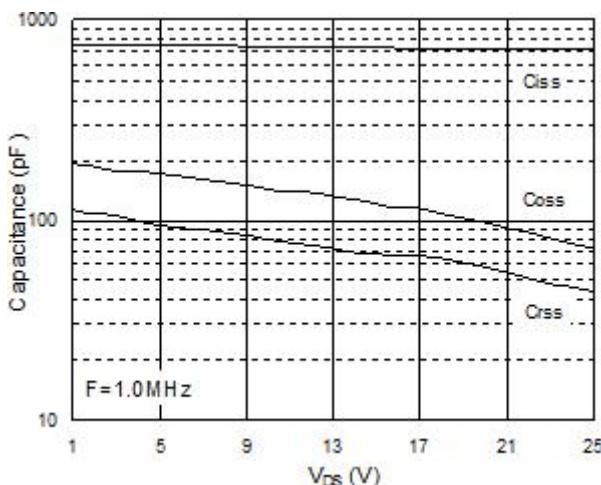


Fig.7 Capacitance

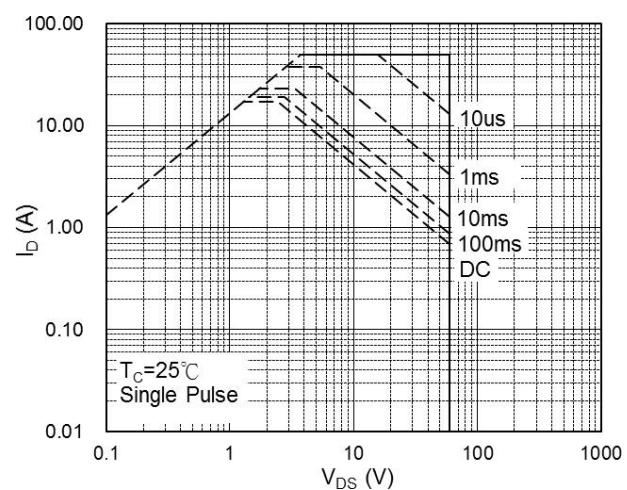


Fig.8 Safe Operating Area

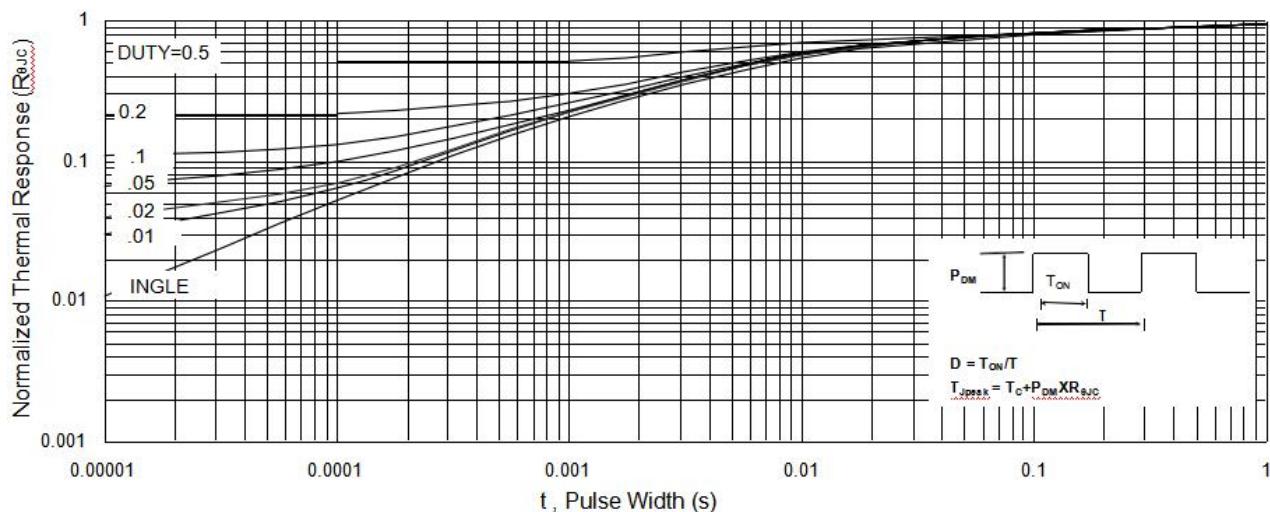


Fig.9 Normalized Maximum Transient Thermal Impedance

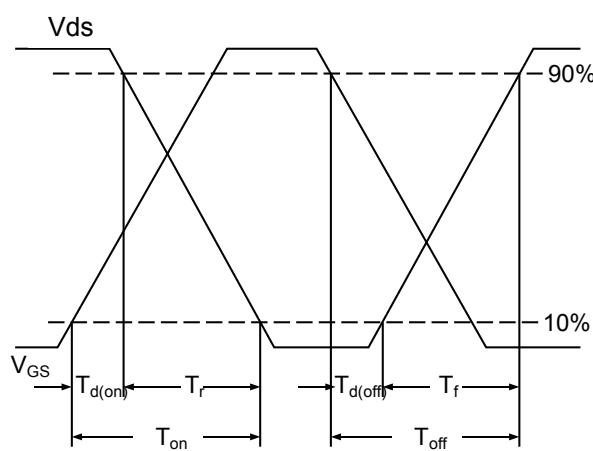


Fig.10 Switching Time Waveform

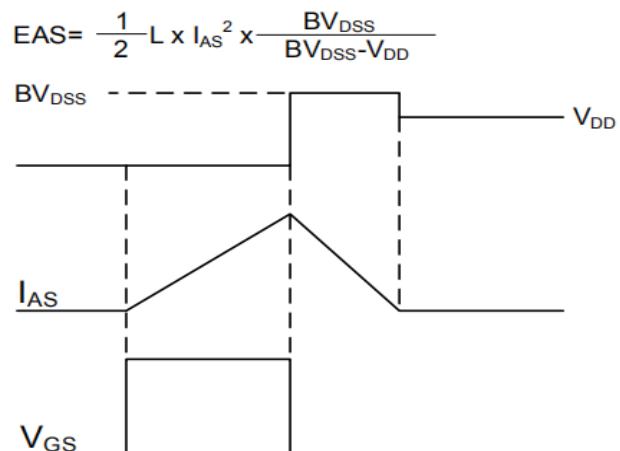


Fig.11 Unclamped Inductive Waveform

P-Channel Typical Characteristics

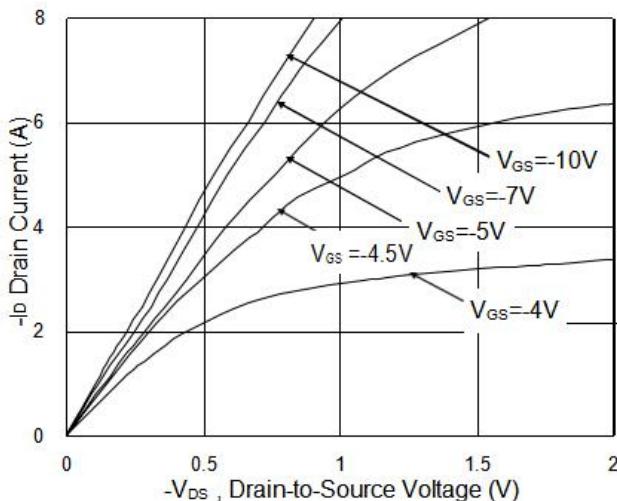


Fig.1 Typical Output Characteristics

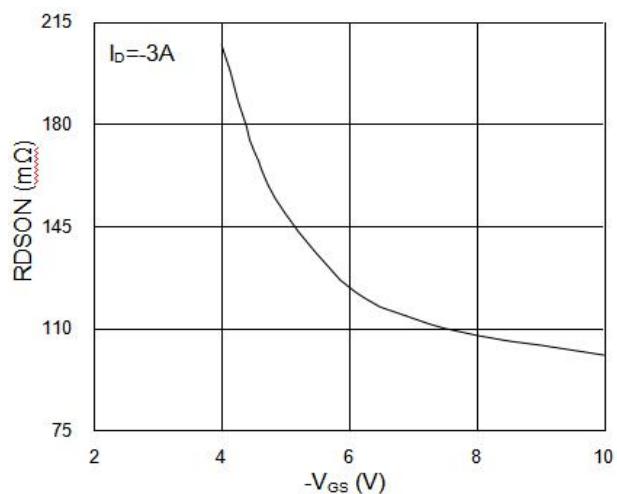


Fig.2 On-Resistance v.s Gate-Source

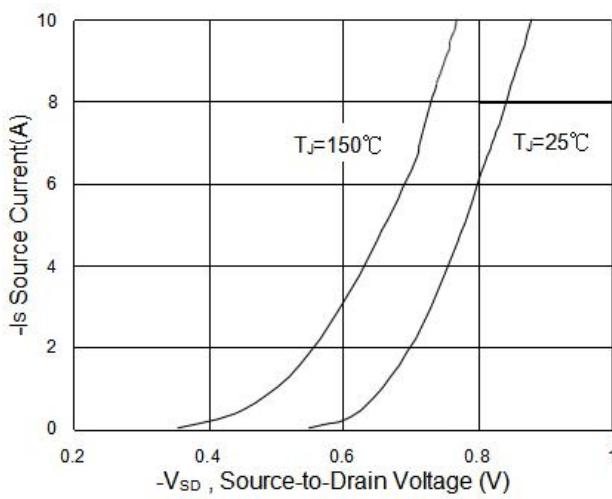


Fig.3 Forward Characteristics of Reverse

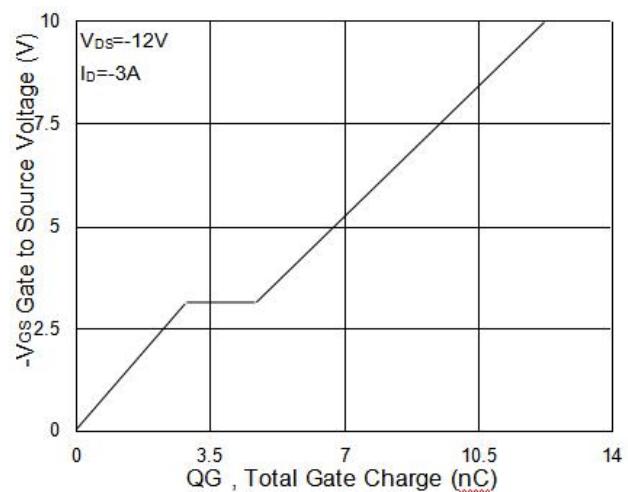


Fig.4 Gate-Charge Characteristics

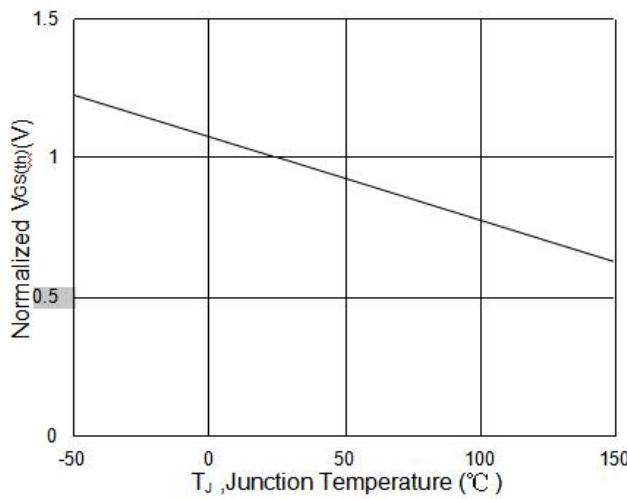


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

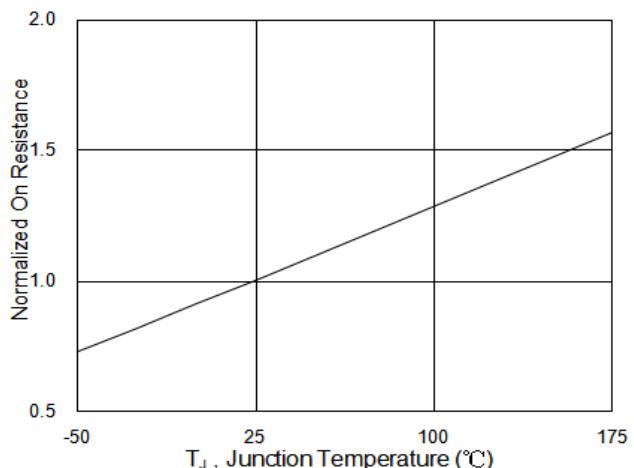


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

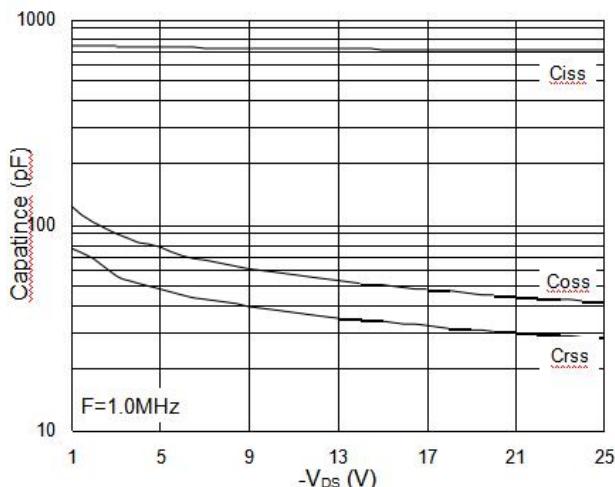


Fig.7 Capacitance

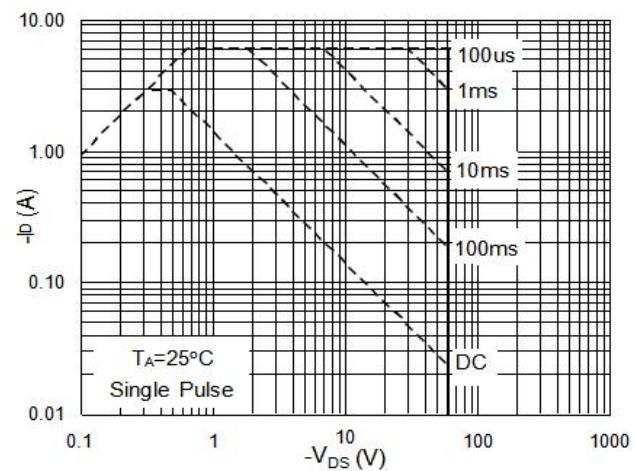


Fig.8 Safe Operating Area

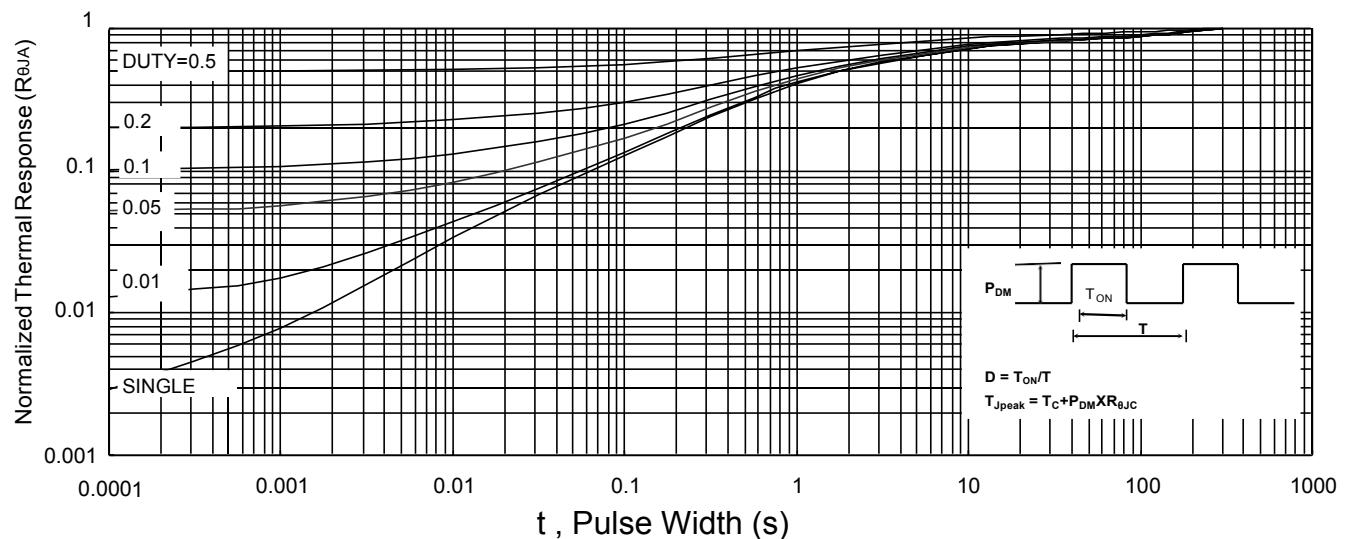


Fig.9 Normalized Maximum Transient Thermal Impedance

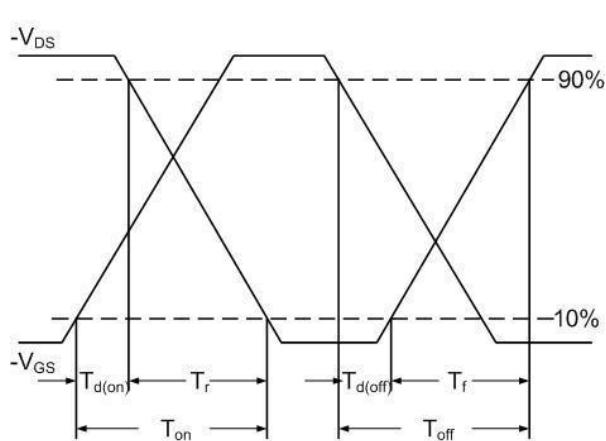


Fig.10 Switching Time Waveform

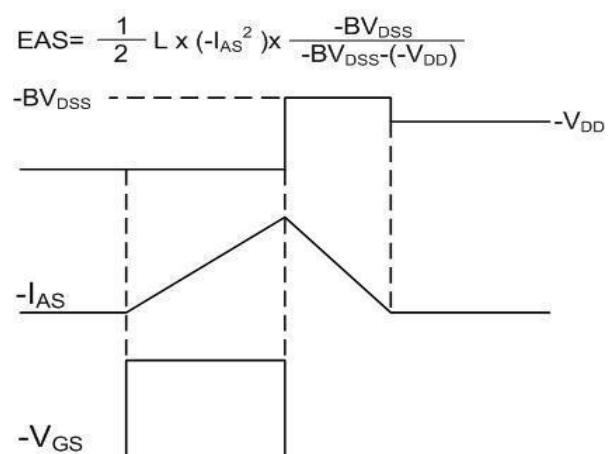
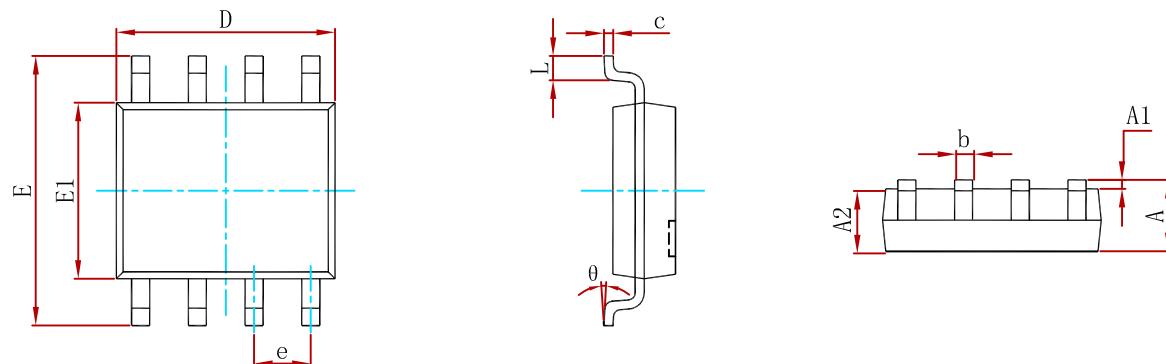


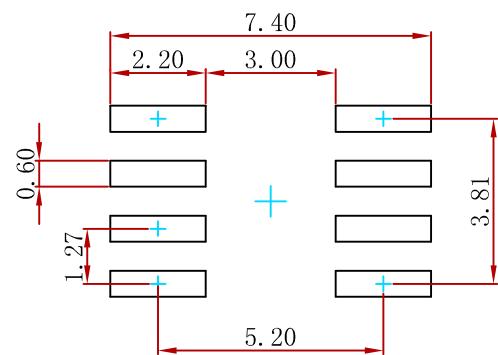
Fig.11 Unclamped Inductive Waveform

PACKAGE MECHANICAL DATA



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.

REEL SPECIFICATION

P/N	PKG	QTY
AO4612-MS	SOP-8	3000

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[BSS340NWH6327XTSA1](#) [MCM3400A-TP](#) [DMTH10H4M6SPS-13](#) [IRF40SC240ARMA1](#) [IPS60R1K0PFD7SAKMA1](#)
[IPS60R360PFD7SAKMA1](#) [IPS60R600PFD7SAKMA1](#)