

MSKSEMI 美森科

SEMICONDUCTOR



ESD



TVS



TSS



MOV



GDT



PLED

CD4069

产品规格手册

概述

CD4069 是一款采用先进 CMOS 技术设计的低功耗宽范围工作电压的反相器。它内部集成六组相互独立的反相器电路，具有高抗干扰能力和驱动能力

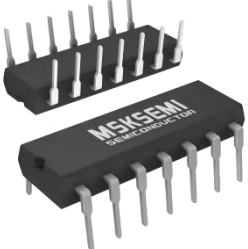
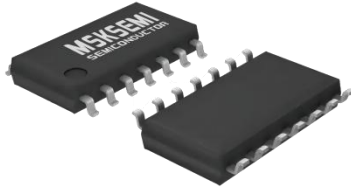
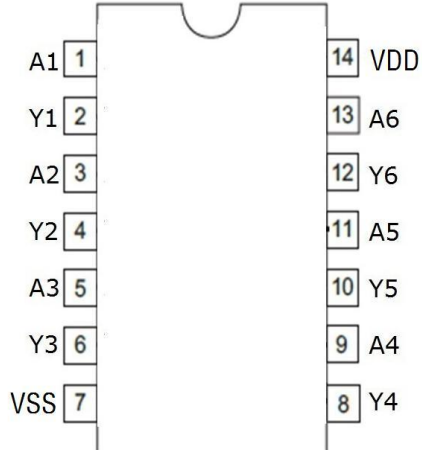
产品用途

- 数字逻辑驱动
- 无线门铃
- 工控应用
- 其它应用领域

特征

- 低输入电流： $I_{IN} \leq 1\mu A$, @ $V_{IN}=V_{DD}=15V, T_a=25^\circ C$
- 低静态功耗： $I_{DD} \leq 4\mu A$, @ $V_{DD}=15V, T_a=25^\circ C$
- 宽工作电压范围：3.0V to 15.0V
- 封装形式：DIP-14 、SOP-14

参考信息

封装图		脚位信息
		
DIP-14	SOP-14	DIP14/SOP14 管脚功能定义

封装形式和管脚功能定义

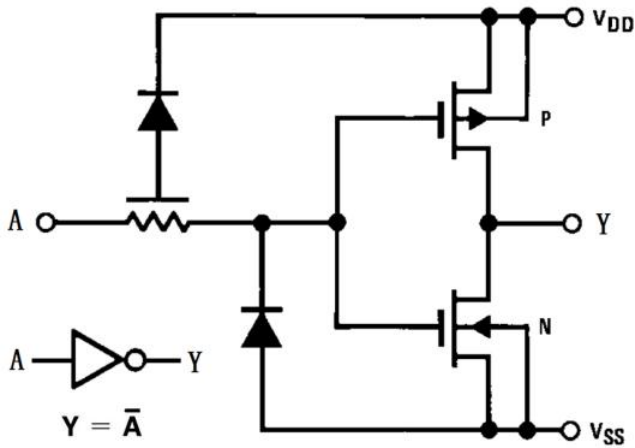
管脚序号	管脚定义	管脚序号	管脚定义
DIP14/SOP14		DIP14/SOP14	
1	A1	14	VDD
2	Y1	13	A6
3	A2	12	Y6
4	Y2	11	A5
5	A3	10	Y5
6	Y3	9	A4
7	VSS	8	Y4

极限值

参数	符号	极限值	单位
电源电压	V_{DD}	-0.5-18	V
输入电压	V_{IN}	-0.5+VSS- V_{DD} +0.5V	V
功耗	P_D	500	mW
工作温度	T_A	0-70	°C
存储温度	T_S	-65-150	°C
引脚焊接温度	T_W	260, 10s	°C

注: 极限参数是指无论在任何条件下都不能超过的极限值。如果超过此极限值, 将有可能造成产品劣化等物理性损伤; 同时在接近极限参数下, 不能保证芯片可以正常工作。

原理逻辑图



真值表

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

推荐工作条件

项目	符号	最小值	典型值	最大值	单位
工作电压	V _{DD}	2.5		15	V
输入输出电压	V _{IN} 、V _{out}	0		V _{DD}	V
工作温度	T _A	0		60	°C

电学特性
直流电学特性： TA=25°C

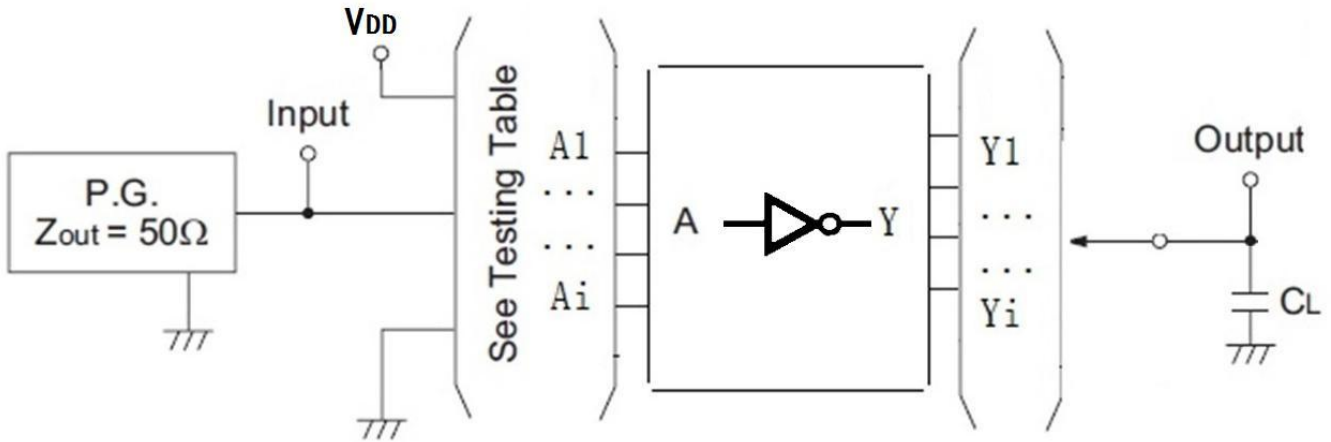
符号	项目	测试条件	VDD (V)	最小值	典型值	最大值	单位
V _{IH}	高电平有效 输入电压	I _O ≤ 1uA	V _O = 0.5V	5	4.0		V
			V _O = 1V	10	8.0		V
			V _O = 1.5V	15	12.0		V
V _{IL}	低电平有效 输入电压	I _O ≤ 1uA	V _O = 4.5V	5		1.0	V
			V _O = 9V	10		2.0	V
			V _O =13.5V	15		3.0	V
V _{OH}	高电平输出电压	I _{OUT} < 1uA	5	4.95			V
			10	9.95			V
			15	14.95			V
V _{OL}	低电平输出电压	I _{OUT} < 1uA	5		0	0.05	V
			10		0	0.05	V
			15		0	0.05	V
I _{IN}	输入电流	V _{IN} =V _{DD} or V _{SS}	15		0	1.0	uA
I _{OH}	高电平输出电流	V _O = 4.5V	5		-1.4	-0.45	mA
		V _O = 9V	10		-3.0	-1.2	mA
		V _O = 13.5V	15		-10	-3	mA
I _{OL}	低电平输出电流	V _O = 0.4V	5	0.45	3.3		mA
		V _O = 0.5V	10	1.0	12		mA
		V _O = 1.5V	15	3.0	24		mA
I _{DD}	工作电流	V _{IN} =V _{DD} or V _{SS}	5			1.0	uA
			10			2.0	uA
			15			4.0	uA

交流电学特性： Ta=25°C，见测试方法。

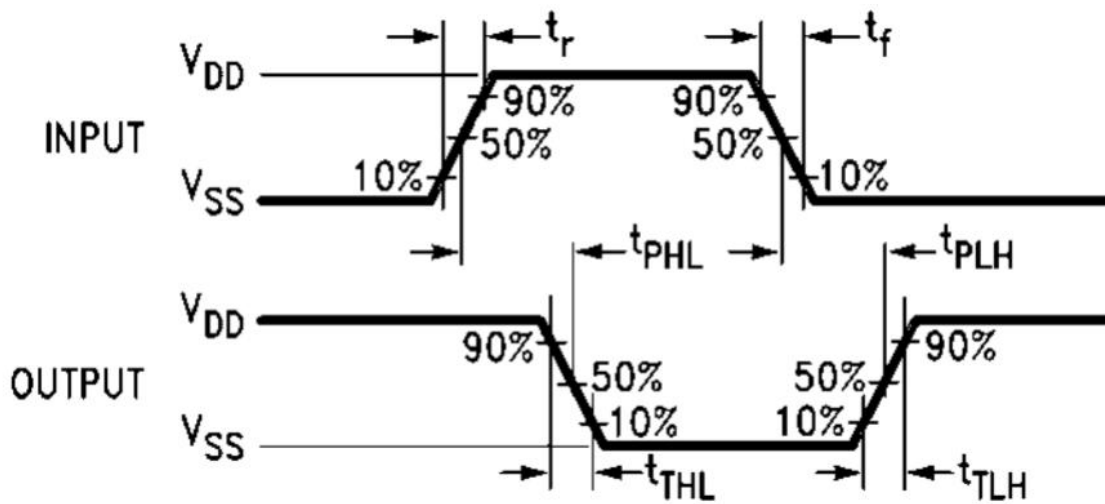
项目	符号	测试条件	最小值	典型值	最大值	单位
最大传输延迟时间 A to Y	t _{PHL}	VDD=5V C _L =51pF		32		ns
	t _{PLH}			42		ns
	t _{PHL}	VDD=10V C _L =51pF		23		ns
	t _{PLH}			32		ns
	t _{PHL}	VDD=15V C _L =51pF		25		ns
	t _{PLH}			27		ns

测试方法

1、测试接线图



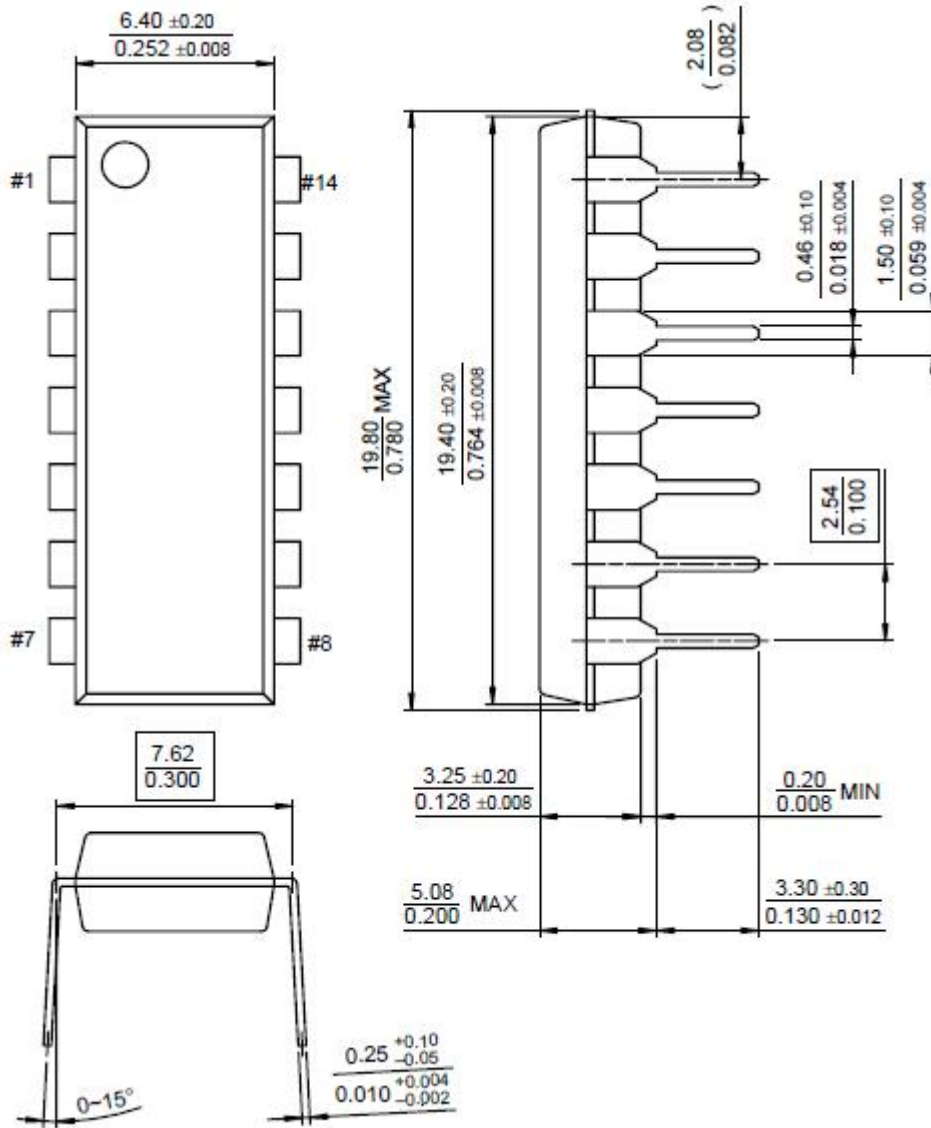
2、波形测量示意图



- 注：
- 1、 See Testing Table 指交流电学特性表中相应测试项目；
 - 2、 CL 电容为外接贴片电容(0603) ，靠近输出管脚接入，电容地靠近芯片 VSS；
 - 3、 Input: 端口输入电平， f=1MHz,D=50%方波， tr=tf ≤20ns；
 - 4、 Output: Y 端输出测试。

DIP-14 包装数据

单位：毫米 / 英寸

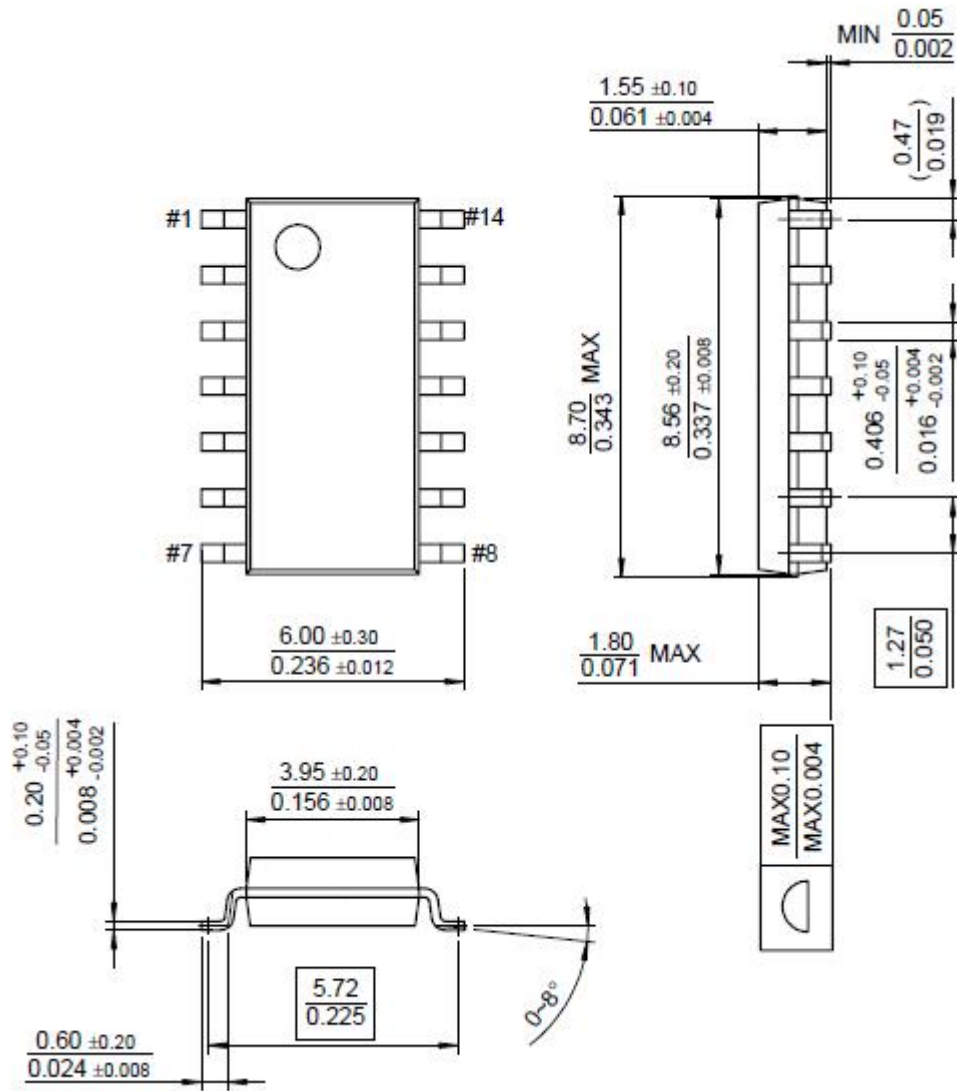


卷轴规格

P/N	PKG	QTY
CD4069UBE-MS	DIP-14	1000

SOP-14 包装数据

单位：毫米 / 英寸



卷轴规格

P/N	PKG	QTY
CD4069UBM-M	SOP-14	2500

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