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SEMICONDUCTOR



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## L293D-L293DD(MS)

Product specification

## DESCRIPTION

The Device is a monolithic integrated high volt-age, high current four channel driver designed to accept standard DTL or TTL logic levels and drive inductive loads (such as relays solenoides, DC and stepping motors) and switching power tran- sistors. To simplify use as two bridges each pair of chan-nels is equipped with an enable input. A separate supply input is provided for the logic, allowing op-eration at a lower voltage and internal clamp di-odes are included.


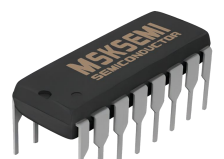


This device is suitable for use in switching appli-cations at frequencies up to 5 kHz.

The L293D is assembled in a 16 lead plastic package which has 4 center pins connected to- gether and used for heatsinking

The L293DD is assembled in a 20 lead surface mount which has 8 center pins connected to- gether and used for heatsinking.

- 600mA OUTPUT CURRENT CAPABILITY PER CHANNEL
- 1.2A PEAK OUTPUT CURRENT (non repeti- tive) PER CHANNEL
- ENABLE FACILITY
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)
- INTERNAL CLAMP DIODES

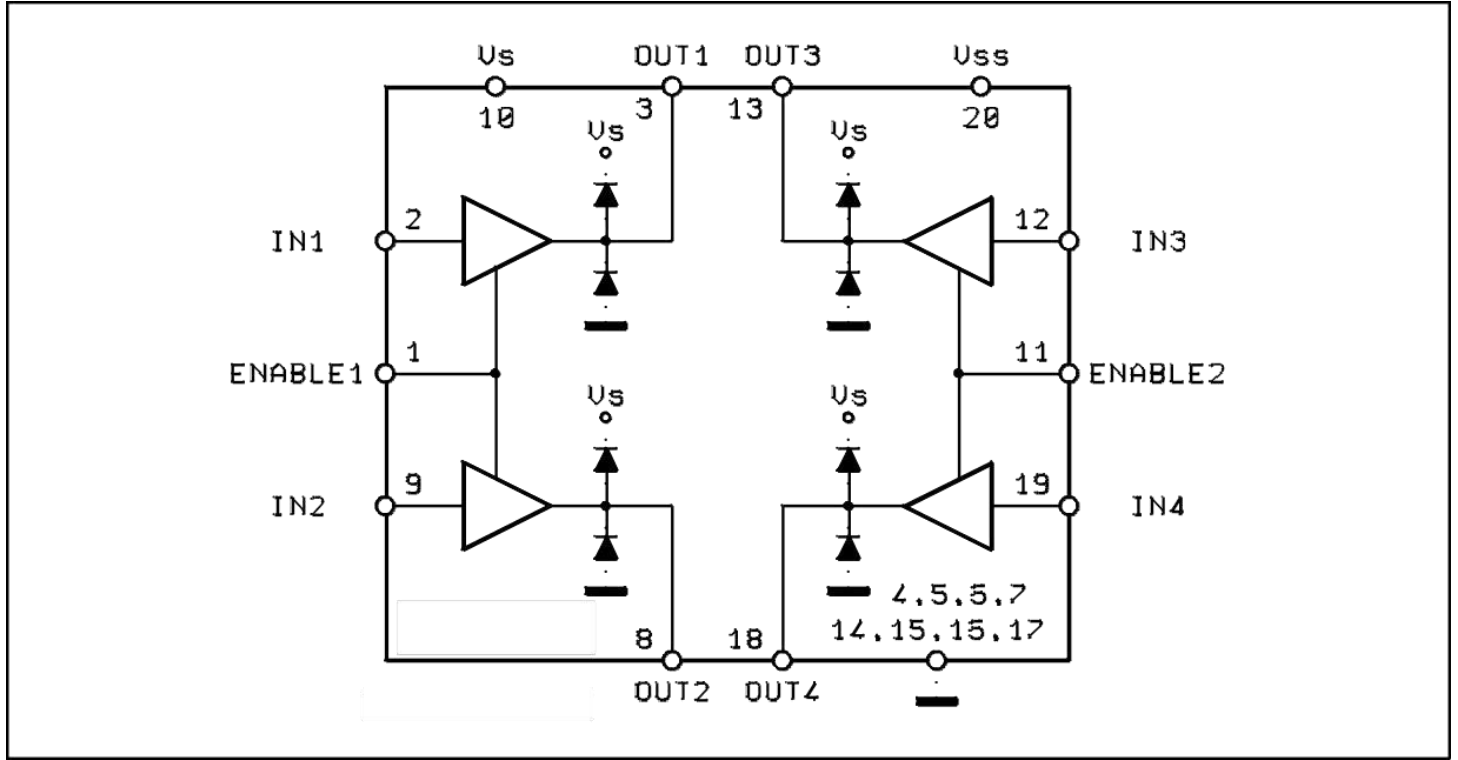
## Reference News

PACKAGE OUTLINE		Marking	
			
SOP-20	DIP-16	SOP-20	DIP-16

## ordering information

P/N	PKG	QTY
L293DD(MS)	SOP-20	1000/tray
L293D(MS)	DIP-16	25/One tube 1000/a box of

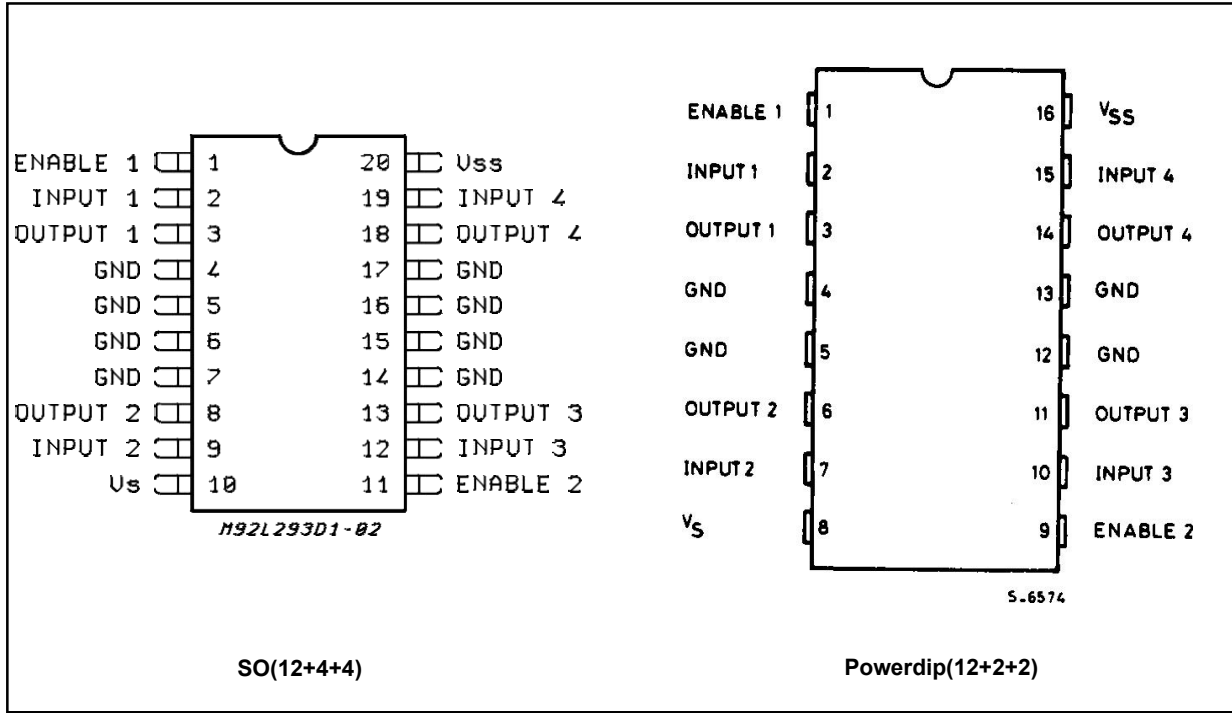
**BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_s$	Supply Voltage	36	V
$V_{SS}$	Logic Supply Voltage	36	V
$V_i$	Input Voltage	7	V
$V_{en}$	Enable Voltage	7	V
$I_o$	Peak Output Current (100 $\mu$ s non repetitive)	1.2	A
$P_{tot}$	Total Power Dissipation at $T_{pins} = 90^\circ\text{C}$	4	W
$T_{stg}, T_j$	Storage and Junction Temperature	- 40 to 150	$^\circ\text{C}$

**PIN CONNECTIONS (Top view)**



**THERMAL DATA**

Symbol	Description	DIP	SO	Unit
R <sub>th j-pins</sub>	Thermal Resistance Junction-pins max.	-	14	°C/W
R <sub>th j-amb</sub>	Thermal Resistance junction-ambient max.	80	50 (*)	°C/W
R <sub>th j-case</sub>	Thermal Resistance Junction-case max.	14	-	

(\*) With 6sq. cm on board heatsink.

**ELECTRICAL CHARACTERISTICS** (for each channel,  $V_S = 24V$ ,  $V_{SS} = 5V$ ,  $T_{amb} = 25^\circ C$ , unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_S$	Supply Voltage (pin 10)		$V_{SS}$		36	V
$V_{SS}$	Logic Supply Voltage (pin 20)		4.5		36	V
$I_S$	Total Quiescent Supply Current (pin 10)	$V_i = L ; I_o = 0 ; V_{en} = H$		2	6	mA
		$V_i = H ; I_o = 0 ; V_{en} = H$		16	24	mA
		$V_{en} = L$			4	mA
$I_{SS}$	Total Quiescent Logic Supply Current (pin 20)	$V_i = L ; I_o = 0 ; V_{en} = H$		44	60	mA
		$V_i = H ; I_o = 0 ; V_{en} = H$		16	22	mA
		$V_{en} = L$		16	24	mA
$V_{IL}$	Input Low Voltage (pin 2, 9, 12, 19)		- 0.3		1.5	V
$V_{IH}$	Input High Voltage (pin 2, 9, 12, 19)	$V_{SS} < 7V$	2.3		$V_{SS}$	V
		$V_{SS} > 7V$	2.3		7	V
$I_{IL}$	Low Voltage Input Current (pin 2, 9, 12, 19)	$V_{IL} = 1.5V$			- 10	$\mu A$
$I_{IH}$	High Voltage Input Current (pin 2, 9, 12, 19)	$2.3V < V_{IH} < V_{SS} - 0.6V$		30	100	$\mu A$
$V_{enL}$	Enable Low Voltage (pin 1, 11)		- 0.3		1.5	V
$V_{enH}$	Enable High Voltage (pin 1, 11)	$V_{SS} < 7V$	2.3		$V_{SS}$	V
		$V_{SS} > 7V$	2.3		7	V
$I_{enL}$	Low Voltage Enable Current (pin 1, 11)	$V_{enL} = 1.5V$		- 30	- 100	$\mu A$
$I_{enH}$	High Voltage Enable Current (pin 1, 11)	$2.3V < V_{enH} < V_{SS} - 0.6V$			$\pm 10$	$\mu A$
$V_{CE(sat)H}$	Source Output Saturation Voltage (pins 3, 8, 13, 18)	$I_o = - 0.6A$		1.4	1.8	V
$V_{CE(sat)L}$	Sink Output Saturation Voltage (pins 3, 8, 13, 18)	$I_o = + 0.6A$		1.2	1.8	V
$V_F$	Clamp Diode Forward Voltage	$I_o = 600nA$		1.3		V
$t_r$	Rise Time (*)	0.1 to 0.9 $V_o$		250		ns
$t_f$	Fall Time (*)	0.9 to 0.1 $V_o$		250		ns
$t_{on}$	Turn-on Delay (*)	0.5 $V_i$ to 0.5 $V_o$		750		ns
$t_{off}$	Turn-off Delay (*)	0.5 $V_i$ to 0.5 $V_o$		200		ns

(\*) See fig. 1.

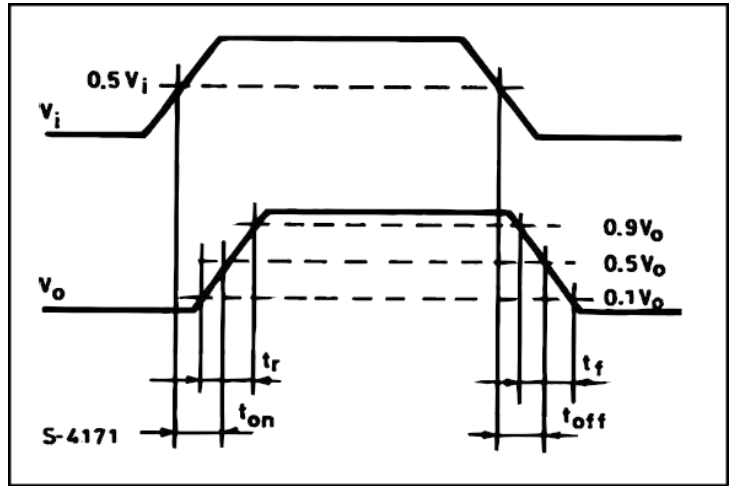
**TRUTH TABLE (one channel)**

Input	Enable (*)	Output
H	H	H
L	H	L
H	L	Z
L	L	Z

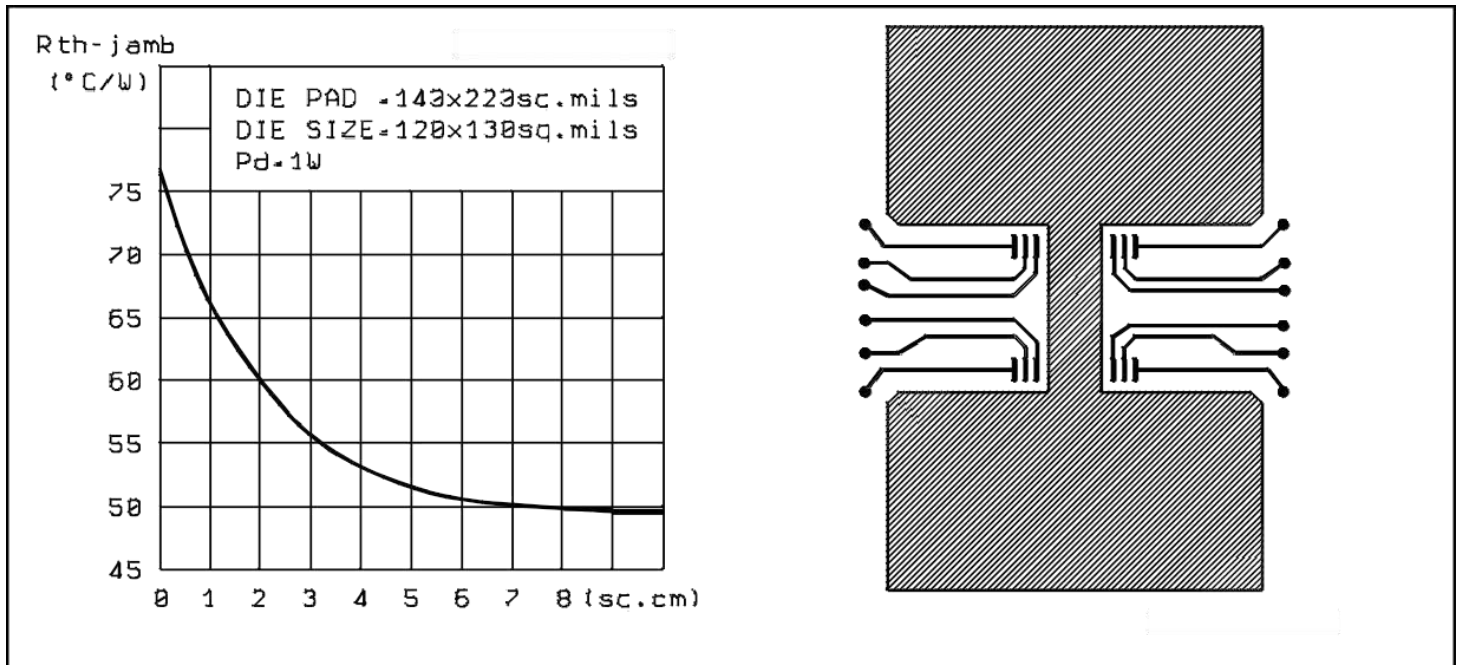
Z = High output impedance

(\*) Relative to the considered channel

**Figure 1: Switching Times**

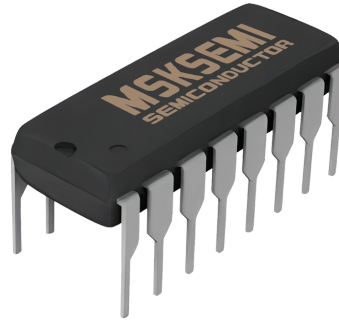


**Figure 2: Junction to ambient thermal resistance vs. area on board heatsink (SO12+4+4 package)**

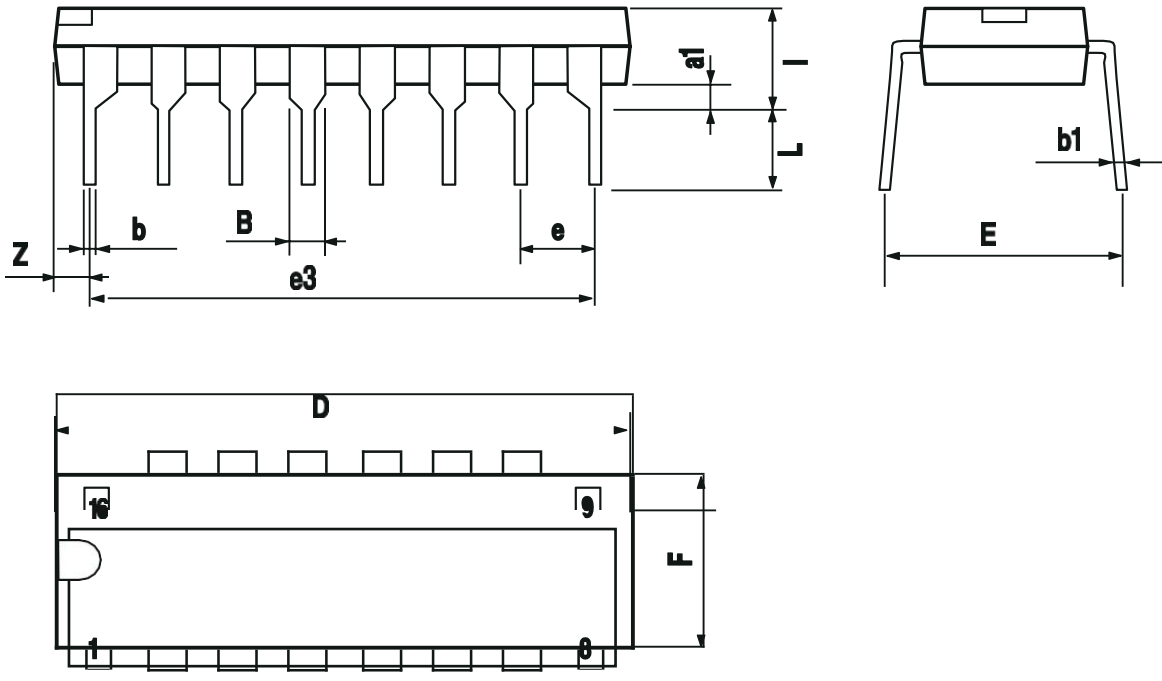


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			20.0			0.787
E		8.80			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050

**OUTLINE AND MECHANICAL DATA**

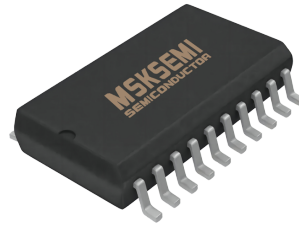


**DIP-16**

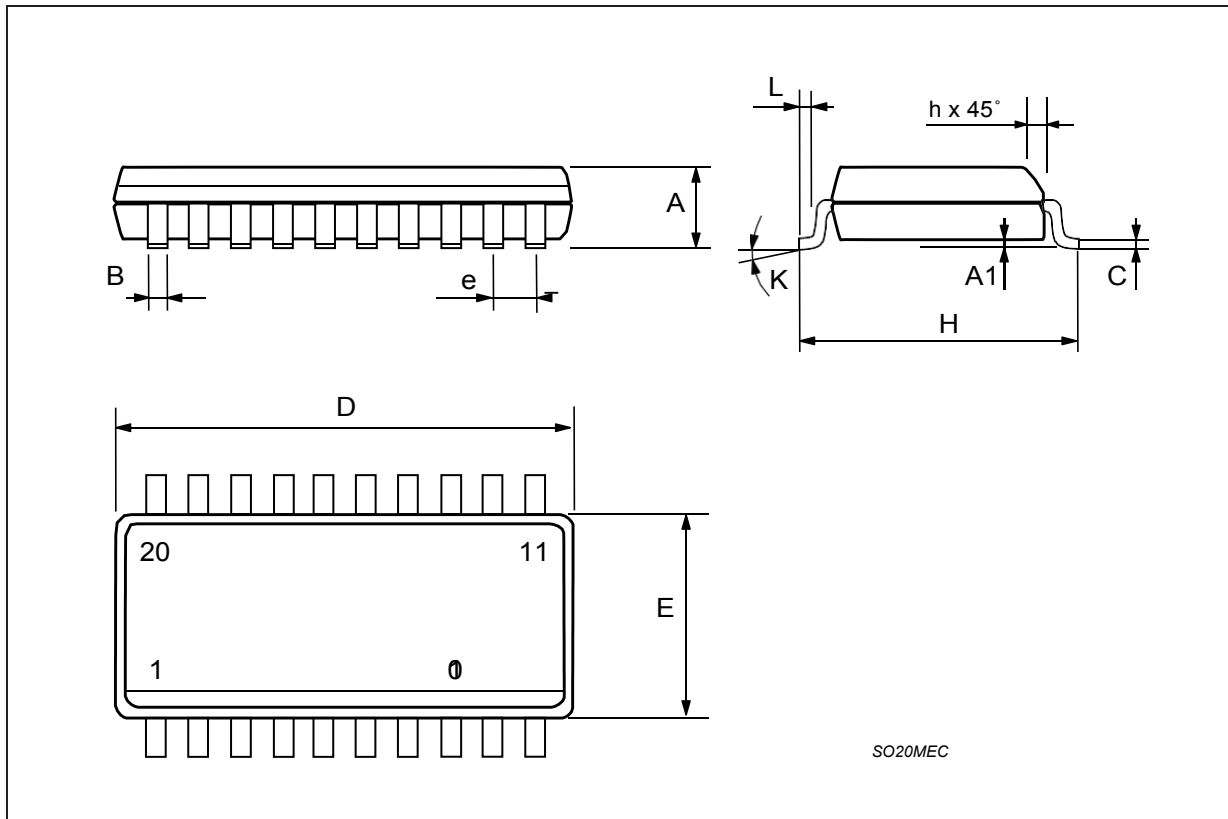


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.3	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.6		13	0.496		0.512
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
K	0° (min.)8° (max.)					

**OUTLINE AND MECHANICAL DATA**



**SOP-20**





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