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PLED

LMV324(MS)

Product specification

GENERAL DESCRIPTION

The LMV324(MS) (quad) are general purpose, low offset, high frequency response and low power operational amplifiers. With an excellent bandwidth of 1MHz, a slew rate of 1V/μs, and a quiescent current of 28μA per amplifier at 5V, the LMV324(MS) family can be designed into a wide range of applications.

The LMV324(MS) op-amps are designed to provide optimal performance in low voltage and low power systems. The input common-mode voltage range includes ground, and the maximum input offset voltage is 3mV. These parts provide rail-to-rail output swing into heavy loads.

The LMV324(MS) families of operational amplifiers are specified at the full temperature range of -40°C to +125°C under single or dual power supplies of 1.5V to 5.5V.

FEATURES

- Input Offset Voltage: 1mV (Typical)
- Low Supply Current: 28μA (Vs=5V)
- Supply Range: 1.8V to 5.5V
- Gain Bandwidth: 1MHz (Vs=5V)
- Slew rate: 1V/μs (Vs=5V)
- Rail-to-Rail Input and Output
- Low Cost
- Micro size Packages:
- LMV324(MS) : SOP-14

APPLICATIONS

- Battery and Power Supply Control
- Audio Outputs
- Smoke/Gas/Environment Sensors
- Portable Equipment and Mobile Devices
- Sensor Interfaces
- Active Filters
- Medical Equipment

Pin Configuration and Functions

PACKAGE OUTLINE	Pin Assignments	Marking
<p>SOP-14</p>	<p>Pin Assignments:</p> <ul style="list-style-type: none"> Pin 1: OUTA Pin 2: -INA Pin 3: +INA Pin 4: V+ Pin 5: +INB Pin 6: -INB Pin 7: OUTB Pin 8: OUTC Pin 9: -INC Pin 10: +INC Pin 11: V- Pin 12: +IND Pin 13: -IND Pin 14: OUTD 	<p>Note: ***=batch</p>

Pin Description

PIN		I/O	DESCRIPTION
NAME	Number		
+INA	3		Noninverting input, channel A
+INB	5		Noninverting input, channel B
+INC	10		Noninverting input, channel C
+IND	12		Noninverting input, channel D
-INA	2		Inverting input, channel A
-INB	6		Inverting input, channel B
-INC	9		Inverting input, channel C
-IND	13		Inverting input, channel D
OUTA	1	0	Output, channel A
OUTB	7	0	Output, channel B
OUTC	8		Output, channel C
OUTD	14	0	Output, channel D
V-	4	—	Negative (lowest) power supply
V+	11	—	Positive (highest) power supply

TYPICAL APPLICATION

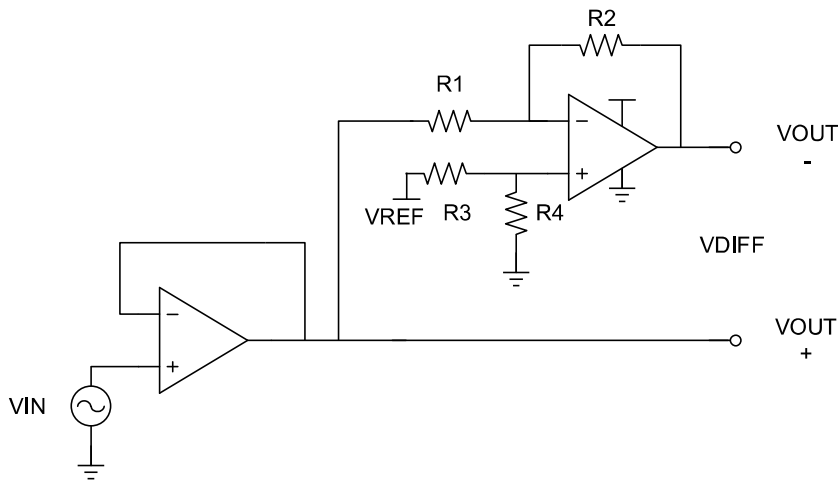


Figure 1. Typical Application

SPECIFICATIONS

Absolute Maximum Ratings⁽¹⁾

		MIN	MAX	UNIT
Voltage	Supply Voltage		6	V
	Signal Input Terminals Voltage ⁽²⁾	(V-) - 0.5	(V+) + 0.5	V
	Signal Input Terminals Voltage ⁽³⁾	(V-) - 0.5	(V+) + 0.5	V
Current	Signal Input Terminals Current ⁽²⁾	-10	10	mA
	Signal output Terminals Current ⁽³⁾	-200	200	mA
	Output Short-Circuit ⁽⁴⁾	Continuous		
θ_{JA}	Operating Temperature Range	-55	125	°C
	Storage Temperature Range	-65	150	°C
	Junction Temperature	-40	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.

(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.5V beyond the supply rails should be current-limited to ± 200 mA or less.

(4) Short-circuit to ground, one amplifier per package.

ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM)	± 2000
		Charged-Device Model (CDM)	± 500
		Machine Model	100

Recommended Operating Conditions

		MIN	MAX	UNIT
Supply voltage, $V_s = (V+) - (V-)$	Single-supply	1.5	5.5	V
	Dual-supply	± 0.75	± 2.75	V

ELECTRICAL CHARACTERISTICS (V_S = +5V)

 At T_A = 25°C, V_{CM}=V_{OUT}= V_S /2, unless otherwise noted.

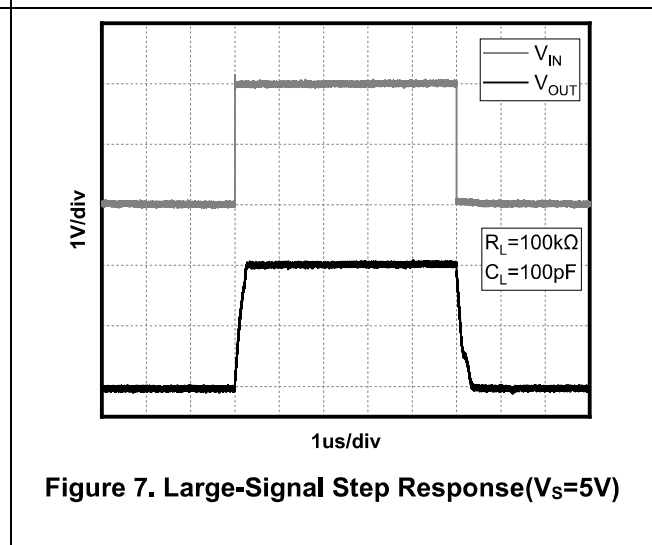
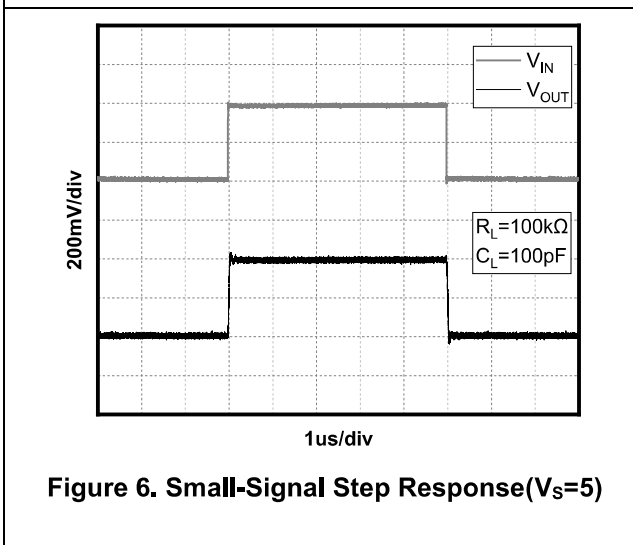
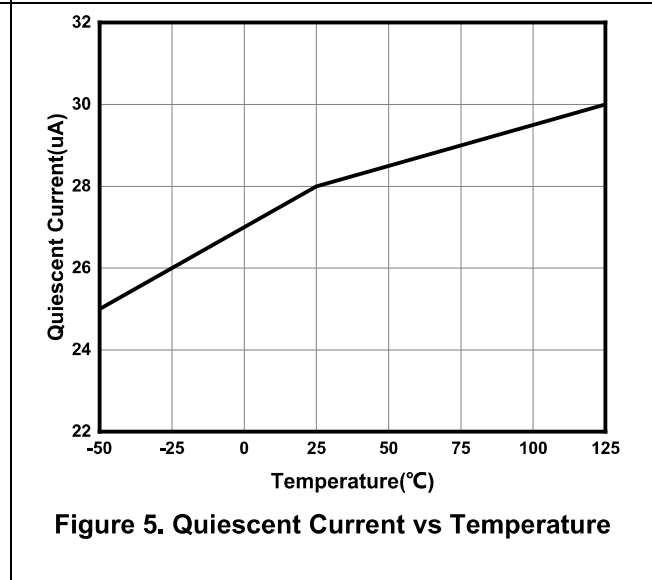
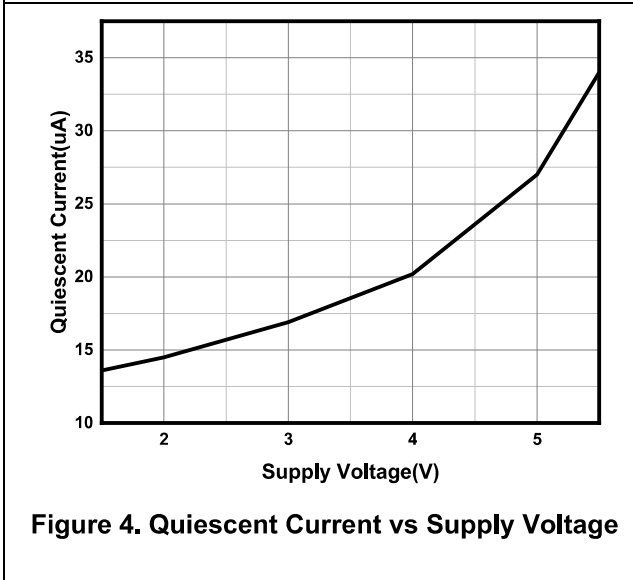
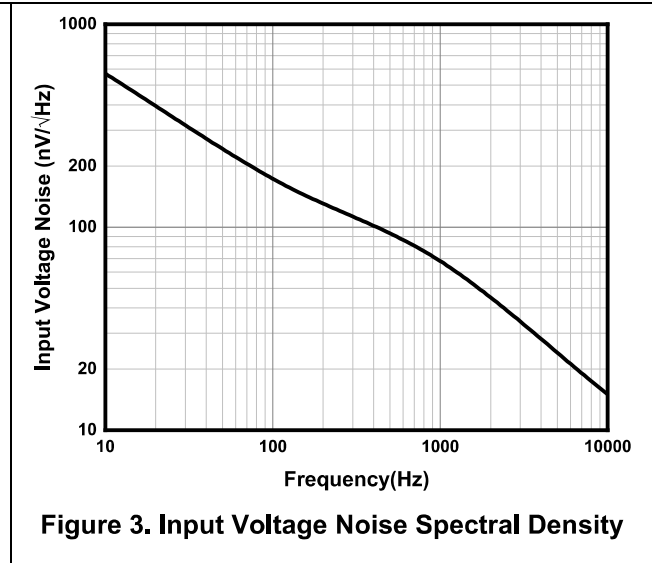
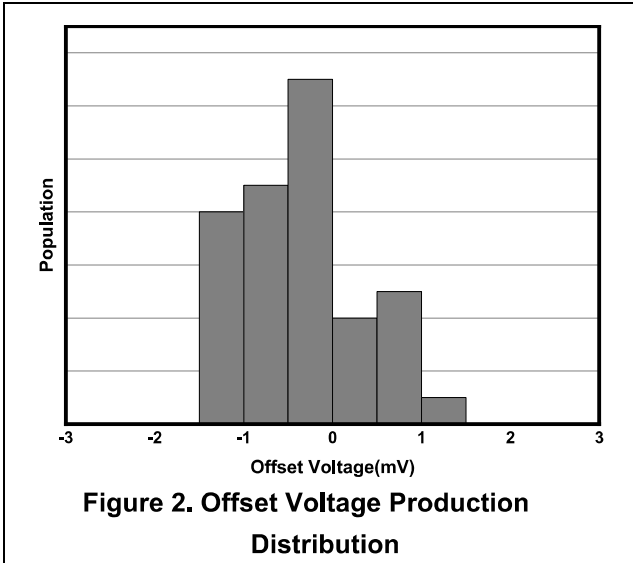
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE					
V _{OS}	Input Offset Voltage	-3	±1	3	mV
dV _{OS} /dT	Input Offset Voltage Average Drift	T _A = -55°C to 125°C		1.8	µV/°C
INPUT CURRENT					
I _B	Input Bias Current		5		pA
I _{OS}	Input Offset Current		1		pA
NOISE					
V _N	Input Voltage Noise	f=0.1Hz to 10Hz	20		µV _{PP}
e _n	Input Voltage Noise Density	f=1kHz	65		nV/√Hz
INPUT VOLTAGE					
V _{CM}	Common-Mode Voltage Range		V _S -0.1	V _S +0.1	V
CMRR	Common-Mode Rejection Ratio	V _{CM} =0.1V to 4V	70	80	dB
FREQUENCY RESPONSE					
GBW	Gain-Bandwidth Product		1		MHz
SR	Slew Rate	G = +1, V _{IN} =2V Step	1		V/µs
t _s	Settling Time to 0.1%	G = +1, V _{IN} =2V Step	2.5		µs
OUTPUT					
A _v	Open-Loop Voltage Gain	V _{OUT} =0.1V to 4.9V R _L =100kΩ	80	100	dB
V _{OUT-SWING}	Output Swing from Rail	R _L =100kΩ		5	mV
I _{SC}	Output Short-Circuit Current	Source current		45	mA
		Sink current		70	mA
C _L ⁽¹⁾	Capacitive Load Drive	G = +1, V _{IN} =0.2V Step		1000	pF

POWER SUPPLY						
PSRR	Power-Supply Rejection Ratio	$V_S=1.5V$ to $5.5V$	80	90		dB
V_S	Operating Voltage Range		1.5		5.5	V
I_Q	Quiescent Current/Amplifier	$I_O=0A$		28	40	μA

(1) Capacitive load drive means that above a given maximum value, the output waveform will oscillate under the step response.

TYPICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$, $V_S = +5\text{V}$, $G=+1$, $V_{IN}=V_{OUT}= V_S / 2$, unless otherwise noted.



TYPICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$, $V_S = +5\text{V}$, $G=+1$, $V_{IN}=V_{OUT}= V_S /2$, unless otherwise noted.

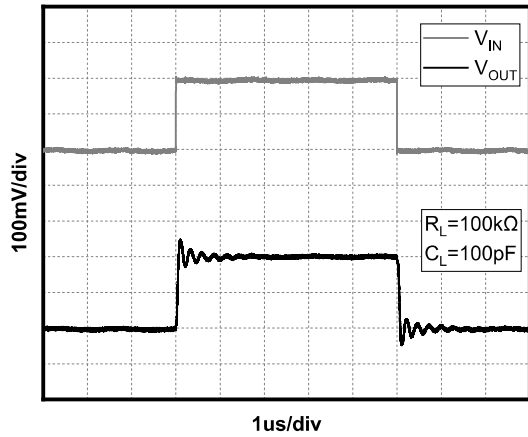


Figure 8. Small-Signal Step Response($V_S=1.5\text{V}$)

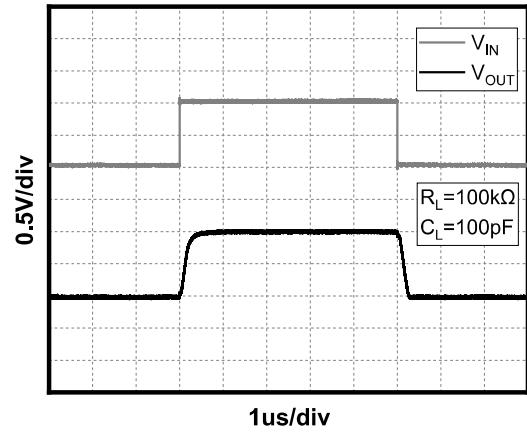


Figure 9. Large-Signal Step Response($V_S=1.5\text{V}$)

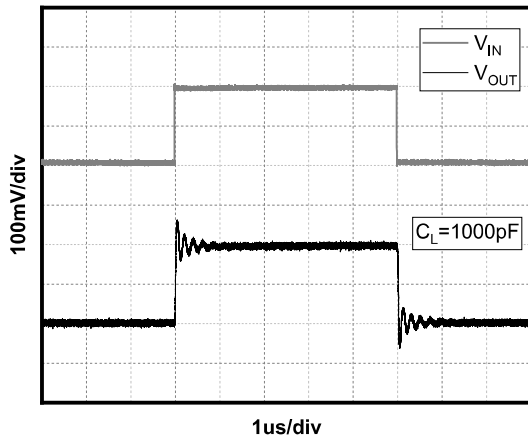


Figure 10. Capacitive Load Drive($C_L=1000\text{pF}$)

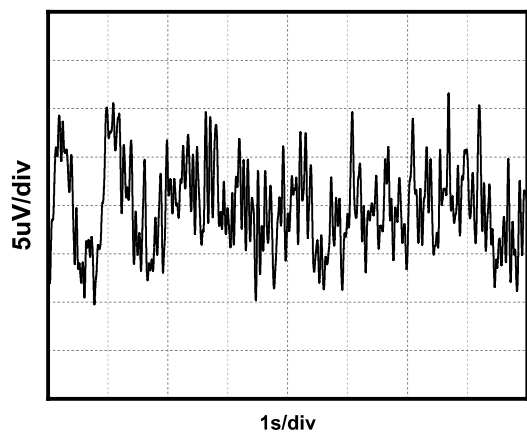


Figure 11. 0.1Hz to 10Hz Noise

Detailed Description

Overview

The LMV324(MS) devices are a low power, unity-gain stable, rail-to-rail operational amplifier that operate in a single-supply voltage range of 1.8V to 5.5V ($\pm 0.9V$ to $\pm 2.75V$). A high supply voltage of 6V (absolute maximum) can permanently damage the amplifier. Rail-to-rail input and output wobbles significantly increase the dynamic range, especially in low-supply applications. Good layout practices require that a 0.1uF capacitor be used where it is tightly threaded through the power supply pin.

Phase Reversal Protection

The LMV324(MS) devices have internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the LMV324(MS) prevents phase reversal with excessive commonmode voltage. Instead, the appropriate rail limits the output voltage

Typical Applications

1 Voltage Follower

As shown in Figure 12, the voltage gain is 1. With this circuit, the output voltage V_{OUT} is configured to be equal to the input voltage V_{IN} . Due to the high input impedance and low output impedance, the circuit can also stabilize the output voltage, the output voltage expression is Detailed Descriptio

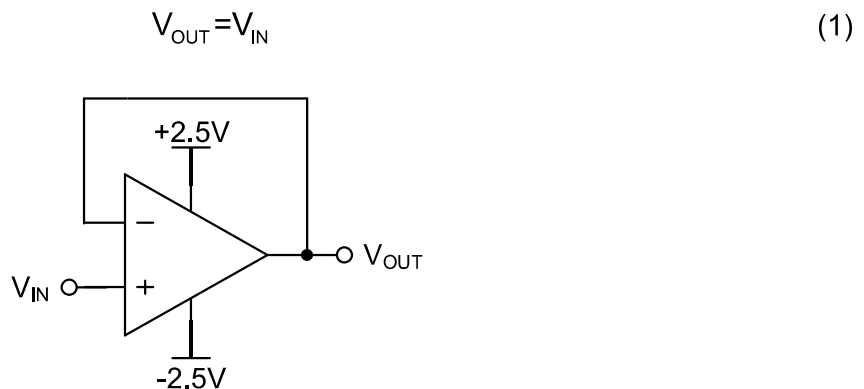


Figure 12. Voltage Follower

2 Inverting Proportional Amplifier

As shown in Figure 13, for a reverse-phase proportional amplifier, the input voltage V_{IN} is amplified by a voltage gain that depends on the ratio of R_1 to R_2 . The output voltage V_{OUT} is inversely with the input voltage V_{IN} . The input impedance of the circuit is equal to R_1 , and the output voltage expression is

$$V_{OUT} = -\frac{R_2}{R_1} V_{IN} \quad (2)$$

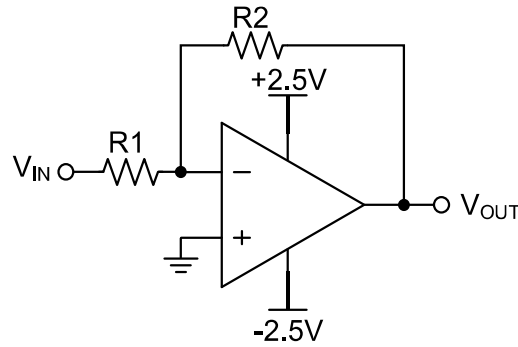


Figure 13. Inverting Proportional Amplifier

3 Noninverting Proportional Amplifier

As shown in Figure 14, for a noninverting amplifier, the input voltage V_{IN} is amplified by a voltage gain that depends on the ratio of $R1$ to $R2$. The output voltage V_{OUT} is in phase with the input voltage V_{IN} . In fact, this circuit has a high input impedance because its input side is the same as the input side of the operational amplifier. The output voltage expression is

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) V_{IN} \quad (3)$$

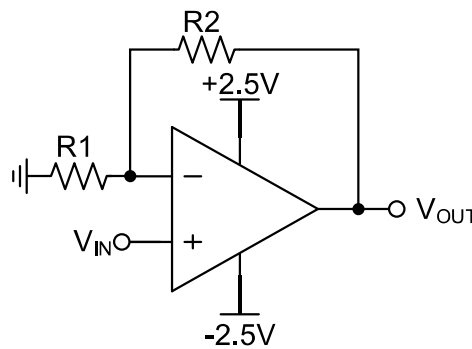


Figure 14. Noninverting Proportional Amplifier

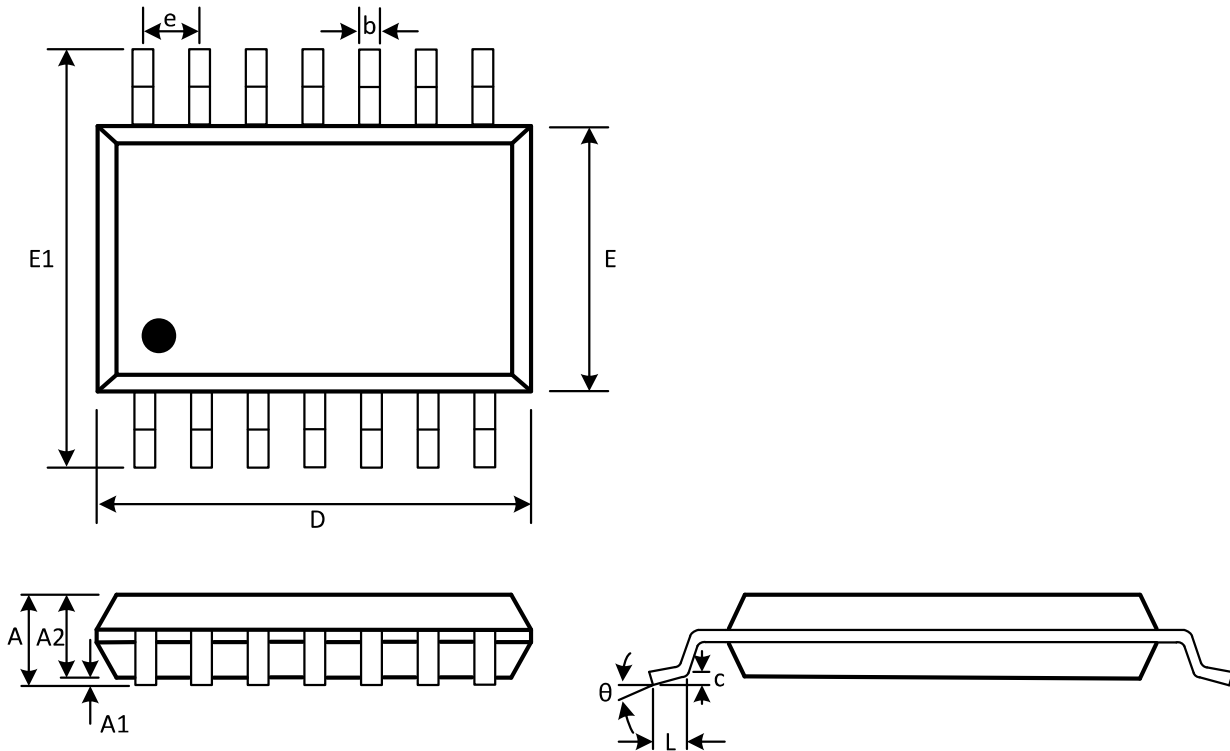
Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1uF capacitor closely across the supply pins.

These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI susceptibility.

PACKAGE DESCRIPTION

SOP-14



(Unit: mm)

Symbol	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.310	0.510
c	0.100	0.250
D	8.450	8.850
e	1.270(BSC)	
E	5.800	6.200
E1	3.800	4.000
L	0.400	1.270
θ	0°	8°

REEL SPECIFICATION

P/N	PKG	QTY
LMV324(MS)	SOP-14	2500

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