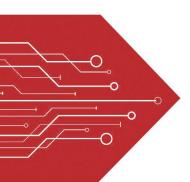
## MSKSEMI















**ESD** 

TVS

TSS

MOV

GDT

**PLED** 

# Broduct data sheet





**SOT-89** 

Daalyaga	Pin	assignn	signment		
Package	1	2	3		
SOT-89	T1	Т2	G		

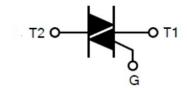
#### **FEATURES**

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drivers and microcontrollers
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate

#### **APPLICATIONS**

- General purpose bidirectional switching
- General purpose low power phase control
- General purpose low power switching
- Solid-state relay

#### SYMBOL:



#### **ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	VALUE		UNIT		
Panatitiva Paak Off State Voltages	V <sub>DRM,</sub> V <sub>RRM</sub>	MAC97A6 400		V		
Repetitive Peak Off-State Voltages		MAC9	MAC97A8 600		] <b>V</b>	
RMS on-State Current	I <sub>T(RMS)</sub>		8.0		Α	
Non-Repetitive Peak On-State Current	I <sub>TSM</sub>		8		Α	
I <sup>2</sup> t for fusing	l²t		0.32		A <sup>2</sup> s	
	JIT/-14	I		50		
Repetitive rate of rise of on-state current after triggering		II		50	A /C	
	dIT/dt	III		50	A/uS	
		IV		10		
Peak gate current	I <sub>GM</sub>		1		Α	
Peak Gate Voltage	$V_{GM}$		5		V	
Peak Gate Power	$P_{GM}$		5		W	
Average Gate Power	$P_{G(AV)}$		0.1		W	
Operating junction temperature	TJ		+125		$^{\circ}$	
Storage Temperature	T <sub>STG</sub>	_	40 ~ +1	150	$^{\circ}$	

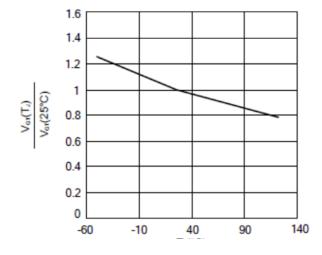


## **ELECTRICAL CHARACTERISTICS** (TJ=25°C)

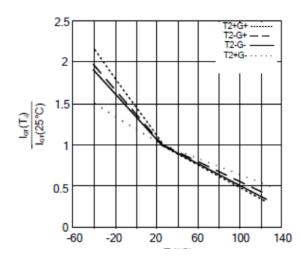
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
Peak Repetitive Forward or Reverse Blocking Current	I <sub>DRM</sub> I <sub>RRM</sub>	$V_{AK}$ = Rated $V_{DRM}$ or $V_{RRM}$ ;			10	uA
			I		5.0	
Gate Trigger Current	I <sub>GT</sub>	$V_D = 12V$ $I_{GT} = 0.1A$	II		5.0	mA
			III		5.0	
			IV		7.0	
Gate Trigger Voltage	$V_{GT}$	$V_D=12V$ , RL= $100\Omega$			2.0	V
Peak Forward On-State Voltage	V <sub>TM</sub>	IT=1.0A,			1.7	V
			I		10	
Holding Current	IL	V <sub>D</sub> =12V	II		20	m ^
		I <sub>G</sub> =0.1A,	III		10	mA
			IV		10	
Latch Current	$I_{H}$	V <sub>D</sub> =12V ,IG=0.1A			10	mA
Critical Rate of Rise of Off-State Voltage	dV/dt	$V_D=67\%V_{DRM}, R_{GK}=1k\Omega,$		10		V/µs

#### **ELECTRICAL CHARACTERISTIC CURVE**

Normalized Gate Trigger Voltage as a of Function Junction Temperature; Typical Values.

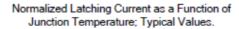


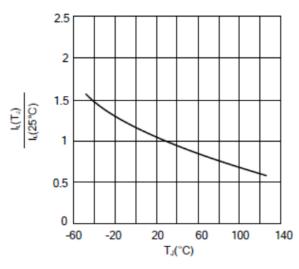
Normalized Gate Trigger Current as a Function of Junction Temperature; Typical Values.



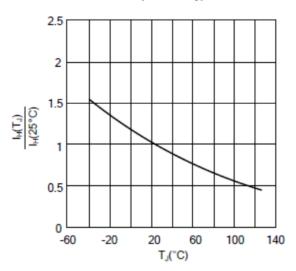




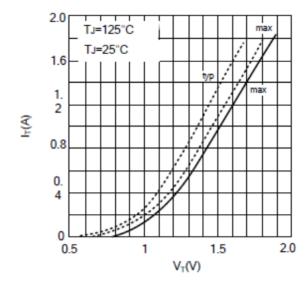




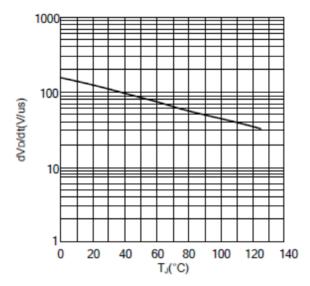
Normalized Holding Current as a Function of Junction Temperature; Typical Values.



On-State Current as a Function of On-State Voltage; Typical and Maximum Values.

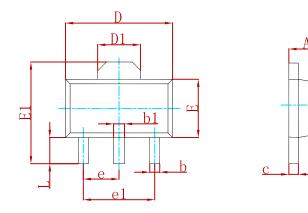


Critical Rate of Rise of Off-State Voltage as a Function of Junction Temperature; Typical Values.



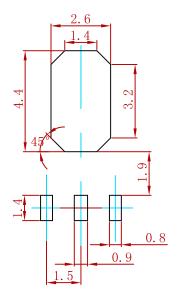


#### **PACKAGE MECHANICAL DATA**



Symbol	Dimensions In Millimeters		Dimension	s In Inches
Symbol	Min	Max	Min	Max
Α	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
С	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF.		0.061 REF.	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
е	1.500 TYP.		0.060 TYP.	
e1	3.000 TYP.		0.118 TYP.	
L	0.900	1.200	0.035	0.047

### **Suggested Pad Layout**



#### Note:

- 1.Controlling dimension:in millimeters.
- 2.General tolerance:±0.05mm.
- 3. The pad layout is for reference purposes only.

#### **REEL SPECIFICATION**

P/N	PKG	QTY
MAC97A6 THRU MAC97A8	SOT-89	1000



Semiconductor Compiance



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