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OPA2348AIDR-MS/OPA2348AIDGKR-MS

Product specification

GENERAL DESCRIPTION

The OPA2348AIDR-MS/OPA2348AIDGKR-MS is dual CMOS operational amplifier that uses the proprietary auto-calibration technique to simultaneously provides very low offset voltage near-zero drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high-impedance inputs that have a common-mode range 200mV beyond the rails, and rail-to-rail output that swings within 50mV of the rails single or dual supplies as low as 2.1V($\pm 1.35V$) and up to 5.5V($\pm 2.75V$) can be used. These devices are optimized for low voltage, single supply operation.

The OPA2348AIDR-MS/OPA2348AIDGKR-MS offers excellent CMRR without the crossover associated with traditional complementary input stages. This design results in superior performance for driving analog-to-digital converters (ADC) without degradation of differential linearity.

The OPA2348AIDR-MS/OPA2348AIDGKR-MS is available in the 8-pin and VSSOP packages.


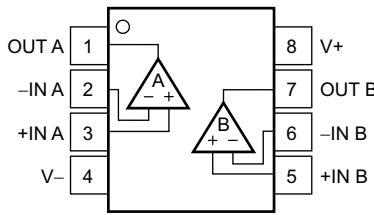



FEATURES

- VDD range: 2.1V to 5.5V
- Low Offset Voltage: 0.5mV (Typical)
- Low Drit: 0.65 $\mu V/^\circ C$ (Typical)
- Low Noise
- Quiescent Current: 50 μA (Total)
- Rail to Rail Input/Output
- MicroSize Packages: SOP8 and VSSOP8

APPLICATIONS

- Transducers
- Temperature Measurement
- Electronic Scales
- Medical instrumentation
- Handheld Test Equipment

Pin Description and Marking

| | | | |
|----------------|---|---|---|
| SOP-8 |  |  |  |
| VSSOP-8 |  | |  |

| NAME | PIN | | I/O | DESCRIPTION |
|-------|-------|---------|-----|---------------------------------|
| | SOP-8 | VSSOP-8 | | |
| -IN A | 2 | 2 | I | Inverting input, channel A |
| -IN B | 6 | 6 | I | Inverting input, channel B |
| +IN A | 3 | 3 | I | Noninverting input, channel A |
| +IN B | 5 | 5 | I | Noninverting input, channel B |
| OUT A | 1 | 1 | O | Output, channel A |
| OUT B | 7 | 7 | O | Output, channel B |
| V- | 4 | 4 | — | Negative (lowest) power supply |
| V+ | 8 | 8 | — | Positive (highest) power supply |

SIMPLIFIED SCHEMATIC

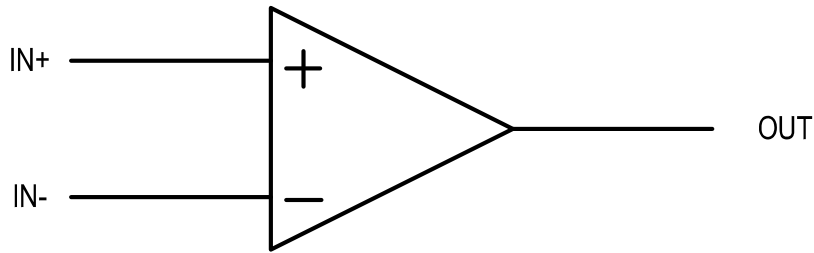


Figure 1. Simplified Schematic

ABSOLUTE MAXIMUM RATINGS

Thermal Resistance θ_{JC} 130°C/W
Supply Voltage.....2.1 to 5.5V
Signal Input Terminals Voltage..... -0.1 to (V+)+0.1V
Operating Junction Temperature..... 150°C
Operating Temperature Range.....-40°C to 125°C
Storage Temperature -65°C to 150°C

ordering information

| P/N | PKG | QTY |
|------------------|---------|------|
| OPA2348AIDR-MS | SOP-8 | 2500 |
| OPA2348AIDGKR-MS | VSSOP-8 | 3000 |

ELECTRICAL CHARACTERISTICS

(At $T_A = 25^\circ\text{C}$, $R_L=10\text{k}$ connected to $V_S/2$, and $V_{OUT}=V_S/2$, unless otherwise noted.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|---|-------------|------|-------------|------------------------------|
| Input Offset Voltage | $V_S=\pm 2.5\text{V}$ | -2 | 0.5 | 2 | mV |
| Input Offset Voltage Drift | $T_A = -55^\circ\text{C}$ to 125°C | | 0.65 | | $\mu\text{V}/^\circ\text{C}$ |
| Power Supply Rejection Ratio | $V_S = 2.1\text{V}$ to 5.5V $T_A = -55^\circ\text{C}$ to 125°C | 80 | 90 | | dB |
| Input Bias Current | $T_A = 25^\circ\text{C}$ | | 2 | | pA |
| Input Offset Current | | | 1 | | pA |
| Common-mode Voltage Range | | $(V_-)-0.1$ | | $(V_+)+0.1$ | V |
| Common-mode Rejection Ratio | $(V_-)-0.1 < V_{CM} < (V_+)+0.1$ $T_A = -55^\circ\text{C}$ to 125°C | 80 | 95 | | dB |
| Open Loop Voltage Gain | $(V_-)+100\text{mV} < V_O < (V_+)-100\text{mV}$, $R_L=10\text{k}$ $T_A = -55^\circ\text{C}$ to 125°C | 80 | 100 | | dB |
| Gain-bandwidth product | $C_L=120\text{pF}$ | | 1.5 | | MHz |
| Slew Rate | $G=+1$ | | 1.2 | | $\text{V}/\mu\text{s}$ |
| Specified Voltage Range | | 2.1 | | 5.5 | V |
| Quiescent Current (Total) | $I_O=0\text{A}$ | | 50 | | μA |
| Operating Temperature Range | | -55 | | 125 | $^\circ\text{C}$ |
| Storage Temperature Range | | -65 | | 150 | $^\circ\text{C}$ |

TYPICAL PERFORMANCE CHARACTERISTICS

(At $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $C_L = 20\text{pF}$, unless otherwise noted.)

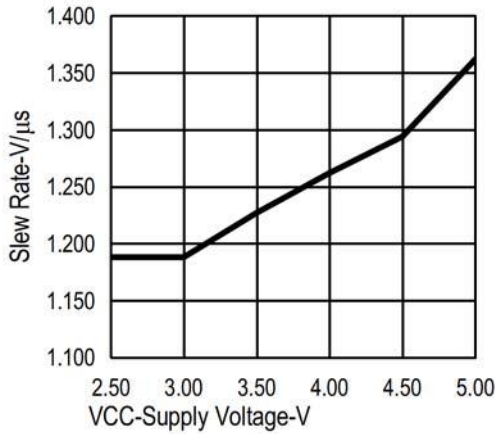


Figure 2. Slew Rate vs Supply Voltage

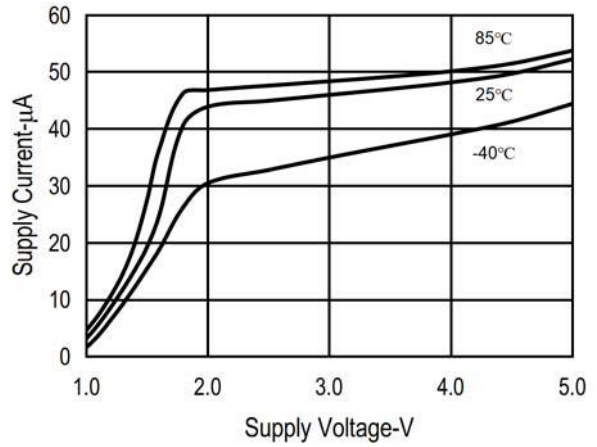


Figure 3. Supply Current vs Supply Voltage

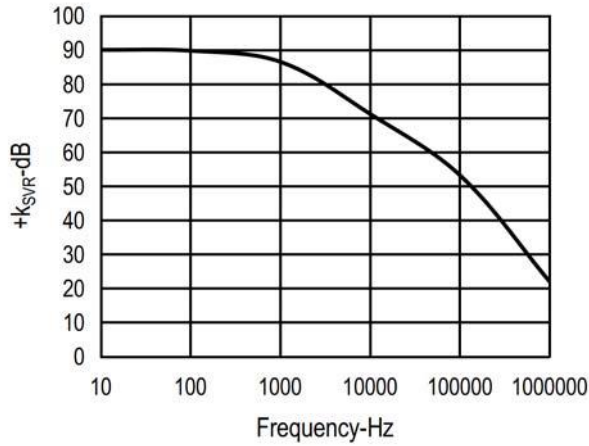


Figure 4. +ksvr vs Frequency

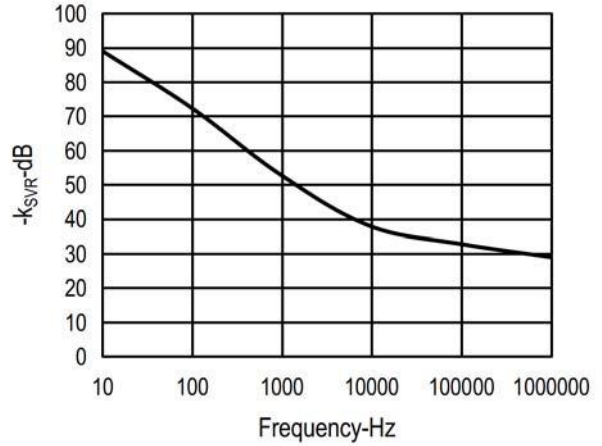


Figure 5. -ksvr vs Frequency

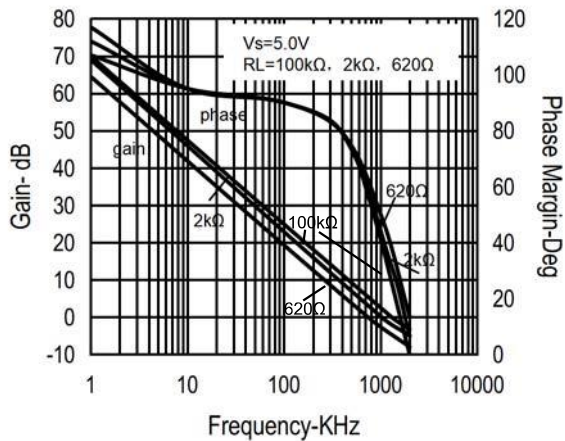


Figure 6. Frequency Response vs Resistive Load

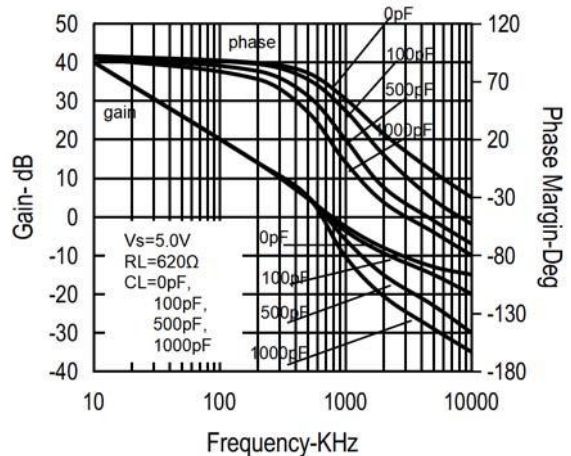


Figure 7. Frequency Response vs Capacitive Load

TYPICAL PERFORMANCE CHARACTERISTICS

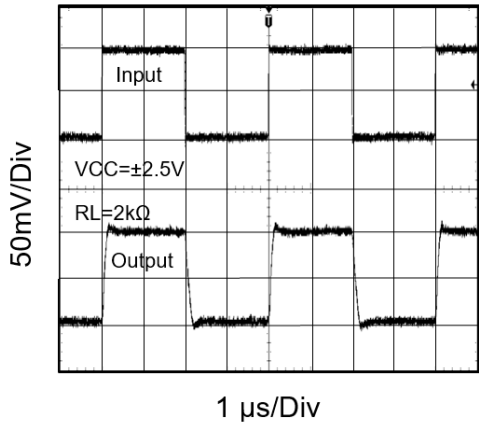


Figure 8. Noninverting Small-Signal Pulse Response

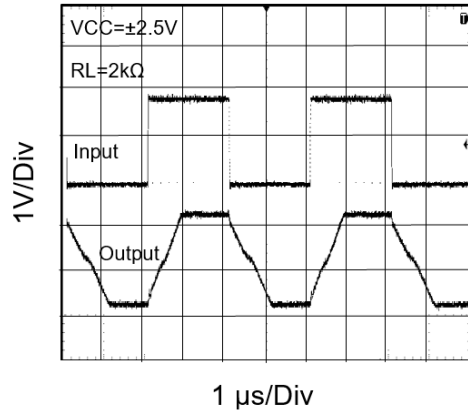


Figure 9. Noninverting Large-Signal Pulse Response

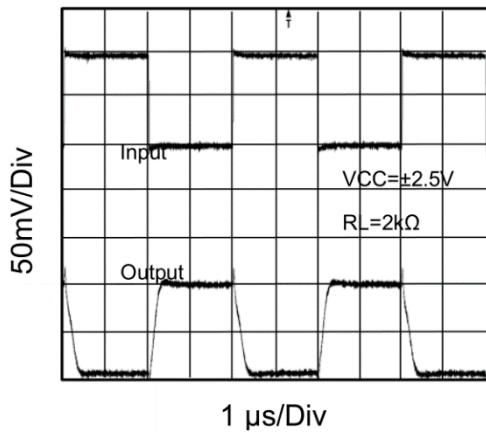


Figure 10. Inverting Small-Signal Pulse Response

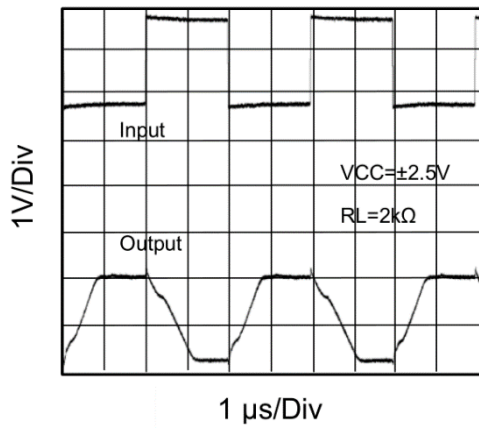


Figure 11. Inverting Large-Signal Pulse Response

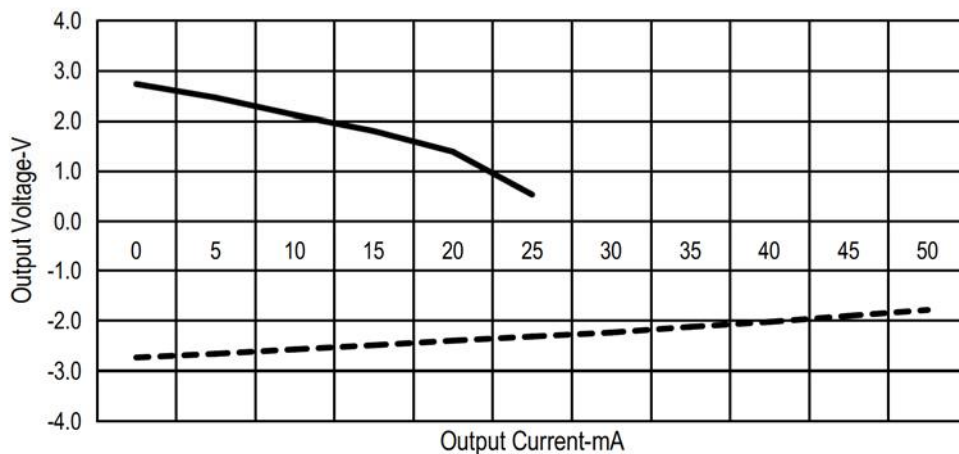


Figure 12. Output Voltage vs Output Current

FUNCTIONAL DESCRIPTION

Operating Voltage

The OPA2348AIDR-MS/OPA2348AIDGKR-MS device is fully specified and ensured for operation from 2.1V to 5.5V. In addition, many specifications apply from -55°C to 125°C. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristics graphs.

Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The OPA2348AIDR-MS/OPA2348AIDGKR-MS device has a 1.5-MHz unity-gain bandwidth.

Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The OPA2348AIDR-MS/OPA2348AIDGKR-MS devices have a 1.2-V/ μ s slew rate. The LMV358-MS is characterized to perform with this technique; the recommended resistor value is approximately 20 k.

Device Functional Modes

The OPA2348AIDR-MS/OPA2348AIDGKR-MS device has a single functional mode. The device is powered on as long as the power supply voltage is between 2.1V(\pm 1.35V) and 5.5V(\pm 2.75V).

APPLICATIONS INFORMATION

The OPA2348AIDR-MS/OPA2348AIDGKR-MS is a unity-gain stable, precision operational amplifier with very low offset voltage drift; these devices are also free from output phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power-supply pins. In most cases, 0.1 μ F capacitors are adequate.

Typical Application

Figure 13 shows a simple circuit to convert a single-ended input into differential output. The OPA2348AIDR-MS/OPA2348AIDGKR-MS could be used to build this circuit. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage, V_{out+} . The second amplifier inverts the input and adds a reference voltage to generate V_{out-} . Both V_{out+} and V_{out-} range from 0.5 to 2V. The difference, V_{DIFF} , is the difference between V_{out+} and V_{out-} .

Detailed Design Procedure

Linearity over the input range is key for good dc accuracy. The common mode input range and the output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design. Because OPA2348AIDR-MS/OPA2348AIDGKR-MS has a bandwidth of 1 MHz, this circuit will only be able to process signals with frequencies of less than 1 MHz.

Because the transfer function of V_{out-} is heavily reliant on resistors (R_1 , R_2 , R_3 , and R_4), use resistors with low tolerances to maximize performance and minimize error. This design used resistors with resistance values of 36 k with tolerances measured to be within 2%. If the noise of the system is a key parameter, the user can select smaller resistance values (6 k or lower) to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

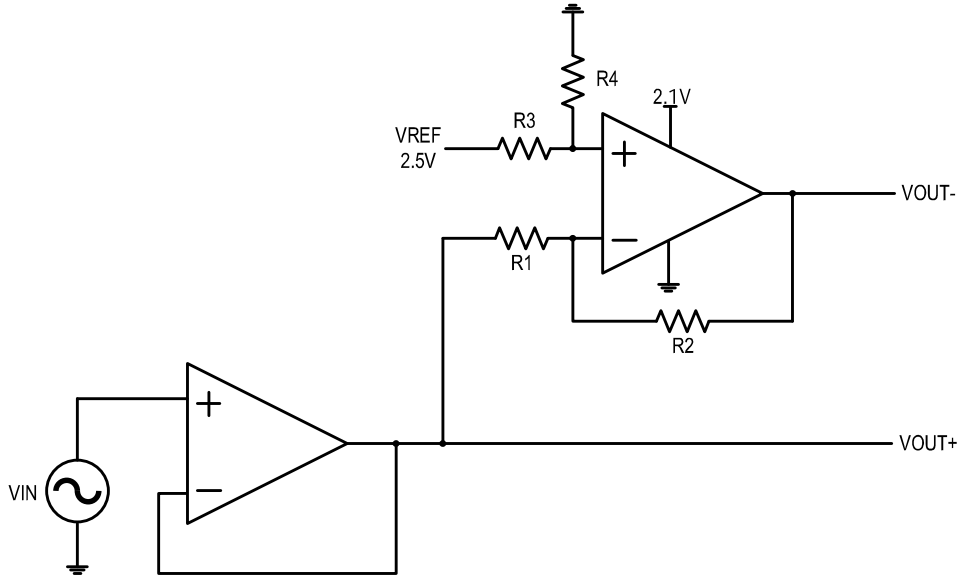
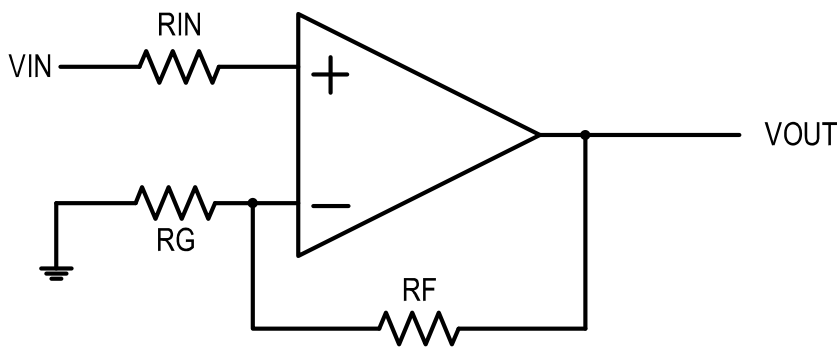


Figure 13. Schematic for Single-Ended Input to Differential Output Conversion

LAYOUT

Use good PCB layout practices for best operational performance of the device, including:

- Keep the length of input traces as short as possible.
- Run the input traces as far away from the supply lines as possible to reduce parasitic coupling.
- Place components close to device and to each other to reduce parasitic capacitance and parasitic errors.
- Use low-ESR, ceramic bypass capacitors to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
- Grounding for analog and digital portions of circuitry separately to suppress the noise.



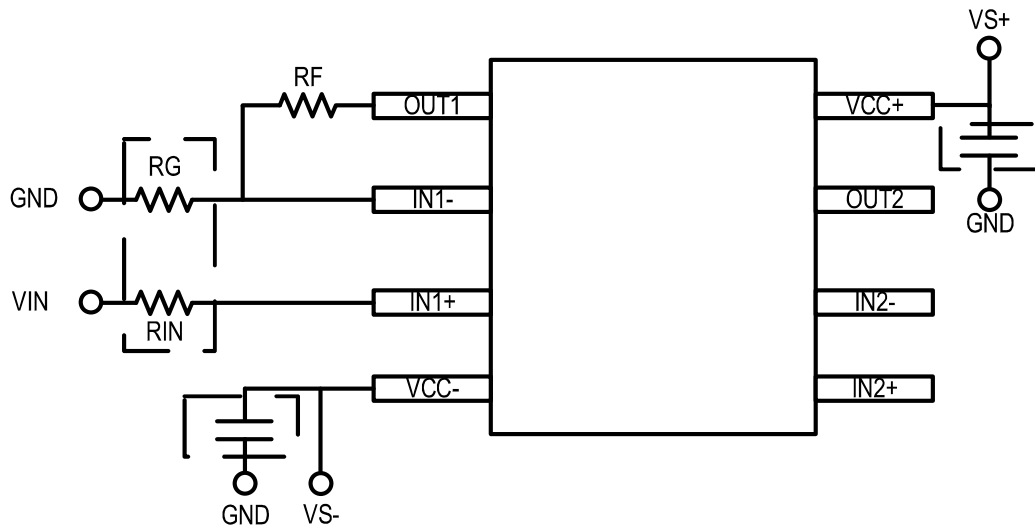
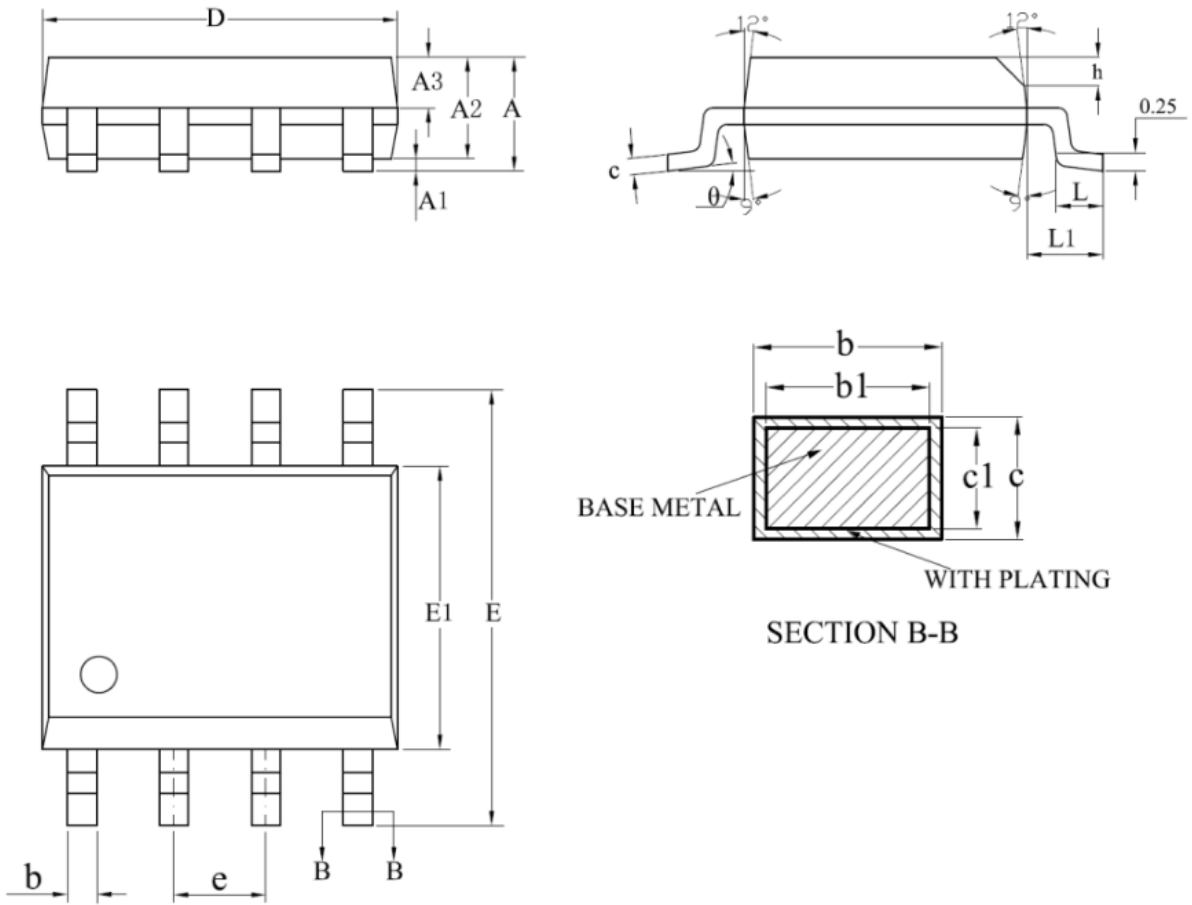


Figure 14. Operational Amplifier Schematic and Board Layout for Noninverting Configuration

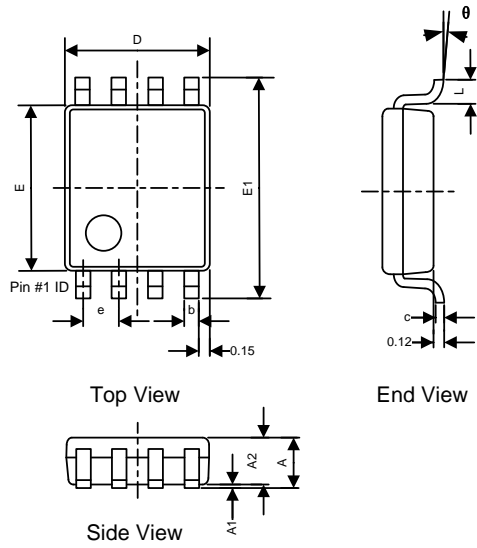
PACKAGE DESCRIPTION

SOP-8



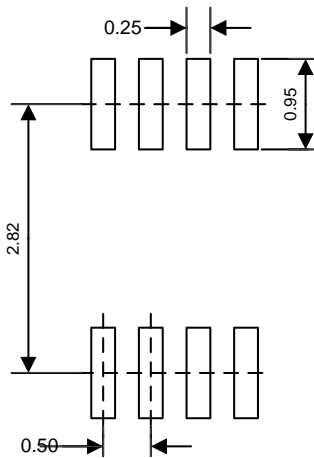
| SYMBOL | millimeter | | |
|----------|------------|------|------|
| | min | nom | max |
| A | - | - | 1.75 |
| A1 | 0.10 | - | 0.23 |
| A2 | 1.30 | 1.40 | 1.50 |
| A3 | 0.60 | 0.65 | 0.70 |
| b | 0.39 | - | 0.47 |
| b1 | 0.38 | 0.41 | 0.44 |
| c | 0.20 | - | 0.24 |
| c1 | 0.19 | 0.20 | 0.21 |
| D | 4.80 | 4.90 | 5.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | 1.27BSC | | |
| h | 0.25 | - | 0.50 |
| L | 0.50 | - | 0.80 |
| L1 | 1.05REF | | |
| θ | 0 | - | 8° |

PACKAGE DESCRIPTION



| DIMENSIONS | | | | | | |
|------------|-------------|------|------|----------|-------|-------|
| Symbol | MILLIMETERS | | | INCHES | | |
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.60 | 0.75 | 0.90 | 0.023 | 0.029 | 0.035 |
| A1 | 0.00 | 0.05 | 0.10 | 0.000 | 0.002 | 0.004 |
| A2 | 0.60 | 0.70 | 0.80 | 0.023 | 0.027 | 0.031 |
| b | 0.17 | - | 0.27 | 0.007 | - | 0.011 |
| c | 0.08 | - | 0.23 | 0.003 | - | 0.009 |
| D | 1.90 | 2.00 | 2.10 | 0.075 | 0.079 | 0.083 |
| E | 2.20 | 2.30 | 2.40 | 0.086 | 0.090 | 0.094 |
| E1 | 3.00 | 3.10 | 3.20 | 0.118 | 0.122 | 0.126 |
| e | 0.50BSC | | | 0.020BSC | | |
| L | 0.20 | 0.28 | 0.35 | 0.008 | 0.011 | 0.014 |
| θ | 0° | 3° | 6° | 0° | 3° | 6° |

Land Pattern



NOTES:

1. Compound dimension: 2.00×2.30;
2. Unit: mm;
3. General tolerance ± 0.05 mm unless otherwise specified;
4. The layout is just for reference.

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