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## Si7850DP-MS

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Product specification

## Description

The Si7850DP-MS uses advanced trench technology to provide excellent RDS(ON) , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

## Features

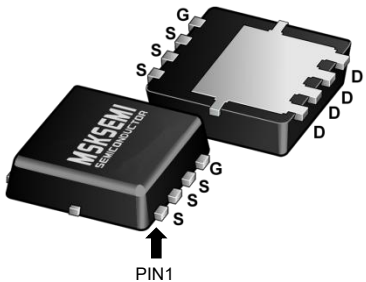
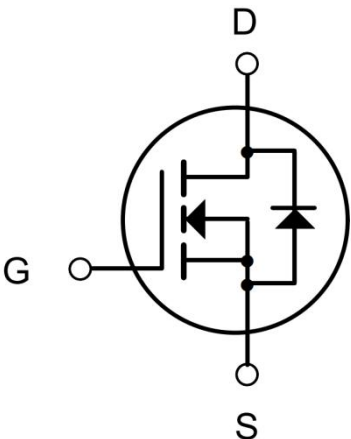

VDS = 60V ID =30 A

RDS(ON) < 25mΩ @ VGS=10V

## Application

- Battery protection
- Load switch
- Uninterruptible power supply

## Reference News

PACKAGE OUTLINE	N-Channel MOSFET	Marking
 <p>DFN5X6-8L</p>		

## Absolute Maximum Ratings (TC=25°C unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	60	V
VGS	Gate-Source Voltage	±20	V
Id@Tc=25°C	Continuous Drain Current, VGS @ 10V <sup>1</sup>	30	A
Id@Tc=100°C	Continuous Drain Current, VGS @ 10V <sup>1</sup>	15	A
IDM	Pulsed Drain Current <sup>2</sup>	46	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	25.5	mJ
IAS	Avalanche Current	22.6	A
Pd@Tc=25°C	Total Power Dissipation <sup>4</sup>	34.7	W
TSTG	Storage Temperature Range	-55 to 150	°C
TJ	Operating Junction Temperature Range	-55 to 150	°C
RθJA	Thermal Resistance Junction-ambient <sup>1</sup>	62	°C/ W
RθJC	Thermal Resistance Junction-Case <sup>1</sup>	3.6	°C/ W

**Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
B <sub>V</sub> DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	60	---	---	V
Δ B <sub>V</sub> DSS/ Δ T <sub>J</sub>	B <sub>V</sub> DSS Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =1mA	---	0.063	---	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =15A	---	20	25	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	---	24	20	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.2	---	2.5	V
Δ V <sub>GS(th)</sub>	V <sub>GS(th)</sub> Temperature Coefficient		---	-5.24	---	MV/°C
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =48V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =48V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V	---	---	±100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =15A	---	17	---	S
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	3.2	---	Ω
Q <sub>g</sub>	Total Gate Charge (4.5V)	V <sub>DS</sub> =48V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =12A	---	12.6	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	3.2	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	6.3	---	
T <sub>d(on)</sub>	Turn-On Delay Time		---	8	---	
T <sub>r</sub>	Rise Time	V <sub>DD</sub> =30V, V <sub>GS</sub> =10V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =10A	---	14.2	---	ns
T <sub>d(off)</sub>	Turn-Off Delay Time		---	24.4	---	
T <sub>f</sub>	Fall Time		---	4.6	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	---	1378	---	pF
C <sub>oss</sub>	Output Capacitance		---	86	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	64	---	

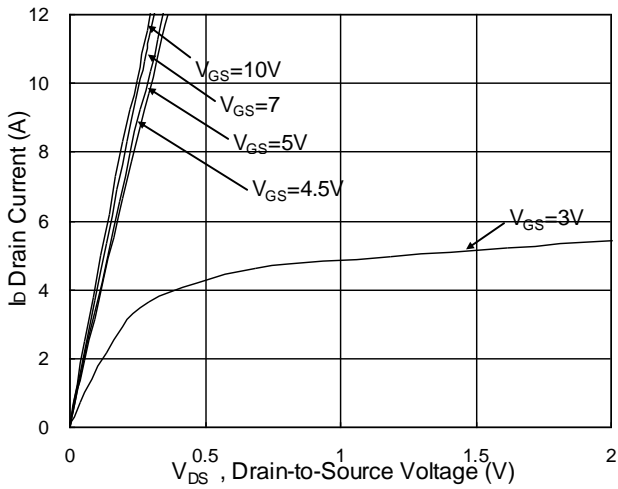
**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I <sub>S</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	30	A
I <sub>SM</sub>	Pulsed Source Current <sup>2,5</sup>		---	---	46	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =1A, T <sub>J</sub> =25°C	---	---	1.2	V

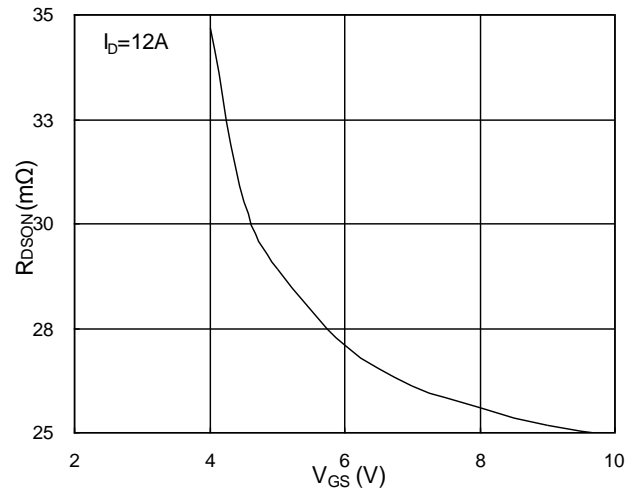
**Note :**

- The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- The EAS data shows Max. rating. The test condition is V<sub>DD</sub>=25V, V<sub>GS</sub>=10V, L=0.1mH, I<sub>AS</sub>=22.6A
- The power dissipation is limited by 150C junction temperature
- The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.

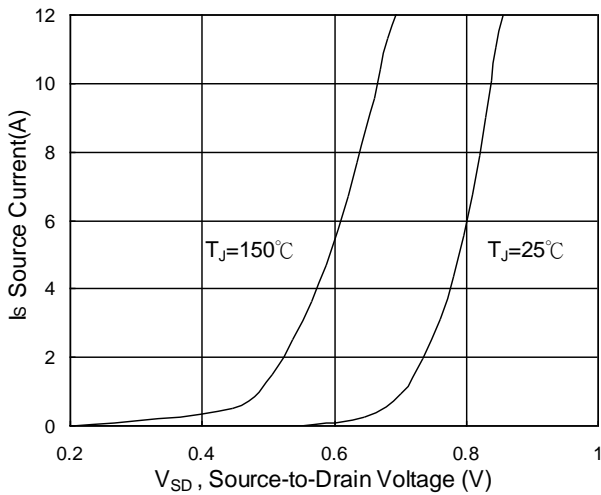
**Typical Characteristics**



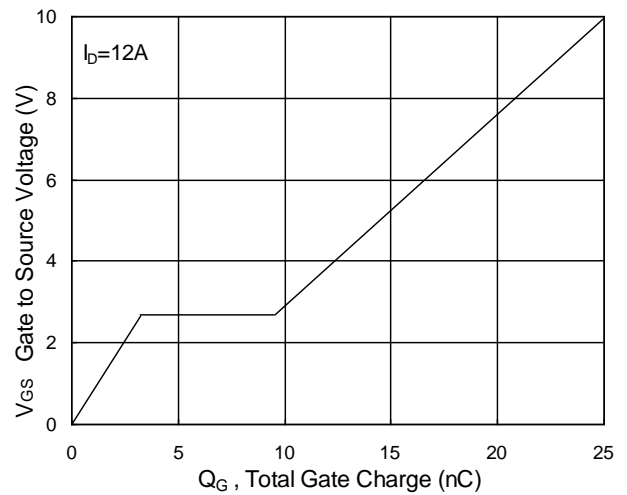
**Fig.1 Typical Output Characteristics**



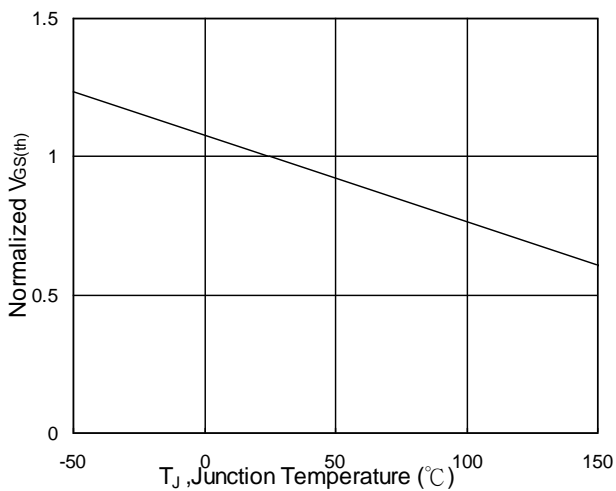
**Fig.2 On-Resistance v.s Gate-Source**



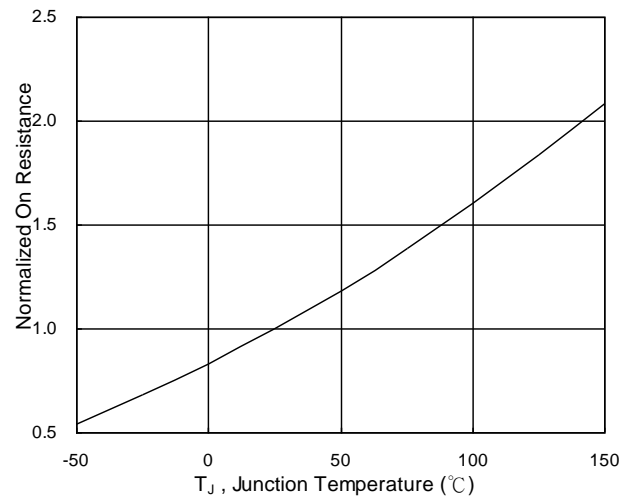
**Fig.3 Forward Characteristics of Reverse**



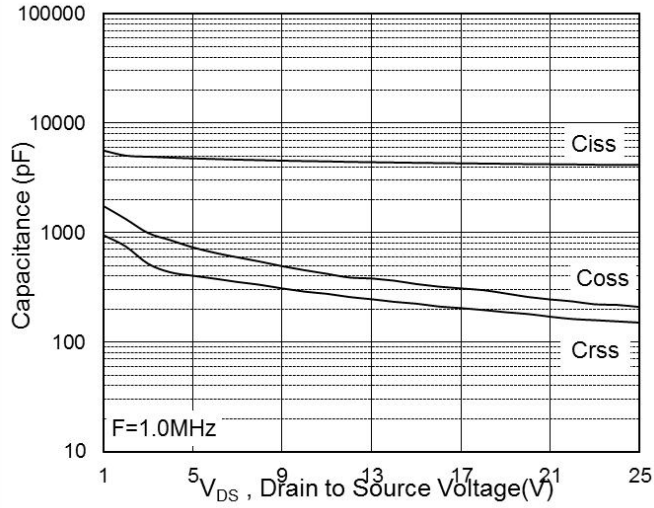
**Fig.4 Gate-Charge Characteristics**



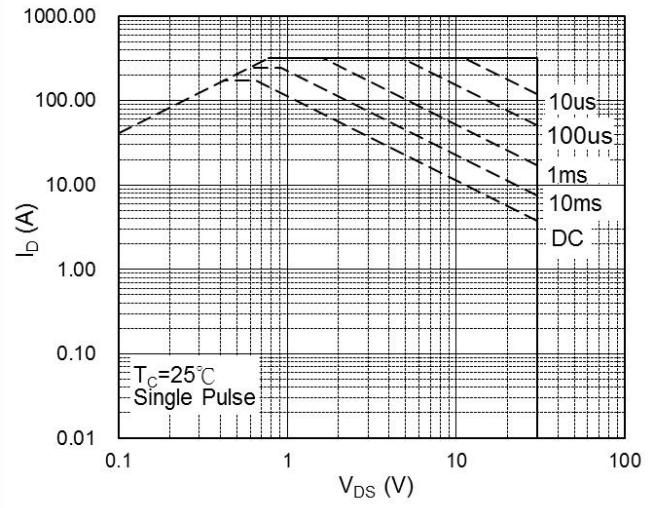
**Fig.5 Normalized V<sub>GS(th)</sub> v.s T<sub>J</sub>**



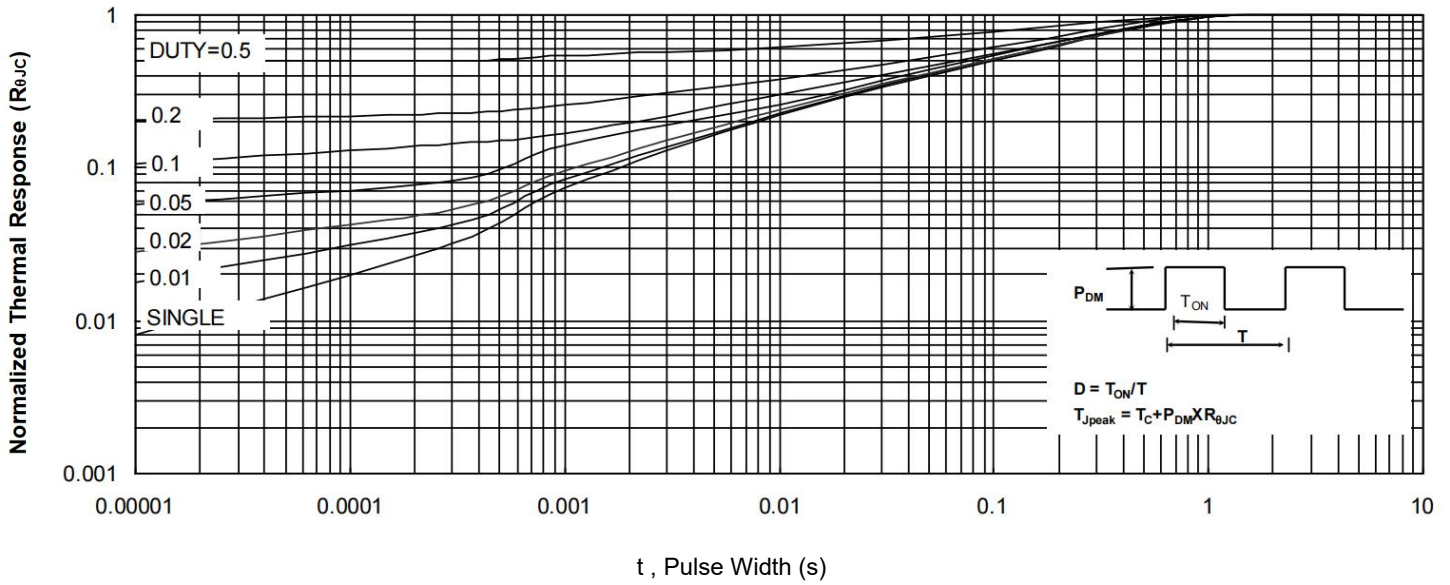
**Fig.6 Normalized R<sub>DS(on)</sub> v.s T<sub>J</sub>**



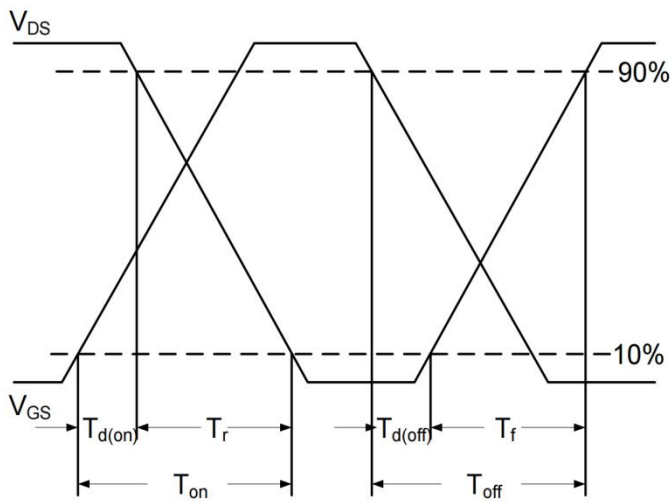
**Fig.7 Capacitance**



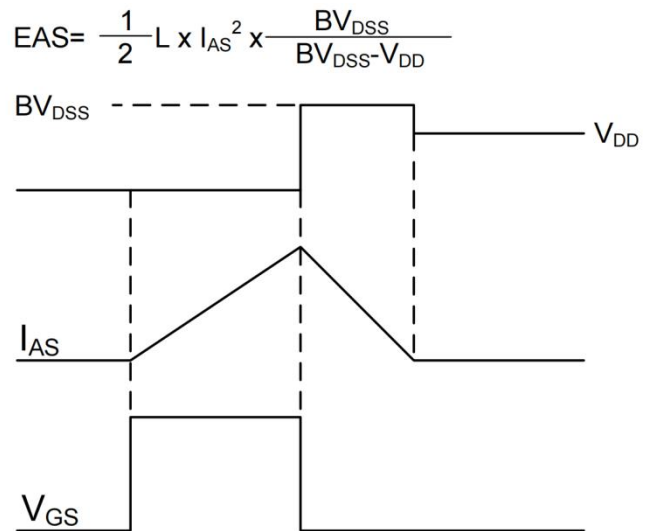
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

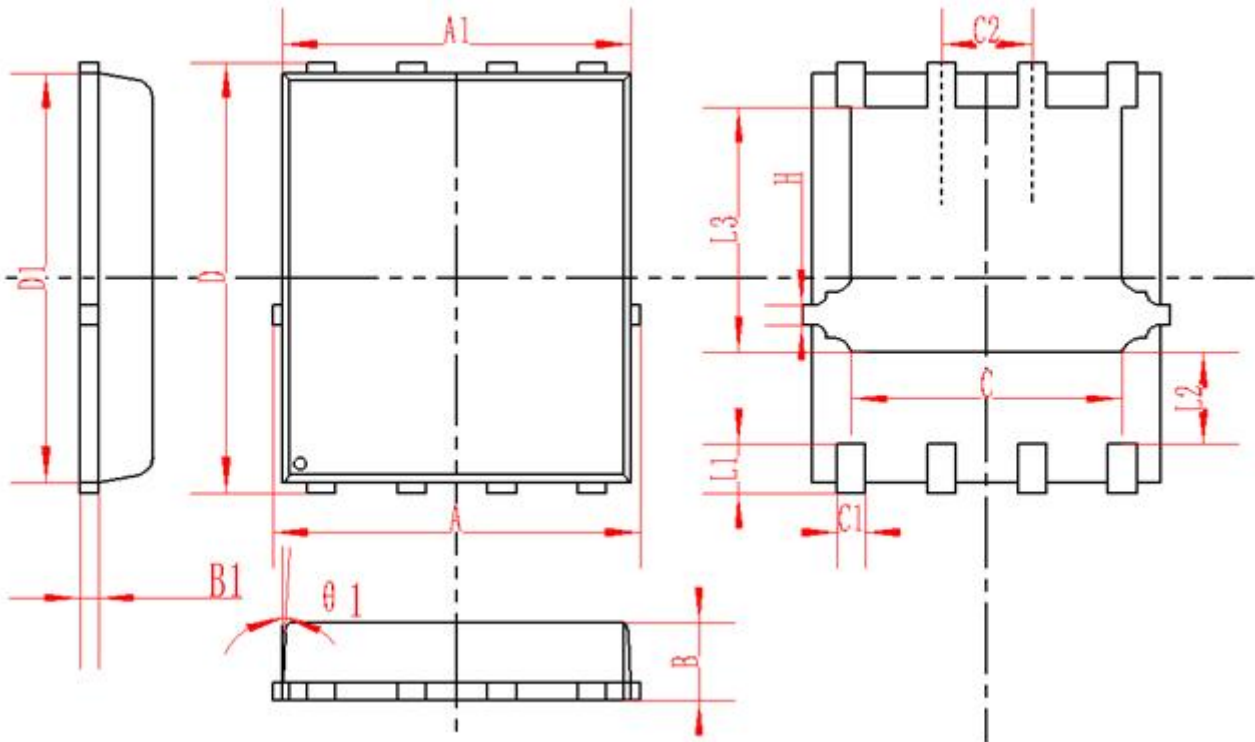


**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**

$$EAS = \frac{1}{2} L \times I_{AS}^2 \times \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

**DFN5X6-8L Package Information**


SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.95	5	5.05	0.195	0.197	0.199
A1	4.82	4.9	4.98	0.190	0.193	0.196
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.67	5.75	5.83	0.223	0.226	0.230
B	0.9	0.95	1	0.035	0.037	0.039
B1	0.254REF			0.010REF		
C	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2	1.27TYP			0.5TYP		
$\theta 1$	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
H	0.24	0.25	0.26	0.009	0.010	0.010

**REEL SPECIFICATION**

P/N	PKG	QTY
Si7850DP-MS	DFN5X6-8L	5000

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