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SEMICONDUCTOR



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## ULN2001D(MS)

Product specification

## GENERAL DESCRIPTION

The ULN2001D(MS) is high-voltage high-current Darlington transistor arrays each containing seven open collector common emitter pairs.

Each pair is rated at 500mA. Suppression diodes are included for inductive load driving, the inputs and outputs are pinned in opposition to simplify board layout.

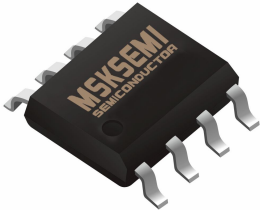
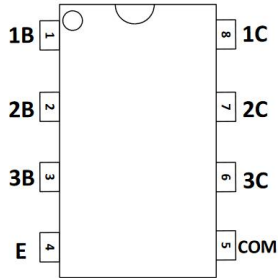
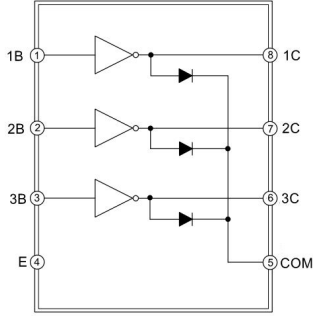

These devices are capable of driving a wide range of loads including solenoids, relays, DC motors, LED displays, filament lamps, thermal print-heads and high-power buffers.

The ULN2001D(MS) is available in both a small outline 8-pin package (SOP8 ).

## FEATURES

- 500-mA-Rated Collector Current(single output)
- High-Voltage Outputs:50V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications

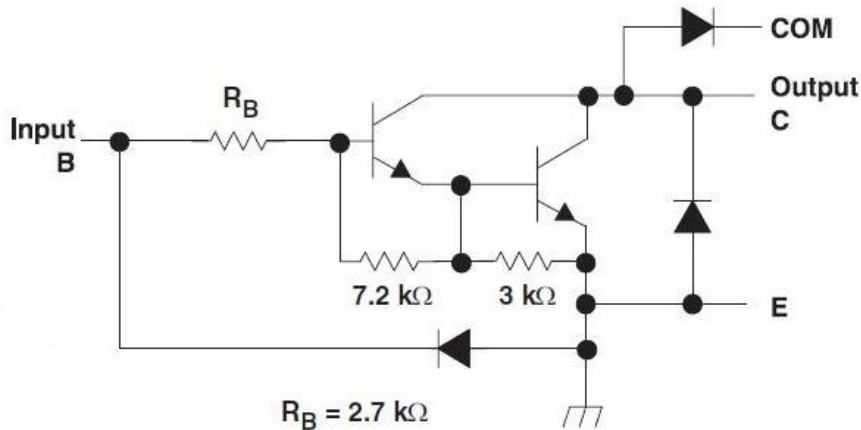
## Pin Configuration and Functions

PACKAGE OUTLINE	Pin Assignments	ConnectionDiagram	Marking
 <p>SOP-8</p>			 <p>Note: *****=batch</p>

## Pin Descriptions

Pin Number	Pin Name	Function
1	1B	Input pair1
2	2B	Input pair2
3	3B	Input pair3
4	E	Common Emitter (ground)
5	COM	Common Clamp Diodes
6	3C	Output pair3
7	2C	Output pair2
8	1C	Output pair1

**Functional Block Diagram**



Note: All resistor values shown are nominal.

The collector-emitter diode is a parasitic structure and should not be used to conduct current. If the collector(s) go below ground an external Schottky diode should be added to clamp negative undershoots.

**Absolute Maximum Ratings (1)**

At 25°C free-air temperature (unless otherwise noted)

Symbol	Parameter		Min	Max	Unit
V <sub>CC</sub>	Collector to emitter voltage			50	V
V <sub>R</sub>	Clamp diode reverse voltage(2)			50	V
V <sub>I</sub>	Input voltage(2)			30	V
I <sub>CP</sub>	Peak collector current	See typical characteristics		500	mA
I <sub>OK</sub>	Output clamp current			500	mA
I <sub>TE</sub>	Total emitter-terminal current			-2.5	A
T <sub>A</sub>	Operating free-air temperature range	TX2001D	-40	+105	°C
θ <sub>JA</sub>	Thermal Resistance Junction-to-Ambient(3)			63	°C/W
θ <sub>JC</sub>	Thermal Resistance Junction-to-Case(4)			12	
T <sub>J</sub>	Operating virtual junction temperature			+150	°C
T <sub>STG</sub>	Storage temperature range		-65	+150	°C
ESD	Human Body Mode		--	3000	V

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
- (3) Maximum power dissipation is a function of T<sub>J(max)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is PD = (T<sub>J(max)</sub> – T<sub>A</sub>)/θ<sub>JA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- (4) Maximum power dissipation is a function of T<sub>J(max)</sub>, θ<sub>JC</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is PD = (T<sub>J(max)</sub> – T<sub>A</sub>)/θ<sub>JC</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Collector to Emitter voltage	-	50	V
T <sub>A</sub>	Operating Ambient Temperature	-40	+105	°C

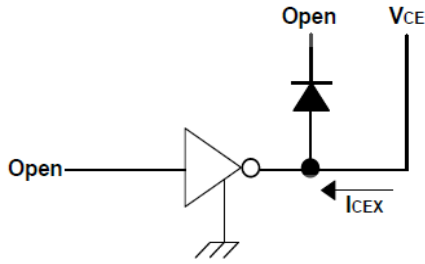
**Electrical Characteristics(TA=+25°C, unless otherwise specified)**

Parameter		Test Figure	Test Conditions		TX2001D			Unit
					MIN	TYP	MAX	
$V_{I(on)}$	On-state input voltage	Figure 6	VCE = 2 V	IC = 200 mA	--	--	2.4	V
				IC = 250 mA	--	--	2.7	
				IC = 300 mA	--	--	3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	Figure 5	II = 250 $\mu$ A,	IC = 100 mA	--	0.9	1.1	V
			II = 350 $\mu$ A,	IC = 200 mA	--	1	1.3	
			II = 500 $\mu$ A,	IC = 350 mA	--	1.2	1.6	
$I_{CEX}$	Collector cutoff current	Figure 1	VCE = 50 V,	II = 0	--	--	50	$\mu$ A
		Figure 2	VCE = 50 V, TA = +105°C	II = 0	--	--	100	
$V_F$	Clamp forward voltage	Figure 8	IF = 350 mA		--	1.7	2	V
$I_{I(off)}$	Off-state input current	Figure 3	VCE = 50 V, IC = 500 $\mu$ A		50	65	--	$\mu$ A
II	Input current	Figure 4	VI = 3.85 V		--	0.93	1.35	mA
IR	Clamp reverse current	Figure 7	VR = 50 V	TA = 25°C	--	--	50	$\mu$ A
				TA = 70°C	--	--	100	
Ci	Input capacitance		VI = 0, f = 1 MHz		--	15	25	pF

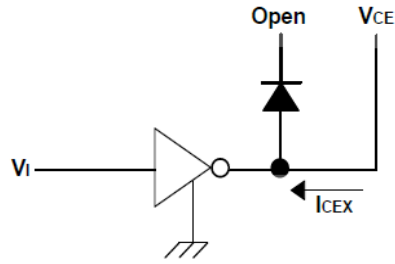
**Switching Characteristics (TA = +25°C, unless otherwise specified)**

Parameter		Test Conditions	TX2001D			UNIT
			MIN	TYP	MAX	
$t_{PLH}$	Propagation delay time, low- to high-level output	See Figure 9	--	0.25	1	$\mu$ s
$t_{PHL}$	Propagation delay time, high- to low-level output	See Figure 9	--	0.25	1	$\mu$ s
$V_{OH}$	High-level output voltage after switching	VS = 50 V, IO = 300 mA, See Figure 9	VS-20	--	--	mV

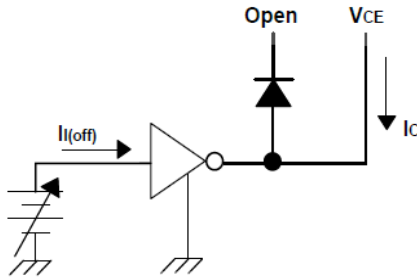
**Parameter Measurement Information**



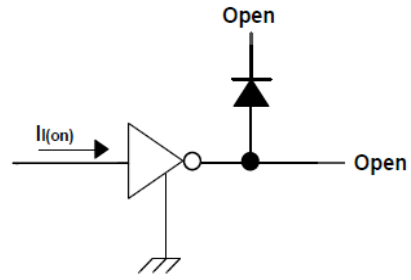
**Fig.1  $I_{CEX}$  Test Circuit**



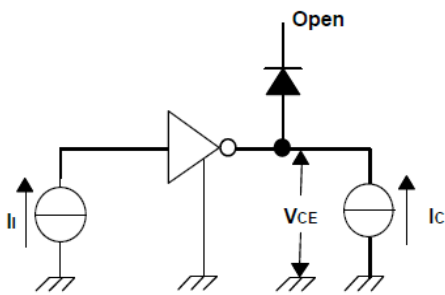
**Fig.2  $I_{CEX}$  Test Circuit**



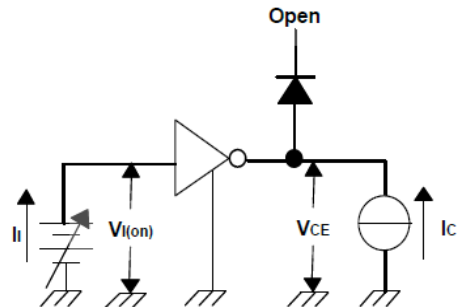
**Fig.3  $I_{I(off)}$  Test Circuit**



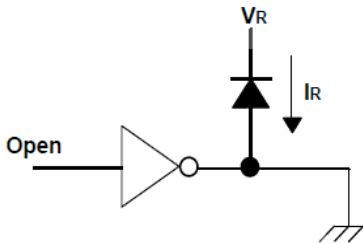
**Fig.4  $I_I$  Test Circuit**



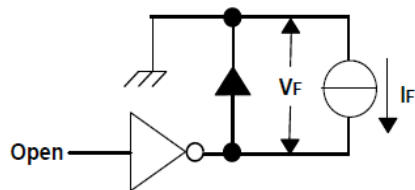
**Fig. 5  $h_{FE}$ ,  $V_{CE(sat)}$  Test Circuit**



**Fig. 6  $V_{I(on)}$  Test Circuit**



**Fig. 7  $I_R$  Test Circuit**



**Fig. 8  $V_F$  Test Circuit**

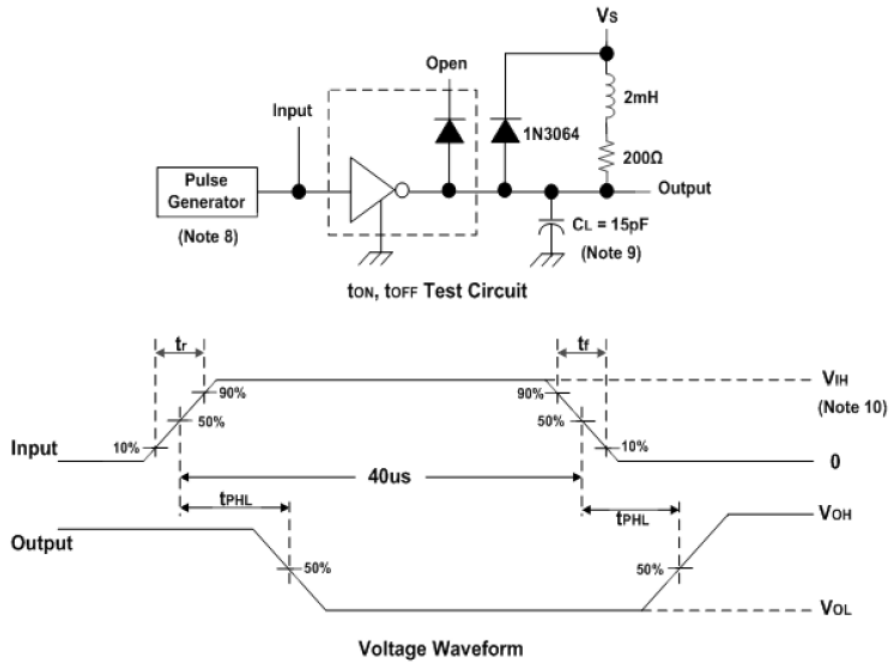


Fig. 9 Latch-Up Test Circuit and Voltage Waveform

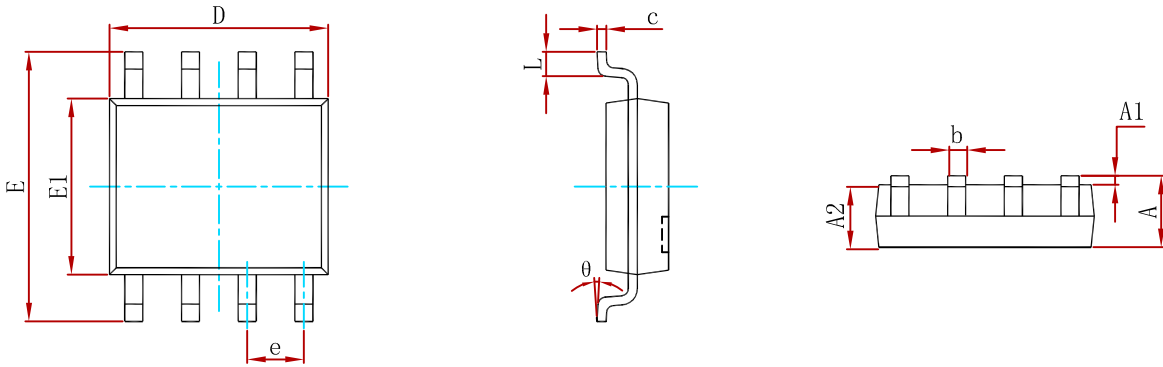
Notes: 8. The pulse generator has the following characteristics:

Pulse Width=12.5Hz, output impedance 50Ω,  $t_r \leq 5ns$ ,  $t_f \leq 10ns$ .

9.  $C_L$  includes probe and jig capacitance.

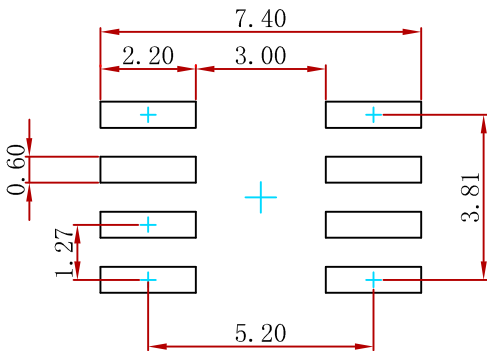
10.  $V_{IH} = 3V$

**PACKAGE MECHANICAL DATA**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°

**Suggested Pad Layout**



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance:  $\pm 0.05\text{mm}$ .  
 3. The pad layout is for reference purposes only.

**REEL SPECIFICATION**

P/N	PKG	QTY
ULN2001D(MS)	SOP-8	3500

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