# muRata

**Reference Specification** 

DES Series High Temperature Low Loss Lead Type Disc Ceramic Capacitors for General Purpose

Product specifications in this catalog are as of Dec. 2017, and are subject to change or obsolescence without notice.

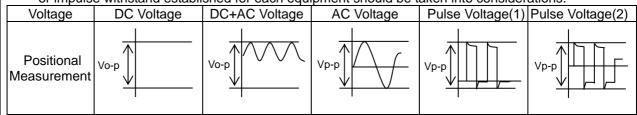
Please consult the approval sheet before ordering. Please read rating and Cautions first.

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# 1. OPERATING VOLTAGE

When DC-rated capacitors are to be used in AC or ripple current circuits, be sure to maintain the Vp-p value of the applied voltage or the Vo-p which contains DC bias within the rated voltage range. When the voltage is started to apply to the circuit or it is stopped applying, the irregular voltage may be generated for a transit period because of resonance or switching. Be sure to use a capacitor within rated voltage containing these irregular voltage.

When DC-rated capacitors are to be used in input circuits from commercial power source (AC filter), be sure to use Safety Recognized Capacitors because various regulations on withstand voltage or impulse withstand established for each equipment should be taken into considerations.



### 2. OPERATING TEMPERATURE AND SELF-GENERATED HEAT

Keep the surface temperature of a capacitor below the upper limit of its rated operating temperature range. Be sure to take into account the heat generated by the capacitor itself.

When the capacitor is used in a high-frequency current, pulse current or the like, it may have the selfgenerated heat due to dielectric-loss. The frequency of applied voltage should be in less than 300kHz in sine wave. Applied voltage should be the load such as self-generated heat is within 15 °C on the condition of atmosphere temperature 25 °C. When measuring, use a thermocouple of small thermal capacity-K of  $\phi$ 0.1mm and be in the condition where capacitor is not affected by radiant heat of other components and wind of surroundings. Excessive heat may lead to deterioration of the capacitor's characteristics and reliability.(Never attempt to perform measurement with the cooling fan running. Otherwise, accurate measurement cannot be ensured.)

#### 3. FAIL-SAFE

When capacitor would be broken, failure may result in a short circuit. Be sure to provide an appropriate fail-safe function like a fuse on your product if failure would follow an electric shock, fire or fume.

#### 4. LOAD REDUCTION AND SELF-GENERATED HEAT DURING APPLICATION OF HIGH-FREQUENCY AND HIGH-VOLTAGE

Since the heat generated by the low-dissipation capacitor itself is low, its allowable power is much higher than the general B characteristic. However, in case such an applied load that the self-heating temperature is 20 °C at the rated voltage, the allowable power may be exceeded.

Therefore, when using the low-dissipation capacitors in a high-frequency and high-voltage circuit with a frequency of 1kHz or higher, make sure that the Vp-p values including the DC bias, do not exceed the applied voltage value specified in Table 1. Also make sure that the self-heating temperature (the difference between the capacitor's surface temperature and the capacitor's ambient temperature) at an ambient temperature of 25 °C does not exceed the value specified in Table 1.

As shown in Fig. 2, the self-heating temperature depends on the ambient temperature. Therefore, if you are not able to set the ambient temperature to approximately 25 °C, please contact our sales representatives or product engineers.

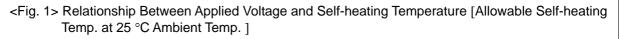
<	< Table 1> Allowable Conditions at High-frequency						
	Temp. Char.	DC	Allowable Condit	Capacitor's			
		Rated Applie	Applied Voltage	Self-heating Temp.	Ambient		
	Ghai.	Voltage	(max.)	(25 °C Ambient Temp.) *1	Temp. *2		
		500V	500Vp-p	15 °C max.			
	D	1kV 800Vp-p	15 °C max.	-25 to +85 °C			
		1kV 1000Vp-p		5 °C max	1		

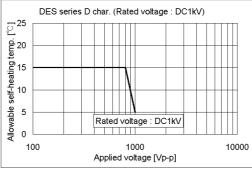
#### <Table 1> Allowable Conditions at High-frequency

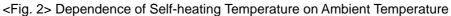
\*1 Fig. 1 shows the relationship between the applied voltage and the allowable self-heating temperature regarding 1kV rated voltage of the DES series D characteristic.

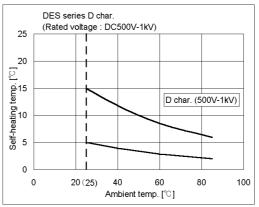
\*2 When the ambient temperature is 85 to 125 °C, the applied voltage needs to be further reduced. If the low-dissipation capacitors needs to be used at an ambient temperature of 85 to 125 °C, please contact our sales representatives or product engineers.

\*3 Fig. 3 shows reference data on the allowable voltage-frequency characteristic for a sine wave voltage.



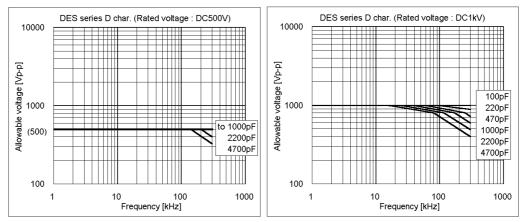






<Fig. 3> Allowable Voltage (Sine Wave Voltage) – Frequency Characteristic [At Ambient Temperature of 85 °C or less]

Because of the influence of harmonics, when the applied voltage is a rectangular wave or pulse wave voltage (instead of a sine wave voltage), the heat generated by the capacitor is higher than the value obtained by application of the sine wave with the same fundamental frequency. Roughly calculated for reference, the allowable voltage for a rectangular wave or pulse wave corresponds approximately to the allowable voltage for a sine wave whose fundamental frequency is twice as large as that of the rectangular wave or pulse wave. This allowable voltage, however, varies depending on the voltage and current waveforms. Therefore, you are requested to make sure that the self-heating temperature is not higher than the value specified in Table 1.



# 5. VIBRATION AND IMPACT

Do not expose a capacitor or its leads to excessive shock or vibration during use.

### 6. SOLDERING

When soldering this product to a PCB/PWB, do not exceed the solder heat resistance specification of the capacitor. Subjecting this product to excessive heating could melt the internal junction solder and may result in thermal shocks that can crack the ceramic element.

When soldering capacitor with a soldering iron, it should be performed in following conditions.

Temperature of iron tip : 400 °C max.

Soldering iron wattage : 50W max.

Soldering time : 3.5 s max.

#### 7. BONDING, RESIN MOLDING AND COATING

In case of bonding, molding or coating this product, verify that these processes do not affect the quality of capacitor by testing the performance of the bonded, molded or coated product in the intended equipment.

In case of the amount of applications, dryness / hardening conditions of adhesives and molding resins containing organic solvents (ethyl acetate, methyl ethyl ketone, toluene, etc.) are unsuitable, the outer coating resin of a capacitor is damaged by the organic solvents and it may result, worst case, in a short circuit.

The variation in thickness of adhesive, molding resin or coating may cause a outer coating resin cracking and/or ceramic element cracking of a capacitor in a temperature cycling.

#### 8. TREATMENT AFTER BONDING, RESIN MOLDING AND COATING

When the outer coating is hot (over 100  $^{\circ}$ C) after soldering, it becomes soft and fragile. So please be careful not to give it mechanical stress.

Failure to follow the above cautions may result, worst case, in a short circuit and cause fuming or partial dispersion when the product is used.

#### 9. OPERATING AND STORAGE ENVIRONMENT

The insulating coating of capacitors does not form a perfect seal; therefore, do not use or store capacitors in a corrosive atmosphere, especially where chloride gas, sulfide gas, acid, alkali, salt or the like are present. And avoid exposure to moisture. Before cleaning, bonding, or molding this product, verify that these processes do not affect product quality by testing the performance of a cleaned, bonded or molded product in the intended equipment. Store the capacitors where the temperature and relative humidity do not exceed -10 to 40 °C and 15 to 85%. Use capacitors within 6 months after delivered. Check the solderability after 6 months or more.

#### **10. LIMITATION OF APPLICATIONS**

Please contact us before using our products for the applications listed below which require especially high reliability for the prevention of defects which might directly cause damage to the third party's life, body or property.

- 1. Aircraft equipment
- 2. Aerospace equipment
- 3. Undersea equipment
- 4. Power plant control equipment
- 5. Medical equipment
- 6. Transportation equipment (vehicles, trains, ships, etc.)
- 7. Traffic signal equipment
- 8. Disaster prevention / crime prevention equipment
- 9. Data-processing equipment exerting influence on public
- 10. Application of similar complexity and/or reliability requirements to the applications listed in the above.

#### NOTICE

#### 1. CLEANING (ULTRASONIC CLEANING)

To perform ultrasonic cleaning, observe the following conditions. Rinse bath capacity : Output of 20 watts per liter or less. Rinsing time : 5 min maximum. Do not vibrate the PCB/PWB directly. Excessive ultrasonic cleaning may lead to fatigue destruction of the lead wires.

#### 2. CAPACITANCE CHANGE OF CAPACITORS

Capacitance might change greatly depending on a surrounding temperature or an applied voltage. So, it is not likely to be able to use for the time constant circuit. Please contact us if you need a detail information.

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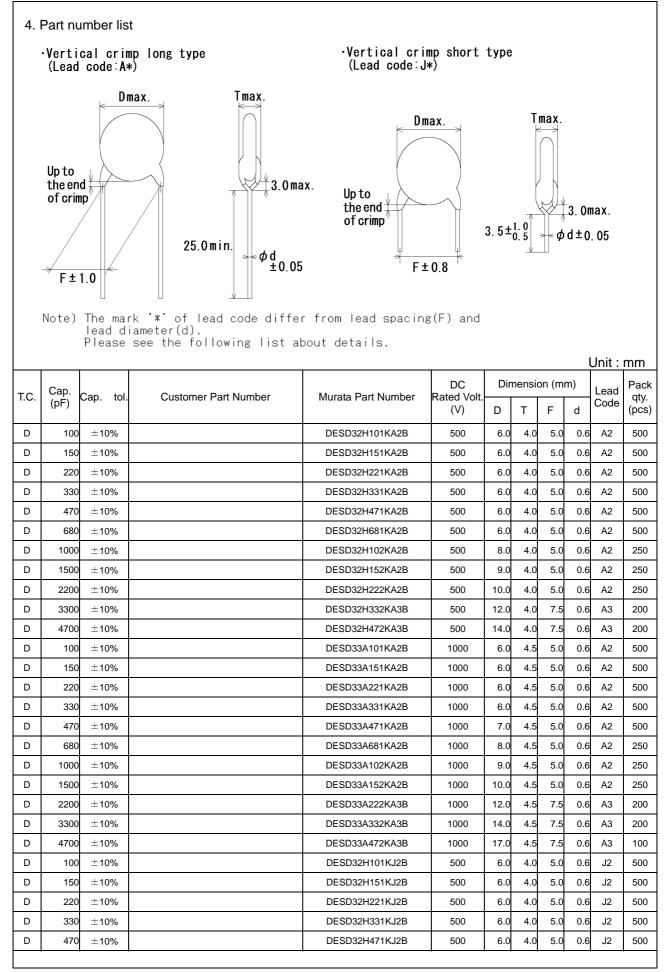
1.Please make sure that your product has been evaluated in view of your specifications with our product being mounted to your product.

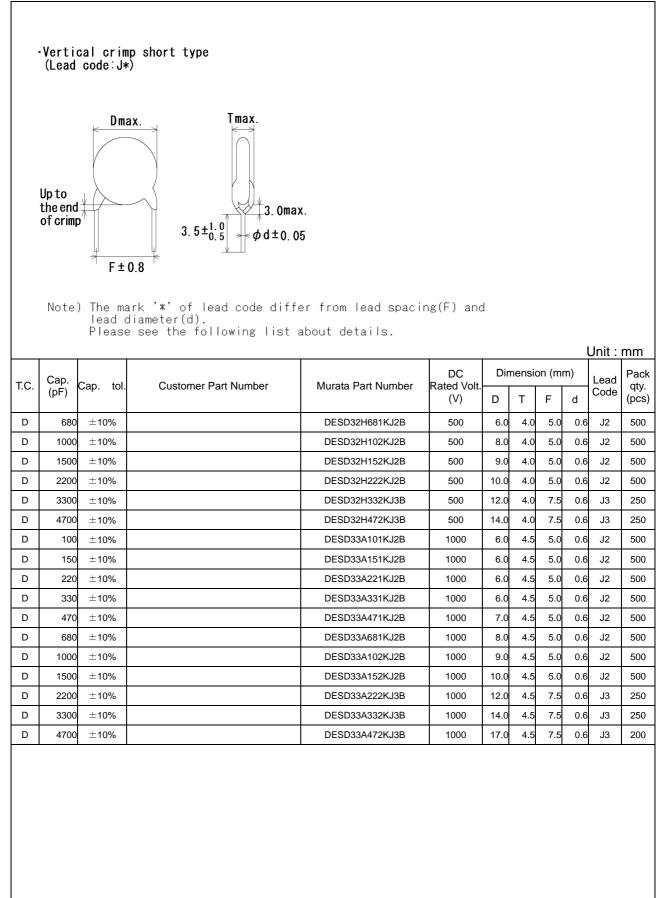
2. You are requested not to use our product deviating from this specification.

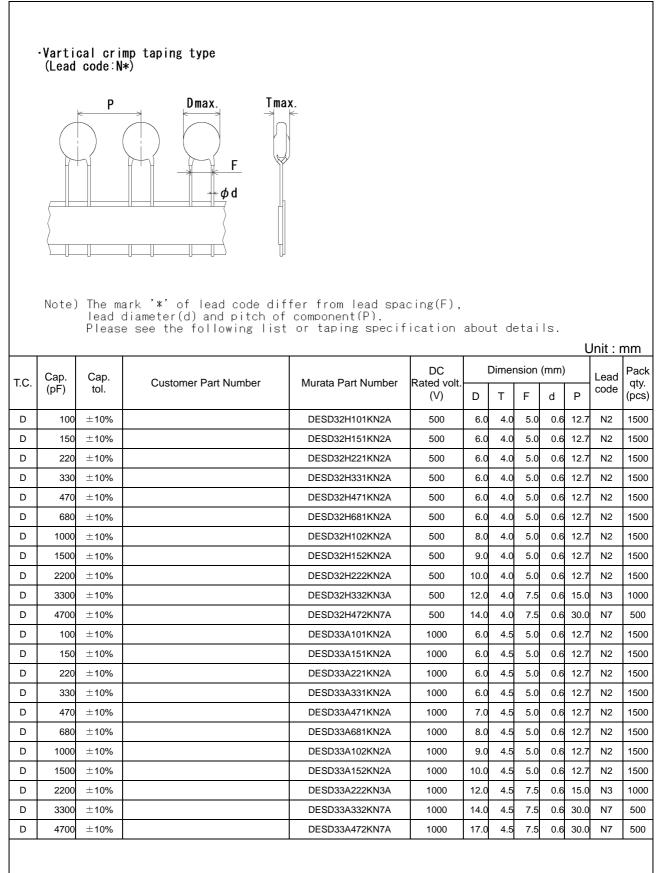
	se products in any automotive cles and plug-in hybrids.			<u> </u>	, , , , , , , , , , , , , , , , , , , ,
2. Rating					
2-1. Operating t -25	emperature range ~ +125°C				
2-2. Part numbe	er configuration				
ex.) <u>DES</u>	D3 3A	332 K	A3	В	
Series	Temperature Rated Ca	pacitance Capacitan			Individual
	characteristic voltage	tolerance	e code	style code	specification
•Tempera	ature characteristic				
[] [	Code	Temperature chara	cteristic		
	D3	D			
F	Please confirm detailed speci	fication on [ Specification	on and tes	t methods ].	
Deted					
Rated v	•	Rated voltage	10	7	
• Rated v	Code	Rated voltag	je	]	
• Capaci The ex.)	Code 2H 3A tance first two digits denote signific In case of 332. $33 \times 10^2 = 3300 \text{pF}$	DC500V DC1kV		the multiplic	er of 10 in pF.
• Capaci The ex.) • Capaci	Code 2H 3A tance first two digits denote signific In case of 332.	DC500V DC1kV cant figures ; the last dig		the multiplic	er of 10 in pF.
• Capaci The ex.) • Capaci	Code2H3Atancefirst two digits denote significIn case of 332. $33 \times 10^2 = 3300 \text{pF}$ tance tolerancease refer to [ Part number list	DC500V DC1kV cant figures ; the last dig		the multiplic	er of 10 in pF.
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• Capaci The ex.) • Capaci Plea	Code         2H         3A         tance         first two digits denote signific         In case of 332. $33 \times 10^2 = 3300 \text{pF}$ tance tolerance         ase refer to [ Part number list         ode         Code         A*         J*	DC500V DC1kV cant figures ; the last dig ]. ]. Vertical crimp long ty Vertical crimp short ty	git denotes	the multiplic	er of 10 in pF.
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• Capaci The ex.) • Capaci Plea • Lead co [ ] * Solo	Code         2H         3A         tance         first two digits denote signific         In case of 332. $33 \times 10^2 = 3300 \text{pF}$ tance tolerance         ase refer to [ Part number list         ode         Code         A*         J*         N*         Please refer to [ Part number         der coated copper wire is app	DC500V DC1kV cant figures ; the last dig ]. Lead style Vertical crimp long ty Vertical crimp short ty Vertical crimp taping er list ].	git denotes	the multiplie	er of 10 in pF.
• Capaci The ex.) • Capaci Plea • Lead co [ ] * Solo	Code         2H         3A         tance         first two digits denote signific         In case of 332. $33 \times 10^2 = 3300 \text{pF}$ tance tolerance         ase refer to [ Part number list         ode	DC500V DC1kV cant figures ; the last dig ]. Vertical crimp long ty Vertical crimp short ty Vertical crimp taping er list ].	git denotes	the multiplic	er of 10 in pF.
• Capaci The ex.) • Capaci Plea • Lead co [ ] * Solo	Code         2H         3A         tance         first two digits denote signific         In case of 332. $33 \times 10^2 = 3300 \text{pF}$ tance tolerance         ase refer to [ Part number list         ode         Code         A*         J*         N*         Please refer to [ Part number         der coated copper wire is app         g style code         Code	DC500V DC1kV cant figures ; the last dig ]. Lead style Vertical crimp long ty Vertical crimp short ty Vertical crimp taping er list ]. lied for termination. Packing type	git denotes	the multiplie	er of 10 in pF.
• Capaci The ex.) • Capaci Plea • Lead co [ ] * Solo	Code         2H         3A         tance         first two digits denote signific         In case of 332. $33 \times 10^2 = 3300 \text{pF}$ tance tolerance         ase refer to [ Part number list         ode         Code         A*         J*         N*         Please refer to [ Part number         der coated copper wire is app         g style code         B	DC500V DC1kV cant figures ; the last dig ]. Lead style Vertical crimp long ty Vertical crimp short ty Vertical crimp taping er list ]. lied for termination. Packing type	git denotes	the multiplic	er of 10 in pF.
• Capaci The ex.) • Capaci Plea • Lead co [ ] * Solo • Packing [ ] • Individu	Code         2H         3A         tance         first two digits denote signific         In case of 332. $33 \times 10^2 = 3300 \text{pF}$ tance tolerance         ase refer to [ Part number list         ode         Code         A*         J*         N*         Please refer to [ Part number         der coated copper wire is app         g style code         Code	DC500V DC1kV cant figures ; the last dig ]. Lead style Vertical crimp long ty Vertical crimp short ty Vertical crimp taping er list ]. lied for termination. Packing type Bulk type Ammo pack taping ty	git denotes		

# 3. Marking

Series code Temperature characteristic Nominal capacitance Capacitance tolerance Rated voltage Company name code Manufacturing year Manufacturing month	: Abbreviation (S) : Letter code : 3 digit system : Code(Omitted for maximum body diameter $\phi$ 6mm and under.) : Letter code(Omitted for the rated voltage DC500V.) : Abbreviation $\bigcirc$ (Omitted for maximum body diameter $\phi$ 9mm and under) : Letter code(The last digit of A.D. year.) : Code $\begin{pmatrix} Feb./Mar. \rightarrow 2 & Aug./Sep. \rightarrow 8 \\ Apr./May \rightarrow 4 & Oct./Nov. \rightarrow O \\ Jun./Jul. \rightarrow 6 & Dec./Jan. \rightarrow D \end{pmatrix}$
	(Example)







# **Reference only**

2   3   :	Ite Appearance and o Marking Dielectric strength		Specificatic No marked defect on form and dimensions. Please refer to [Part r To be easily legible. No failure.	appearance	for visible Dimension The capac DC voltag rated volta applied be (Charge/D The capac balls of dia shortcircu	citor should be in e evidence of defe- ons should be mea- citor should be in citor should not b ge of 200% of the age: DC1kV) or E age (In case of ra etween the lead w Discharge current citor is placed in	asured with slide of spected by naked be damaged when a rated voltage (In of DC voltage of 250% ated voltage: DC50% wires for 1 to 5 s. t≤50mA.) the container with that each lead wire	calipers eyes. case of % of the 00V) ar metal
2	Marking Dielectric	Between lead wires Body	form and dimensions. Please refer to [Part r To be easily legible. No failure.		for visible Dimension The capac DC voltag rated volta applied be (Charge/D The capac balls of dia shortcircu	e evidence of defensions should be mea citor should be in citor should not b ge of 200% of the age: DC1kV) or E age (In case of ra etween the lead w Discharge current citor is placed in iameter 1mm so t	ect. asured with slide of spected by naked be damaged when a rated voltage (In of DC voltage of 250% ated voltage: DC50 wires for 1 to 5 s. t≤50mA.) the container with that each lead wire	calipers eyes. case of % of the 00V) ar metal
4	Dielectric	wires	Please refer to [Part r To be easily legible. No failure.		Dimensior The capac DC voltag rated volta applied be (Charge/D The capac balls of dia shortcircu	Ins should be mean citor should be in citor should not b ge of 200% of the age: DC1kV) or E age (In case of ra etween the lead w Discharge current citor is placed in iameter 1mm so t	asured with slide of spected by naked be damaged when a rated voltage (In of DC voltage of 250% ated voltage: DC50% wires for 1 to 5 s. t≤50mA.) the container with that each lead wire	eyes. case of % of the 00V) ar metal
4	Dielectric	wires	To be easily legible. No failure.		The capac The capac DC voltag rated volta applied be (Charge/D The capac balls of dia shortcircu	citor should be in citor should not b ge of 200% of the age: DC1kV) or E age (In case of ra etween the lead v Discharge current citor is placed in iameter 1mm so t	spected by naked be damaged when a rated voltage (In of DC voltage of 250% ated voltage: DC50 wires for 1 to 5 s. t≤50mA.) the container with that each lead wire	eyes. case o % of th 00V) a metal
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4		wires			DC voltag rated volta rated volta applied be (Charge/D The capac balls of dia shortcircu	ge of 200% of the age: DC1kV) or E age (In case of ra etween the lead v Discharge current icitor is placed in iameter 1mm so t	e rated voltage (In 6 DC voltage of 2509 ated voltage: DC50 wires for 1 to 5 s. t≤50mA.) the container with that each lead wire	case o % of th 00V) a metal
4	en en gin	Body	No failure.		rated volta rated volta applied be (Charge/D The capac balls of dia shortcircu	age: DC1kV) or E age (In case of ra etween the lead w Discharge current icitor is placed in iameter 1mm so t	DC voltage of 2509 ated voltage: DC50 wires for 1 to 5 s. t≤50mA.) the container with that each lead wire	% of th 00V) a metal
		,	No failure.		rated volta applied be (Charge/D The capac balls of dia shortcircu	age (In case of ra etween the lead v Discharge current citor is placed in iameter 1mm so t	ated voltage: DC5( wires for 1 to 5 s. t≤50mA.) the container with that each lead wire	00V) a
		,	No failure.		applied be (Charge/D The capac balls of dia shortcircu	etween the lead w Discharge current icitor is placed in iameter 1mm so t	wires for 1 to 5 s. t≤50mA.) the container with that each lead wire	metal
		,	No failure.		(Charge/D The capac balls of dia shortcircu	Discharge current icitor is placed in iameter 1mm so t	t≤50mA.) the container with that each lead wire	
		,	No failure.		The capac balls of dia shortcircu	icitor is placed in iameter 1mm so t	the container with that each lead wire	
		,			balls of dia shortcircu	iameter 1mm so t	that each lead wire	
						lited, is kept abou		
					off the bal		ut 2mm	
						Ills as shown	V	
					in the figu		Ű.	
						/ (r.m.s.)<50/60H	z> / 🗍	,
						for 1 to 5 s	0000000	About 2
						capacitor lead		etal balls
						d small metals.		stai DällS
	Inculation	Potwoon lood	40.000140			Discharge current		od with
	Insulation	Between lead wires	10000MΩ min.				should be measure	ea with
	Resistance (I.R.) Capacitance	WIICS	Within encoified teler	2000		50V within 60±5 s		C
5	Capacitance		Within specified tolerance.				e measured at 20°	
_	Dissingtion Faster		0.3% max.			and AC5V(r.m.s.		
6	Dissipation Factor	(D.F.)					uld be measured a	it 20°C
-	Tamparatura abar	o otoriotio	Within +20/-30%			2kHz and AC5V(r		
7	Temperature char	acteristic					ment should be ma	ade at
			(Temp. range:-25 to +125°C)			specified in Tabl		
					be stored at $125\pm3^{\circ}$ C for 1 h, then placed at			
			*room condition for 2		24±2 h before initial measurements.			
			Stop		4	0 0		
			Step		1 2 3 4 5			
			Temp.(°C)		20±2 -25±3 20±2 125±2 20±2			
8 ;	Strength of lead	Pull	Lead wire should not cut off.		Ac chown	in the figure of r	ight, fix the body	
	Strength of lead	Full	Capacitor should not		of the can	pacitor and apply	a tensile weight	ПШ
				be broken.	gradually	to each lead wire	e in the radial	<del>(((Y</del>
						of the capacitor u		Ъ
						it for $10\pm1$ s.	1	w
			No marked defect		Each lead wire should be subjected to 5N of weigh and bent 90° at the point of egress, in one direction then returned to its original position and bent 90° in the opposite direction at the rate of one bend in 2 to 3 s.			
		Bending						
								d in 2 to
9 '	Vibration	Appearance						
-	Vibration Appearance resistance Capacitance		No marked defect. Within specified tolerance.		The capacitor should be firmly soldered to the supporting lead wire and vibrated at a frequency			
		Capacitance D.F.	0.3% max.	ance.	range of 10 to 55Hz, 1.5mm in total amplitude, with			
		D.F.	0.5 /0 IIIaX.		about a 1min rate of vibration change from 10Hz			
					to 55Hz and back to 10Hz. Apply for a total of 6 h;			
					2 h each in 3 mutually perpendicular directions.			
0	Solderability of lea	ads	Lead wire should be soldered		The lead wire of a capacitor should be dipped into			
	,		with uniformly coated	on the axial	ethanol solution of 25wt% rosin and then into molte			
			direction over 3/4 of the				cases the depth of	
			circumferential directi	ion.			from the root of lea	
					wires.			20
					Temp. of s	solder ·		
							der (Sn-3Ag-0.5Cu	u)
						C H63 Eutectic S		~)
"room	n condition" Temp	erature: 15 to 35%	C, Relative humidity: 45	to 75% Atm				
			e, . tolative numbery. To					

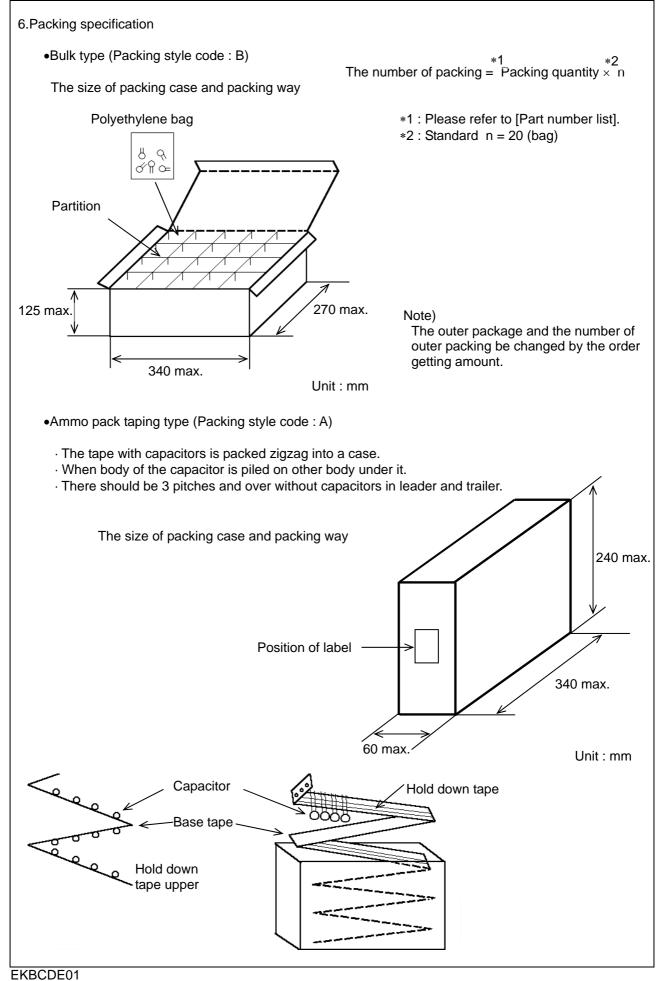
#### **Reference only**

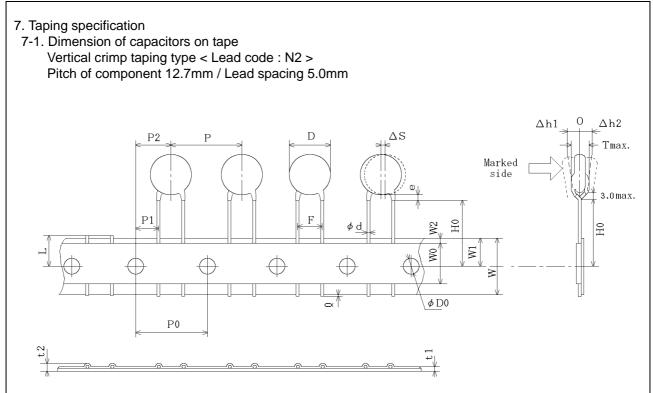
٧o.	<b>F</b> -		Reference of	
11	Iter		Specification	Test method
11	Soldering effect (Non-preheat)	Appearance	No marked defect.	The lead wire should be immersed into the melted
	(Non-preneat)	Capacitance	Within $\pm$ 10%	solder of 350±10°C up to about 1.5 to 2.0mm from
		change Dielectrie	Per item 3.	the main body for 3.5±0.5 s.
		Dielectric strength	Per liem 3.	Pre-treatment :
		(Between lead		Capacitor should be stored at 125±3°C for 1 h,
		wires)		then placed at *room condition for 24±2 h
		wires)		before initial measurements.
				Post-treatment :
				Capacitor should be stored for 24±2 h at *room
	0.11.1			condition.
12	Soldering effect	Appearance	No marked defect.	First the capacitor should be stored at 120+0/-5°C
	(On-preheat)	Capacitance	Within ± 10%	for 60+0/-5 s.
		change	Des iters 0	Then, as in figure, the lead wires should be
		Dielectric	Per item 3.	immersed solder of 260+0/-5°C up to 1.5 to 2.0mm from the root of terminal for 7.5+0/-1 s.
		strength		
		(Between lead		Thermal Capacitor
		wires)		insulating ()
				□
				// Molten
				solder
				Pre-treatment :
				Capacitor should be stored at 125±3°C for 1 h,
				then placed at *room condition for $24\pm 2$ h
				before initial measurements.
				Post-treatment :
				Capacitor should be stored for 24±2 h at *room
				condition.
13	Temperature	Appearance	No marked defect.	The capacitor should be subjected to 5 temperatur
-	cycle	Capacitance	Within ±10%	cycles.
	•	change		<temperature cycle=""></temperature>
		D.F.	0.4% max.	Step Temperature(°C) Time(min)
		I.R.	1 000MΩ min.	1 -25±3 30
		Dielectric	Per item 3.	2 Room Temp. 3
		strength		3 125±3 30
		(Between lead		4 Room Temp. 3
		wires)		
		,		Cycle time : 5 cycle
				Pre-treatment :
				Capacitor should be stored at 125±3°C for 1 h,
				then placed at *room condition for 24±2 h
				_ before initial measurements.
				Post-treatment :
				Capacitor should be stored for 24±2 h at *room
				condition.
	Humidity	Appearance	No marked defect.	Set the capacitor for 500 +24/-0 h at 40±2°C in 90
14		Capacitance	Within ±10%	to 95% relative humidity.
14	(Under steady			
14	(Under steady state)	change	0.40/	Pre-treatment :
14		change D.F.	0.4% max.	Capacitor should be stored at 125±3°C for 1 h,
14		change	0.4% max. 1 000MΩ min.	Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h
14		change D.F.		Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.
14		change D.F.		Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements. Post-treatment :
14		change D.F.		Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements. Post-treatment : Capacitor should be stored for 1 to 2 h at *room
	`state)	change D.F. I.R.	1 000MΩ min.	Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements. Post-treatment : Capacitor should be stored for 1 to 2 h at *room condition.
14		change D.F. I.R. Appearance	1 000MΩ min. No marked defect.	Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements. Post-treatment : Capacitor should be stored for 1 to 2 h at *room condition. Apply the rated voltage for 500 +24/-0 h at 40±2°C
	`state)	change D.F. I.R. Appearance Capacitance	1 000MΩ min.	Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements. Post-treatment : Capacitor should be stored for 1 to 2 h at *room condition. Apply the rated voltage for 500 +24/-0 h at 40±2°C in 90 to 95% relative humidity.
	`state)	change D.F. I.R. Appearance Capacitance change	1 000MΩ min. No marked defect. Within $\pm$ 10%	Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.         Post-treatment :         Capacitor should be stored for 1 to 2 h at *room condition.         Apply the rated voltage for 500 +24/-0 h at 40±2°C in 90 to 95% relative humidity.         (Charge/Discharge current≤50mA.)
	`state)	change D.F. I.R. Appearance Capacitance change D.F.	1 000MΩ min. No marked defect.	Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements. Post-treatment : Capacitor should be stored for 1 to 2 h at *room condition. Apply the rated voltage for 500 +24/-0 h at 40±2°C in 90 to 95% relative humidity.
	`state)	change D.F. I.R. Appearance Capacitance change	1 000MΩ min. No marked defect. Within $\pm$ 10%	Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.         Post-treatment :         Capacitor should be stored for 1 to 2 h at *room condition.         Apply the rated voltage for 500 +24/-0 h at 40±2°C in 90 to 95% relative humidity.         (Charge/Discharge current≤50mA.)
	`state)	change D.F. I.R. Appearance Capacitance change D.F.	1 000MΩ min. No marked defect. Within ±10% 0.6% max.	Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.         Post-treatment :         Capacitor should be stored for 1 to 2 h at *room condition.         Apply the rated voltage for 500 +24/-0 h at 40±2°C in 90 to 95% relative humidity.         (Charge/Discharge current≤50mA.)         Pre-treatment :
	`state)	change D.F. I.R. Appearance Capacitance change D.F.	1 000MΩ min. No marked defect. Within ±10% 0.6% max.	Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.         Post-treatment : Capacitor should be stored for 1 to 2 h at *room condition.         Apply the rated voltage for 500 +24/-0 h at 40±2°C in 90 to 95% relative humidity. (Charge/Discharge current≤50mA.)         Pre-treatment : Capacitor should be stored at 125±3°C for 1 h,
	`state)	change D.F. I.R. Appearance Capacitance change D.F.	1 000MΩ min. No marked defect. Within ±10% 0.6% max.	Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.         Post-treatment :         Capacitor should be stored for 1 to 2 h at *room condition.         Apply the rated voltage for 500 +24/-0 h at 40±2°C in 90 to 95% relative humidity.         (Charge/Discharge current≤50mA.)         Pre-treatment :         Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h
	`state)	change D.F. I.R. Appearance Capacitance change D.F.	1 000MΩ min. No marked defect. Within ±10% 0.6% max.	Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.         Post-treatment :         Capacitor should be stored for 1 to 2 h at *room condition.         Apply the rated voltage for 500 +24/-0 h at 40±2°C in 90 to 95% relative humidity.         (Charge/Discharge current≤50mA.)         Pre-treatment :         Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.
	`state)	change D.F. I.R. Appearance Capacitance change D.F.	1 000MΩ min. No marked defect. Within ±10% 0.6% max.	Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.         Post-treatment :         Capacitor should be stored for 1 to 2 h at *room condition.         Apply the rated voltage for 500 +24/-0 h at 40±2°C in 90 to 95% relative humidity.         (Charge/Discharge current≤50mA.)         Pre-treatment :         Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.
15	state)	change D.F. I.R. Appearance Capacitance change D.F. I.R.	1 000MΩ min. No marked defect. Within ±10% 0.6% max. 1 000MΩ min.	<ul> <li>Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.</li> <li>Post-treatment : Capacitor should be stored for 1 to 2 h at *room condition.</li> <li>Apply the rated voltage for 500 +24/-0 h at 40±2°C in 90 to 95% relative humidity.</li> <li>(Charge/Discharge current≤50mA.)</li> <li>Pre-treatment : Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.</li> <li>Post-treatment : Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.</li> </ul>
15	state)	change D.F. I.R. Appearance Capacitance change D.F. I.R.	1 000MΩ min. No marked defect. Within ±10% 0.6% max. 1 000MΩ min.	Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.         Post-treatment :         Capacitor should be stored for 1 to 2 h at *room condition.         Apply the rated voltage for 500 +24/-0 h at 40±2°C in 90 to 95% relative humidity.         (Charge/Discharge current≤50mA.)         Pre-treatment :         Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.         Post-treatment :         Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.
15	state)	change D.F. I.R. Appearance Capacitance change D.F. I.R.	1 000MΩ min. No marked defect. Within ±10% 0.6% max. 1 000MΩ min.	<ul> <li>Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.</li> <li>Post-treatment : Capacitor should be stored for 1 to 2 h at *room condition.</li> <li>Apply the rated voltage for 500 +24/-0 h at 40±2°C in 90 to 95% relative humidity.</li> <li>(Charge/Discharge current≤50mA.)</li> <li>Pre-treatment : Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.</li> <li>Post-treatment : Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.</li> </ul>
15	state)	change D.F. I.R. Appearance Capacitance change D.F. I.R.	1 000MΩ min. No marked defect. Within ±10% 0.6% max. 1 000MΩ min.	<ul> <li>Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.</li> <li>Post-treatment : Capacitor should be stored for 1 to 2 h at *room condition.</li> <li>Apply the rated voltage for 500 +24/-0 h at 40±2°C in 90 to 95% relative humidity.</li> <li>(Charge/Discharge current≤50mA.)</li> <li>Pre-treatment : Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.</li> <li>Post-treatment : Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.</li> </ul>
15	state)	change D.F. I.R. Appearance Capacitance change D.F. I.R.	1 000MΩ min. No marked defect. Within ±10% 0.6% max. 1 000MΩ min.	<ul> <li>Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.</li> <li>Post-treatment : Capacitor should be stored for 1 to 2 h at *room condition.</li> <li>Apply the rated voltage for 500 +24/-0 h at 40±2°C in 90 to 95% relative humidity.</li> <li>(Charge/Discharge current≤50mA.)</li> <li>Pre-treatment : Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.</li> <li>Post-treatment : Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h before initial measurements.</li> </ul>

# **Reference only**

No.	Ite	m	Specification	Test method
16	Life	Appearance	No marked defect.	Apply a DC voltage of 200% of the rated voltage
		Capacitance change	Within ±10%	(In case of rated voltage:DC500V) or DC voltage of 150% of the rated voltage (In case of rated
		D.F.	0.4% max.	voltage:DC1kV) for 1000 +48/-0 h at 125±2°C and
		I.R.	2000MΩ min.	relative humidity of 50% max (Charge/Discharge current≤50mA.) Pre-treatment : Capacitor should be stored at 125±3°C for 1 h,
				then placed at *room condition for 24±2 h before initial measurements. Post-treatment :
* "roc	m condition" Temp	rature: 15 to 35°	C Relative humidity: 45 to 75%	Capacitor should be stored at 125±3°C for 1 h, then placed at *room condition for 24±2 h. Atmospheric pressure: 86 to 106kPa

ESDES01A

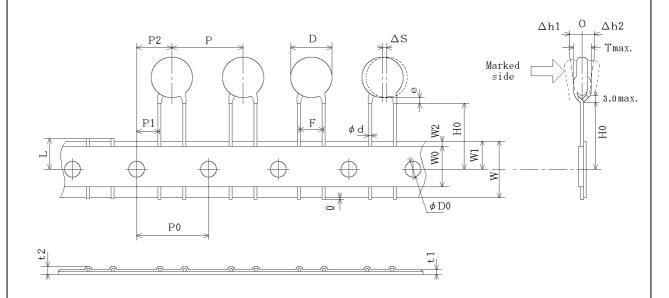




Unit : mm

ltem	Code	Dimensions	Remarks	
Pitch of component	Р	12.7±1.0		
Pitch of sprocket hole	P0	12.7±0.3		
Lead spacing	F	0.8 5.0±0.2		
Length from hole center to component center	P2	6.35±1.3		
Length from hole center to lead	P1	3.85±0.7	Deviation of progress direction	
Body diameter	D	Please refer to [P	art number list ].	
Deviation along tape, left or right	ΔS	0±1.0	They include deviation by lead bend .	
Carrier tape width	W	18.0±0.5		
Position of sprocket hole	W1	9.0±0.5	Deviation of tape width direction	
Lead distance between reference and bottom planes	HO	$18.0\pm^{2.0}_{0}$		
Protrusion length	Q	+0.5~-1.0		
Diameter of sprocket hole	φD0	4.0±0.1		
Lead diameter	φd	0.60±0.05		
Total tape thickness	t1	0.6±0.3	<u>_</u>	
Total thickness, tape and lead wire	t2	1.5 max.	They include hold down tape thickness	
Deviation across tape, front	∆h1	1.0		
Deviation across tape, rear	∆h2	1.0 max.		
Portion to cut in case of defect	L	11.0± <sup>0</sup> <sub>1.0</sub>		
Hold down tape width	W0	11.5 min.		
Hold down tape position	W2	1.5±1.5		
Coating extension on lead	е	Up to the end of c	rimp	
Body thickness	Т	Please refer to [Part number list ].		

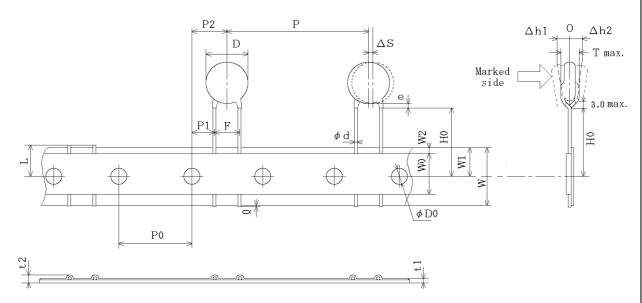
Vertical crimp taping type < Lead code : N3 > Pitch of component 15.0mm / Lead spacing 7.5mm



			Unit : mm
Item	Code	Dimensions	Remarks
Pitch of component	Р	15.0±2.0	
Pitch of sprocket hole	P0	15.0±0.3	
Lead spacing	F	7.5±1.0	
Length from hole center to component center	P2	7.5±1.5	
Length from hole center to lead	P1	3.75±1.0	Deviation of progress direction
Body diameter	D	Please refer to [	Part number list ].
Deviation along tape, left or right	ΔS	0±2.0	They include deviation by lead bend .
Carrier tape width	W	18.0±0.5	
Position of sprocket hole	W1	9.0±0.5	Deviation of tape width direction
Lead distance between reference and bottom planes	H0	$18.0\pm^{2.0}_{0}$	
Protrusion length	Q	+0.5~-1.0	
Diameter of sprocket hole	φD0	4.0±0.1	
Lead diameter	φd	0.60±0.05	
Total tape thickness	t1	0.6±0.3	
Total thickness, tape and lead wire	t2	1.5 max.	They include hold down tape thickness.
Deviation across tape, front	∆h1	0.0	
Deviation across tape, rear	∆h2	2.0 max.	
Portion to cut in case of defect	L	<b>11.0</b> ± <sup>0</sup> <sub>1.0</sub>	
Hold down tape width	W0	11.5 min.	
Hold down tape position	W2	1.5±1.5	
Coating extension on lead	е	Up to the end of	crimp
Body thickness	Т	Please refer to [	Part number list ].

Vertical crimp taping type < Lead code : N7 > Pitch of component 30.0mm /Lead spacing 7.5mm

Item



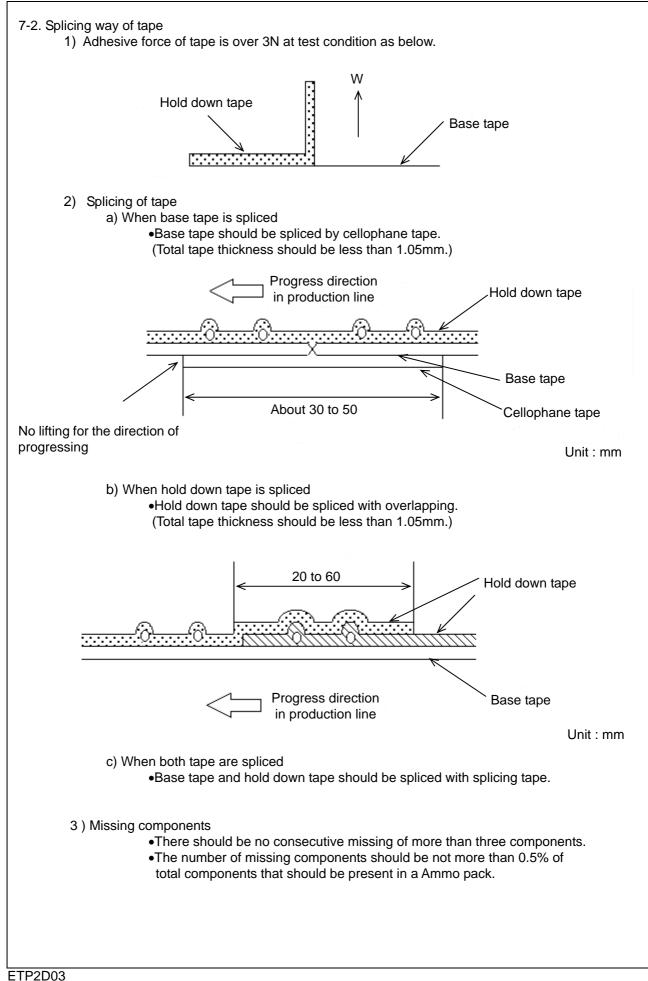
Dimensions

Code 

Remarks

Unit : mm

Rom	oouc	Billionolono	rtomanto	
Pitch of component	Р	30.0±2.0		
Pitch of sprocket hole	P0	15.0±0.3		
Lead spacing	F	7.5±1.0		
Length from hole center to component center	P2	7.5±1.5		
Length from hole center to lead	P1	3.75±1.0	Deviation of progress direction	
Body diameter	D	Please refer to [	Part number list ].	
Deviation along tape, left or right	ΔS	0±2.0	They include deviation by lead bend.	
Carrier tape width	W	18.0±0.5		
Position of sprocket hole	W1	9.0±0.5	Deviation of tape width direction	
Lead distance between reference and bottom	но	$18.0\pm^{2.0}_{0}$		
planes		10.0-0		
Protrusion length	Q	+0.5~-1.0		
Diameter of sprocket hole	φD0	4.0±0.1		
Lead diameter	φd	0.60±0.05		
Total tape thickness	t1	0.6±0.3	They include held down tone thickness	
Total thickness, tape and lead wire	t2	1.5 max.	They include hold down tape thickness	
Deviation across tape, front	∆h1	2.0 max.		
Deviation across tape, rear	∆h2			
Portion to cut in case of defect	L	<b>11.0</b> ± <sup>0</sup> <sub>1.0</sub>		
Hold down tape width	W0	11.5 min.		
Hold down tape position	W2	1.5±1.5		
Coating extension on lead	е	Up to the end of	crimp	
Body thickness	Т	Please refer to [ Part number list ].		



This products of the following crresponds to EU RoHS 当製品は以下の欧州RoHSに対応しています。

(1) RoHS

EU RoHs 2011/65/EC compliance 2011/65/EC(改正RoHS指令)に対応

maximum concentration values tolerated by weight in homogeneous materials

1000 ppm maximum Lead

1000 ppm maximum Mercury

•100 ppm maximum Cadmium

•1000 ppm maximum Hexavalent chromium

•1000 ppm maximum Polybrominated biphenyls (PBB)

•1000 ppm maximum Polybrominated diphenyl ethers (PBDE)

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