

Product Description

The **MYTNC1R86RELA2RA** is miniature UltraBK™ called “Ultra Block”, an ultra-thin high efficiency integrated power solution that combines a 6A DC/DC converter with components.

This totally integrated module provides up to 90.0% efficiency in a small and thin 10.5 x 9.0 x 2.1mm LGA package. Murata’s easy-to-use module terminal design allows simple power layout and maximum efficiency by minimizing routing parasitic resistance.

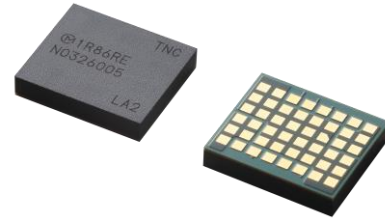
- Wide input voltage 6.0 to 14.4V
- Settable output voltage 0.7 to 1.8V
- Efficiency up to 90.0%
Up to 87.5% Efficiency with 12VIN/1.8VOUT/6A
- Up to 6A
- Ultra-thin/small 10.5 x 9.0 x 2.1mm LGA package
- Suitable to be place on the back side of PCB

Features

- Power-good output
- Over-current and Over-temperature protection
- Remote on/off control
- Output voltage sense
- I²C 6.0-compatible serial interface operating up to 1MHz.

Typical Applications

- PCIe / server applications
- FPGA and DSP
- Datacom / telecom systems
- Distributed bus architectures (DBA)
- Programmable logic and mixed voltage systems



Efficiency

T_a=25°C 12VIN 1.8VOUT

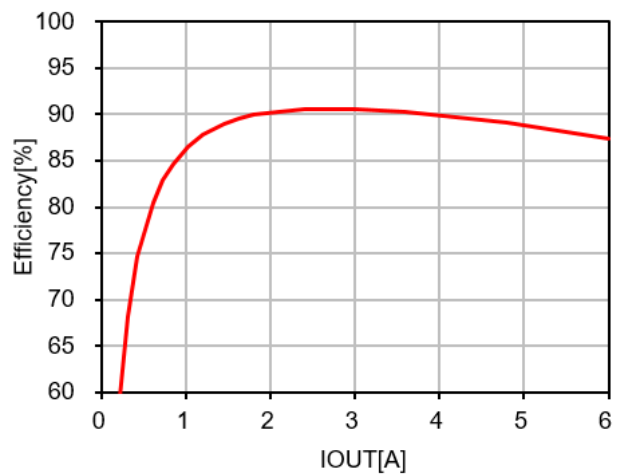


Figure 1. Efficiency Plot

Simplified Application Circuit

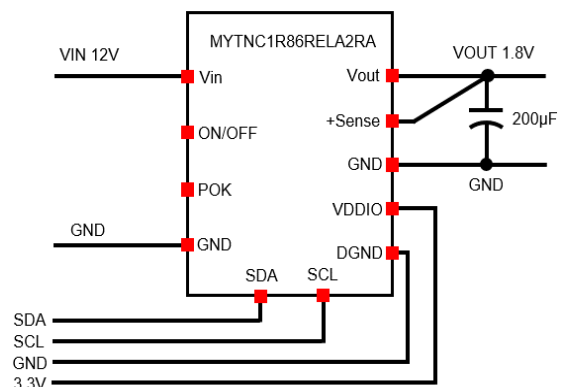




Figure 2. Simplified Circuit Diagram

UltraBK™ 6A DC-DC Converter Module

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Absolute Maximum Ratings⁽¹⁾⁽²⁾

| PARAMETER | MIN | MAX | UNITS |
|---|------|------|-------|
| Vin, ON/OFF Pin ⁽³⁾ | -0.3 | 16 | V |
| POK Pin, SCL, SDA, VDDIO | -0.3 | 5.5 | V |
| Storage Temperature | -40 | 125 | °C |
| Soldering / Reflow temperature ⁽⁴⁾ | - | 260 | °C |
| ESD Tolerance, HBM ⁽⁵⁾ | - | 1000 | V |

Notes:

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may extremely reduce device reliability.
- (2) All voltages are with respect to GND plane.
- (3) Do NOT exceed more than 0.3V from Vin voltage.
- (4) Recommended Reflow profile is written in "Soldering Guidelines".
- (5) Human body model, per the JEDEC standard JS-001-2012.

Table 1. Absolute Maximum Ratings

Recommended Operating Conditions⁽¹⁾

| PARAMETER | MIN | MAX | UNITS |
|------------------------------------|-----|------|-------|
| Input Voltage Range | 6.0 | 14.4 | V |
| Ambient Temperature ⁽²⁾ | -40 | 105 | °C |
| Junction Temperature | -40 | 120 | °C |
| Load Current | 0 | 6 | A |

Notes:

- (1) This module should be operated inside the recommended operating conditions. This module has been designed and tested on the assumption that it will be used under the recommended operating conditions. Operating in not recommended condition may reduce reliability of the module.
- (2) See the temperature derating curves in the thermal deratings. However, do not condensate.

Table 2. Recommended Operating Conditions

Package Thermal Characteristics⁽¹⁾⁽²⁾

| PARAMETER | | TYP | UNITS |
|-----------|--|------|-------|
| Θjcb-1 | Junction-case-bottom at heat Junction1 | 10.0 | °C/W |
| Θjcb-2 | Junction-case-bottom at heat Junction2 | 47.3 | °C/W |
| Θjct-1 | Junction-case-top at heat Junction1 | 64.9 | °C/W |
| Θjct-2 | Junction-case-top at heat Junction2 | 53.7 | °C/W |
| Θja | Junction-air | 19.9 | °C/W |

Notes:

- (1) Package thermal characteristics and performance are acquired and reported in according to the JEDEC standard JESD51-12. See "Fig. 40" below for more information on our measurement conditions.
- (2) Junction thermal resistance is a function not only of the internal parts, but it is also extremely sensitive to the environment which includes, but is not limited to, board thickness, number of layers, copper weight / routes, and air flow. Attention to the board layout is necessary to realize expected thermal performance.

Table 3. Package Thermal Characteristics

Electrical Characteristics

$V_{IN}=12V$, $V_{OUT}=1.8V$, $I_{OUT}=6A$, $T_a=+25^{\circ}C$, unless otherwise noted. The Electrical Characteristics table is based on the test circuit in Figure 35.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------|--|---------------------|------|------|-----------|
| INPUT SUPPLY | | | | | | |
| Input Voltage ⁽¹⁾ | VIN | | 6 | 12 | 14.4 | V |
| Input Voltage Start-up Slew rate ⁽³⁾ | VINSR | | Note ⁽²⁾ | - | 150 | V/ms |
| VIN Under Voltage Lockout Threshold - VIN rising ⁽³⁾ | VIUVH | | - | - | 5.45 | V |
| VIN Under Voltage Lockout Threshold - VIN falling ⁽³⁾ | VIUVL | | 4.5 | - | - | V |
| VIN Under Voltage Lockout Hysteresis | VIUVHYS | | - | 215 | - | mV |
| VIN Current Supply, Switching | IVINSW | No Load | - | 25 | - | mA |
| VIN Current Supply, Shutdown | IVINSD | VOUT=0V, ON/OFF=0V | - | 160 | - | μA |
| Remote ON/OFF Control (ON/OFF Pin) | | | | | | |
| Threshold High ⁽³⁾ | VTREH | Logic ON by pull-up or open of ON/OFF Pin | 1.1 | - | - | V |
| Threshold Low ⁽³⁾ | VTREL | Logic OFF by pull-down of ON/OFF Pin | - | - | 0.4 | V |
| ON/OFF Pin Leakage Current ⁽³⁾ | ILEN | VIN=14.4V, ON/OFF=0V, From Vin to ON/OFF | - | - | 200 | μA |
| CONVERTER | | | | | | |
| Efficiency | EFF | VIN=12.0V, VOUT=1.8V, IOUT=6A | - | 87.5 | - | % |
| | | VIN=12.0V, VOUT=1.2V, IOUT=6A | - | 85.5 | - | % |
| Charge Pump Switching Frequency | | Per a phase | - | 500 | - | kHz |
| Buck Converter Switching Frequency | | Per a phase | - | 1000 | - | kHz |
| Start-up Time | | VOUT=5 to 95% of VOUT VSET1[7:0]=01000110 SS[2:0]=100 | - | 6 | - | msec |
| POWER GOOD (POK Pin) | | | | | | |
| POK Sink Current ⁽³⁾ | | POK=0.4V | 4 | - | - | mA |
| POK Pin Leakage Current ⁽³⁾ | ILPG | POK=5V, POK=High | - | - | 1 | μA |
| POK & Output Under-Voltage | | VOUT falling (fault) | - | 90 | - | % of VOUT |
| | | VOUT rising (good) | - | 95 | - | |
| POK & Output Over-Voltage | | VOUT rising (fault) | - | 110 | - | % of VOUT |
| | | VOUT falling (good) | - | 105 | - | |
| THERMAL SHUTDOWN | | | | | | |
| Thermal Shutdown Threshold | TSD | Shutdown operating | - | 150 | - | °C |
| Thermal Shutdown Hysteresis | TSDHYS | | - | 20 | - | °C |
| OUTPUT | | | | | | |
| Output Voltage ⁽⁴⁾ | VOUT | Initial Setting (VDDIO=3.3V) | | 0.7 | | V |
| | | 9.6 ≤ VIN ≤ 14.4V | 0.7 | - | 1.8 | V |
| | | 7.0 ≤ VIN ≤ 14.4V | 0.7 | - | 1.35 | V |
| | | 6.0 ≤ VIN ≤ 14.4V | 0.7 | - | 1.0 | V |
| Output Voltage Accuracy ⁽¹⁾⁽⁵⁾ | | 6.0 ≤ VIN ≤ 14.4V 0.7 ≤ VOUT ≤ 1.8V ⁽⁴⁾ 0 ≤ IOUT ≤ 6A | -3 | - | +3 | % |
| Temperature variation ⁽³⁾ | | -40 ≤ Ta ≤ 105°C | - | 1 | - | % |
| Total Output Voltage Accuracy ⁽³⁾ | | 0.7 ≤ VOUT ≤ 1.8V ⁽⁴⁾ 0 ≤ IOUT ≤ 6A -40 ≤ Ta ≤ 105°C | -3 | - | +3 | % |

$V_{IN}=12V$, $V_{OUT}=1.8V$, $I_{OUT}=6A$, $T_a=+25^{\circ}C$, unless otherwise noted. The Electrical Characteristics table is based on the test circuit in Figure 35.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|---|-----------------|--|-------------------------|-----------|----------------|--------------|---------|
| Output Current ⁽¹⁾ | IOUT | | 0 | - | 6 | A | |
| Current Limit Inception | | | - | 11 | - | A | |
| Current Limit Method | | | Hiccup | | | | |
| Line Regulation ⁽³⁾⁽⁵⁾ | | $V_{IN}=\text{min. to max.}$ | -1 | - | +1 | % | |
| Load Regulation ⁽³⁾⁽⁵⁾ | | $I_{OUT}=\text{min. to max.}$ | -1 | - | +1 | % | |
| Dynamic Load Peak Deviation | | $I_{OUT}=50\text{-}100\%$, $SR=1.0A/\mu s$ | - | ± 3.0 | - | % | |
| Ripple and Noise ⁽³⁾⁽⁵⁾ (20MHz bandwidth) | | $6.0V \leq V_{IN} \leq 14.4V$ $0.7V \leq V_{OUT} \leq 1.8V^{(4)}$ $0 \leq I_{OUT} \leq 6A$ | - | - | 40 | mV pk-pk | |
| | | $V_{IN}=12.0V$ $0.7 \leq V_{OUT} \leq 1.8V^{(4)}$ $I_{OUT}=6A$ | - | 1 | - | % of Vout | |
| External Output Capacitance Range ⁽³⁾ | COUT | $6.0 \leq V_{IN} \leq 14.4V$ $0.7 \leq V_{OUT} \leq 1.8V^{(4)}$ $0 \leq I_{OUT} \leq 6A$ | SS[2:0] =000 | 200 | - | 600 | μF |
| | | | SS[2:0] =001 | | | 1200 | |
| | | | Other than the above | | | 2000 | |
| TELEMETRY | | | | | | | |
| Average Output Voltage Sense Measurement Time | | 12-bit ADC resolution | - | 512 | - | μs | |
| Output Voltage Sense Refresh Rate | | | - | 1.5 | - | ms | |
| Output Voltage Sense Measurement Resolution | | | - | 1 | - | mV | |
| Output Voltage Sense Measurement Accuracy | | | - | ± 1 | - | % | |
| Average Input Voltage Sense Measurement Time | | 8-bit ADC resolution | - | 1.5 | - | ms | |
| Input Voltage Sense Refresh Rate | | | - | 1.5 | - | ms | |
| Input Voltage Sense Measurement Resolution | | | - | 80 | - | mV | |
| Input Voltage Sense Measurement Accuracy | | | - | ± 2 | - | % | |
| Average TEMP sensor Measurement Time | | 12-bit ADC resolution | - | 4 | - | ms | |
| TEMP sensor Refresh Rate | | | - | 128 | - | μs | |
| TEMP sensor Measurement Resolution | | | - | 0.5 | - | $^{\circ}C$ | |
| TEMP sensor ⁽⁶⁾ Measurement Accuracy | | | - | ± 3 | - | $^{\circ}C$ | |
| Average Output Current Sense Measurement Time | | 12-bit ADC resolution | - | 512 | - | μs | |
| | | 8-bit ADC resolution | | 128 | | | |
| Output Current Sense Refresh Rate | | | - | 128 | - | μs | |
| Output Current Sense Measurement Accuracy | | | - | ± 4 | - | % | |
| Output Current Sense Measurement Resolution | | 12-bit ADC resolution | - | 25 | - | mA | |
| | | 8-bit ADC resolution | | 40 | | | |
| I²C SERIAL INTERFACE(SCL, SDA, VDDIO) | | | | | | | |
| VDDIO Supply Voltage | VDDIO | | 1.08 | - | 5.5 | V | |
| SDA, SCL Input High Voltage | V _{IH} | | 0.7 x VDDIO | - | - | V | |
| SDA, SCL Input Low Voltage | V _{IL} | | - | - | 0.3 x VDDIO | V | |

$V_{IN}=12V$, $V_{OUT}=1.8V$, $I_{OUT}=6A$, $T_a=+25^{\circ}C$, unless otherwise noted. The Electrical Characteristics table is based on the test circuit in Figure 35.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------------------|---|-----------------|-----|------|---------|
| SDA, SCL Input Hysteresis | V_{HYS} | | 0.05 x VDDIO | - | - | V |
| SDA, SCL Input Current | I_{SCL}, I_{SDA} | | -1 | - | 1 | μA |
| SDA Output Low Level | V_{OL} | ISDA=20mA | - | - | 0.4 | V |
| I ² C Interface Initial Wait Time | | Initial wait time from EN logic high to 1 st I ² C command accepted | 1000 | - | - | μs |
| MTP Non-Volatile Memory Write Cycle Time | | | - | 34 | 50 | ms |
| SDA, SCL Pin Capacitance ⁽³⁾ | $C_{I/O}$ | | - | - | 10 | pF |
| I²C INTERFACE TIMING CHARACTERISTICS FOR STANDARD MODE AND FAST MODE PLUS | | | | | | |
| Serial Clock Frequency | F_{SCL} | Standard mode | - | - | 100 | kbits/s |
| | | Fast mode | - | - | 400 | kbits/s |
| | | Fast mode plus | - | - | 1 | Mbits/s |
| Clock Low Period | T_{LOW} | Standard mode | 4.7 | - | - | μs |
| | | Fast mode | 1.3 | - | - | μs |
| | | Fast mode plus | 0.5 | - | - | μs |
| Clock High Period | T_{HIGH} | Standard mode | 4 | - | - | μs |
| | | Fast mode | 600 | - | - | ns |
| | | Fast mode plus | 260 | - | - | ns |
| BUS Free Time between a STOP a START Condition | T_{BUF} | Standard mode | 4.7 | - | - | μs |
| | | Fast mode | 1.3 | - | - | μs |
| | | Fast mode plus | 0.5 | - | - | μs |
| Setup Time for a Repeated START Condition | $T_{SU:STA}$ | Standard mode | 4.7 | - | - | μs |
| | | Fast mode | 600 | - | - | ns |
| | | Fast mode plus | 260 | - | - | ns |
| Hold Time for a Repeated START Condition | $T_{HD:STA}$ | Standard mode | 4 | - | - | μs |
| | | Fast mode | 600 | - | - | ns |
| | | Fast mode plus | 260 | - | - | ns |
| Setup Time of STOP condition | $T_{SU:STO}$ | Standard mode | 4 | - | - | μs |
| | | Fast mode | 600 | - | - | ns |
| | | Fast mode plus | 260 | - | - | ns |
| Data Setup Time | $T_{SU:DAT}$ | Standard mode | 250 | - | - | ns |
| | | Fast mode | 100 | - | - | ns |
| | | Fast mode plus | 50 | - | - | ns |
| Data Hold Time | $T_{HD:DAT}$ | Standard mode | 0 | - | - | μs |
| | | Fast mode | 0 | - | - | ns |
| | | Fast mode plus | 0 | - | - | ns |
| Rise Time of SDA and SCL signals | T_R | Standard mode | - | - | 1000 | ns |
| | | Fast mode | 20 | - | 300 | ns |
| | | Fast mode plus | - | - | 120 | ns |
| Fall time of SDA and SCL Signals | T_F | Standard mode | - | - | 300 | ns |
| | | Fast mode | 20 x VDDIO/5.5V | - | 300 | ns |
| | | Fast mode plus | 20 x VDDIO/5.5V | - | 120 | ns |
| Data Valid Time | T_{VD} | Standard mode | - | - | 3.45 | μs |
| | | Fast mode | - | - | 900 | ns |

$V_{IN}=12V$, $V_{OUT}=1.8V$, $I_{OUT}=6A$, $T_a=+25^{\circ}C$, unless otherwise noted. The Electrical Characteristics table is based on the test circuit in Figure 35.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|-----------|----------------|-----|-----|------|---------|
| | | Fast mode plus | - | - | 450 | ns |
| Data Valid Acknowledge Time | T_{VDA} | Standard mode | - | - | 3.45 | μs |
| | | Fast mode | - | - | 900 | ns |
| | | Fast mode plus | - | - | 450 | ns |
| Capacitive Load for SDA and SCL | C_{BUS} | Standard mode | - | - | 400 | pF |
| | | Fast mode | - | - | 400 | pF |
| | | Fast mode plus | - | - | 550 | pF |

Notes:

- (1) Min/Max specifications are 100% production tested at $T_a=25^{\circ}C$, unless otherwise noted. Limits over the operating range are guaranteed by design.
- (2) See the section of "Limitation of Input Voltage slew rate".
- (3) Guaranteed by design.
- (4) See the Output Voltage Range of fig.9.
- (5) Only statics state.
- (6) The temperature of TEMP sensor includes some error from the surface temperature.

Table 4. Electrical Characteristics

Pin Configuration

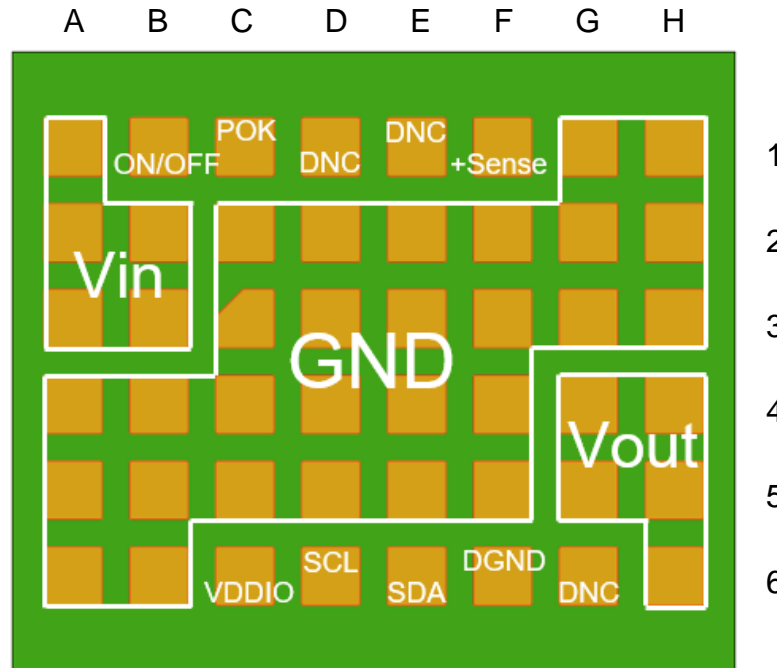


Figure 3. Module Terminal (Top View)

Pin Descriptions

| PIN NO. | NAME | DESCRIPTION |
|--|--------|--|
| A1-A3, B2-B3 | Vin | Input Voltage pins. Apply input voltage between these pins and GND pins. |
| A4-A6, B4-B6, C2-C5, D2-D5, E2-E5, F2-F5, G1-G3, H1-H3 | GND | Ground pins. Connect to the GND plane. |
| B1 | ON/OFF | Remote ON/OFF pin. The pin is connected to Vin through the internal resistance. |
| C1 | POK | Power Good pin. The function is operated by internal open-drain FET. |
| D1, E1, G6 | DNC | Do not connection pins. Those pins must be connect to floating individually. |
| F6 | DGND | Digital ground pin. Connect to I ² C signal GND. |
| E6 | SDA | I ² C Serial bus data input/output pin. |
| D6 | SCL | I ² C Serial bus clock input pin. |
| G4-G5, H4-H6 | Vout | Output pins. Connect the output load between these pins and Ground pins. Place external bypass capacitors as close as possible to these pins to reduce parasitic inductance. |
| C6 | VDDIO | Digital I/O supply voltage for I ² C interface. |
| F1 | +Sense | Output Voltage Sensing pin. Connect to an output near the load to improve load regulation. This pin must be connected to output near the load, or at the module pins. |

Table 5. Pin Descriptions

Functional Block Diagram

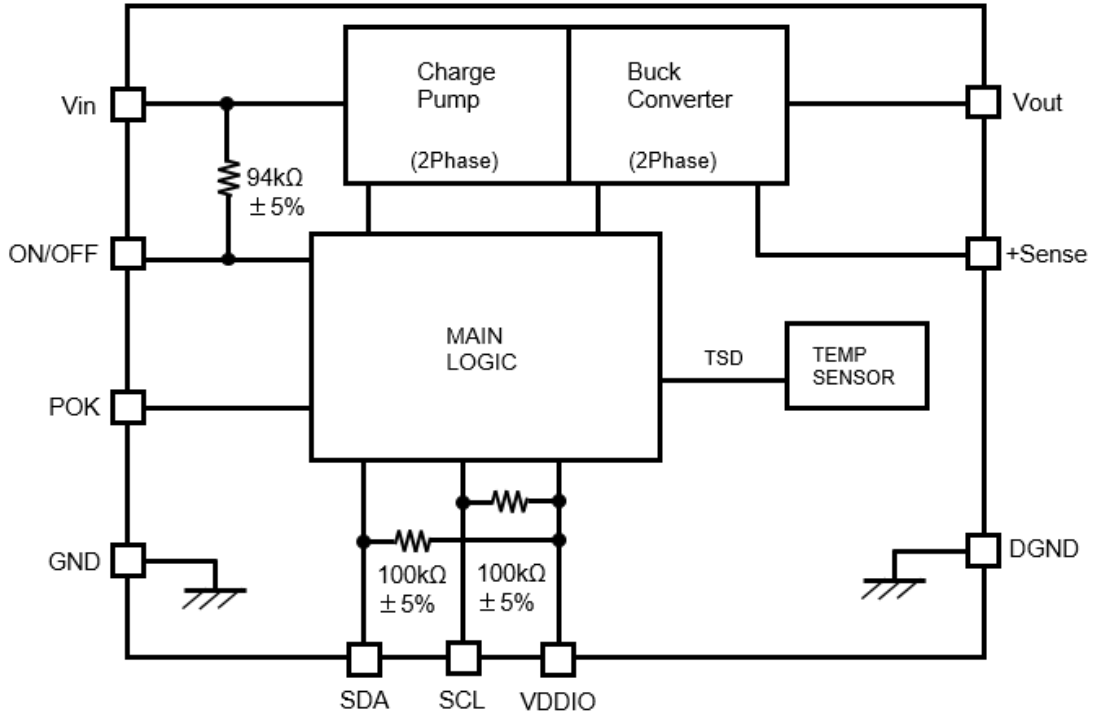


Figure 4. Functional Block Diagram

Typical Performance Characteristics

(VIN=12V Ta=25°C)

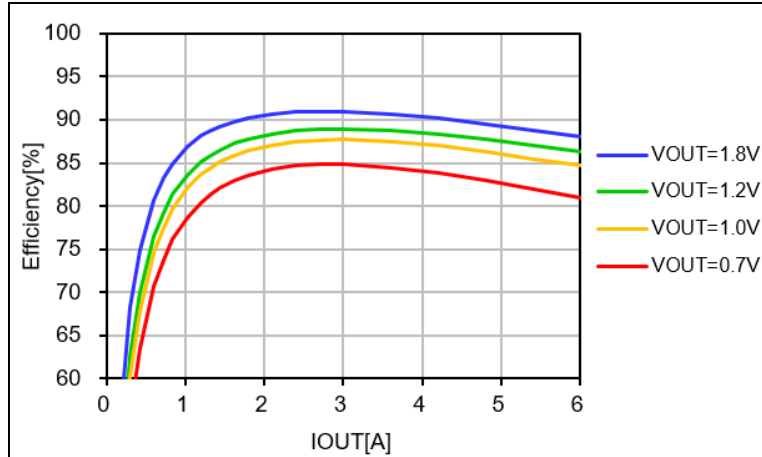


Figure 5. Efficiency vs. Load Current and Output Voltage

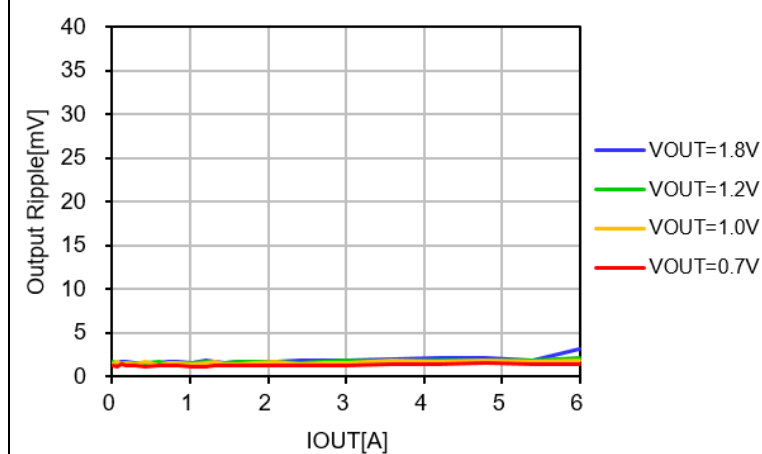


Figure 6. Output Ripple vs. Load Current and Output Voltage
(COUT=200μF, ScopeBW=20MHz)

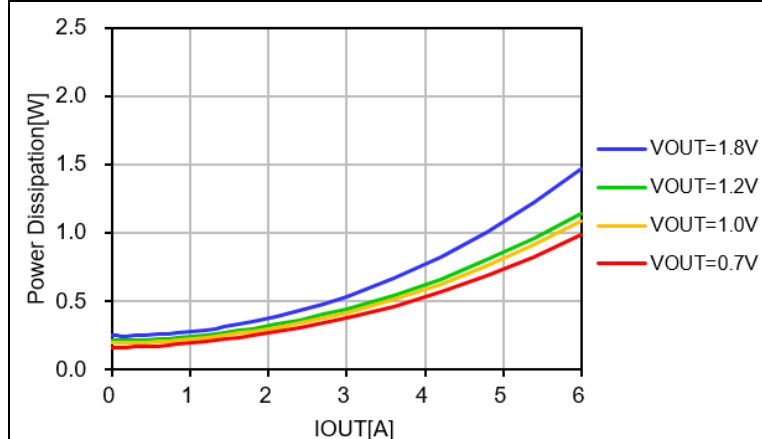
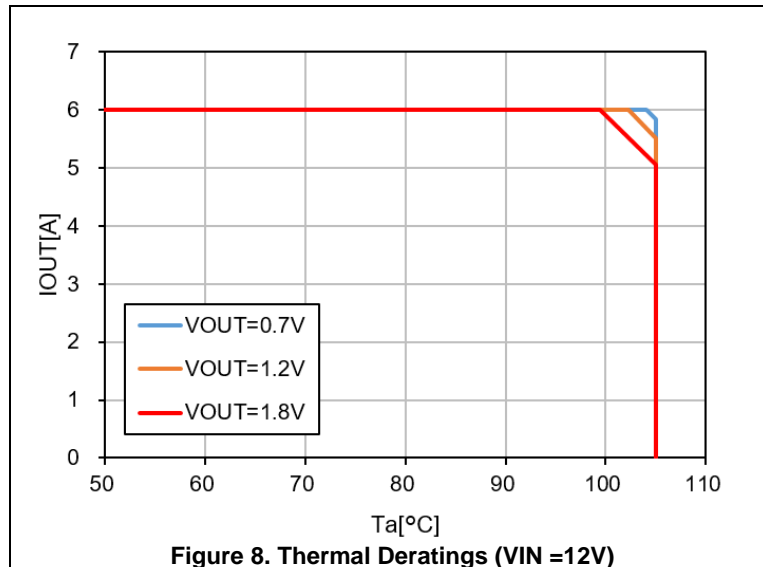


Figure 7. Power Dissipation vs. Load Current and Output Voltage

Thermal Deratings (Reference Data)

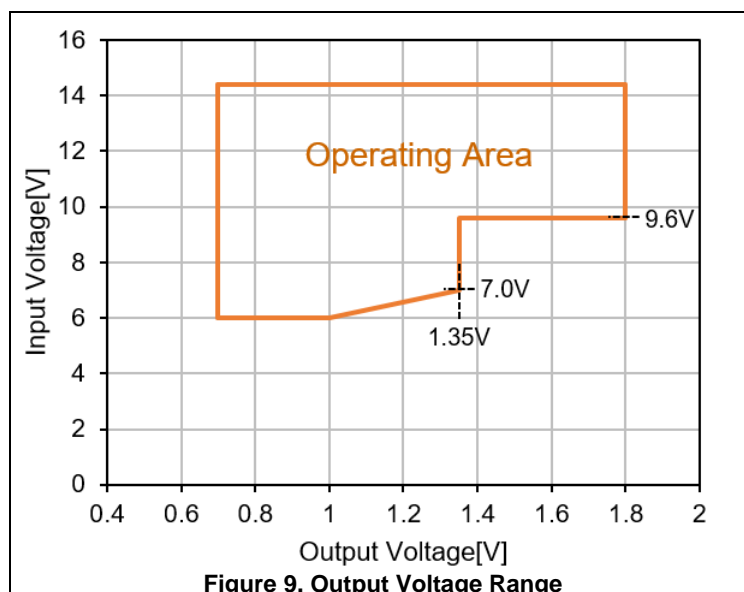


Thermal deratings are evaluated in following condition.

- The product is mounted on 114.5 x 101.5 x 1.6mm (Layer1, 4: 2oz Layer2, 3: 1oz copper) FR-4 board.
- No forced air flow.

Surface temperature of the product: 118.7°C max.

Output Voltage Range



Limitation of Input Voltage Slew rate

When starting the module with ramping Input Voltage up, the slew rate of the ramping should be managed for the proper operation. If Input Voltage ramping up is too steep, it would cause charge injection to the internal nodes via parasitic. The maximum slew rate of the Input Voltage ramp up when booting the module with Input Voltage is specified on the table 4 "Electronic Characteristics".

Similarly, if the VIN slew rate is too low compare with VOUT slew rate, it could prevent expected start up behavior. To avoid hitting the maximum duty cycle operation, the VIN slew rate should satisfy either equation of (eq1) – (eq.6) in the follow table that determined by SS setting. VINSR_L is minimum of input voltage startup slew rate and SS is soft start.

As a reference, estimated value of the slew rate and start-up time for each output voltage is written in the table.

| SS (V/ms) | VINSR EQUATION | CALCULATION EXAMPLE | | | | | |
|--------------|--|---------------------|----------|---------|--------------------------------|----------|---------|
| | | VINSR_L (V/ms) | | | VIN RISE TIME (0V to 12V) (ms) | | |
| | | 1.0VOUT | 1.35VOUT | 1.8VOUT | 1.0VOUT | 1.35VOUT | 1.8VOUT |
| 1.867 | $VINSR \geq 11/15 \times VOUT - 0.41$ (eq.1) | 0.32 | 0.58 | 0.91 | 37.5 | 20.7 | 13.2 |
| 0.934 | $VINSR \geq 22/45 \times VOUT - 0.24$ (eq.2) | 0.25 | 0.42 | 0.64 | 48 | 28.6 | 18.8 |
| 0.467 | $VINSR \geq 11/45 \times VOUT - 0.04$ (eq.3) | 0.2 | 0.29 | 0.4 | 60 | 41.4 | 30 |
| 0.233 | $VINSR \geq 7/45 \times VOUT - 0.04$ (eq.4) | 0.12 | 0.17 | 0.24 | 100 | 70.6 | 50 |
| 0.117 | $VINSR \geq 1/15 \times VOUT + 0.01$ (eq.5) | 0.08 | 0.1 | 0.13 | 150 | 120 | 92.3 |
| 0.058 | $VINSR \geq 2/45 \times VOUT - 0.01$ (eq.6) | 0.03 | 0.02 | 0.07 | 400 | 240 | 171.4 |
| 0.029 | No minimum limitation | - | | | - | | |
| 0.014 | No minimum limitation | - | | | - | | |

Table.6 Minimum input voltage start-up slew rate and start-up time

Detailed Description

The MYTNC1R86RELA2RA is a two-stage DCDC converter that is composed of a dual-phase charge pump-based DCDC converter and a dual-phase synchronous buck DCDC converter. The output voltage range supported from 0.7 to 1.8V (The output voltage range depend on the input voltage.) with load currents of up to 6A and up to 10.8W delivered to the external load. This module isn't designed for the parallel operation.

Output Voltage Remote Sense Function

The MYTNC1R86RELA2RA has a sense pin, +Sense, for this function. The function is capable of compensating for the voltage drop in the wiring by connecting the sense pin to the load point. The upper limit of the compensating by sense function depends on the maximum voltage allowed to the Vout pin (within range of the Output Voltage Accuracy). The sense trace should be as short as possible and shielded by the GND line or something else to reduce noise susceptibility.

The recommended sense line length is within 10cm for output voltage stability. Do NOT connect sense pin to the output of the additional LC filter that sits between the Vout pin and +Sense pin. If the remote sense is not needed, the +Sense pin should be shorted to the Vout pin.

Remote Enable Function

The MYTNC1R86RELA2RA has an enable input pin, ON/OFF, which is designed to be compatible with typical low voltage digital I/O levels so that it can be easily driven by an external controller. The ON/OFF pin logic is high active and connected to the VIN through internal resistors. So if external power sequencing or control is not required, the ON/OFF pin can be left open.

Soft start Function

The MYTNC1R86RELA2RA has a soft start function. This function suppresses the inrush current and the output voltage overshoot. When the function is operating, the converter is controlled in discontinuous current mode (DCM), so the output ripple voltage may be larger than steady-state behavior which is in continuous current mode (CCM). If the input voltage drops and the operating condition deviates from the supported operation range of fig.9 “Output Voltage Range”, you should discharge the input voltage below the VIUVL and then restart. This soft start function is also compatible with pre-bias start-up. However the converter cannot prevent reverse current except during soft start, so the output must NOT be connected to a circuit that has a voltage higher than the output voltage setting.

Power Good Operation

MYTNC1R86RELA2RA has an open-drain “power good” pin, POK. The POK pin must be pulled up externally, though a resistor to a voltage of $\leq 5.5V$. MYTNC1R86RELA2RA will hold the POK pin low during soft start, the VOUT is outside of the regulation or when the fault condition is detected and being handled. Please note that the power good function will not work when the module is inactive. Therefore, the POK pin will be high impedance when the VIN is below the VIUVH or the module disabled.

The power good function is activated after soft start has finished. If the VOUT becomes within +5% to –5% of the target value, internal comparators detect the power good state and the power good signal becomes high. After that, if the VOUT rises or falls to outside of +10% or –10% of the target value, the power good signal becomes low.

The power good function is a flag that indicates the output voltage status and internal protection status. If the POK pin isn't high for a long time from startup, there are some abnormal situation occur in inside the module or external environment.

So, we recommend monitoring the POK pin, and reset the module and the output load in abnormal.

Telemetry System

An ADC-based telemetry system is provided to monitor health of the MYTNC1R86RELA2RA and report status through the I²C interface for fault management and diagnostics. The following signals can be reported using the telemetry circuits: input voltage, output voltage, output current, and MYTNC1R86RELA2RA temperature. Typical parameters for temperature measurement function are as follows:

Resolution: 0.5°C
Accuracy: $\pm 3^\circ\text{C}$
Measurement time: 4ms

The telemetry register functionality is as follows:

- ADC presents a new value, which is latched internally and overwritten as new values come in.
- The read-only registers are updated with the latched values only when the upper byte is read.
- Reading a lower byte does not update the upper-lower byte combo value.
- Reading once returns the previous value; reading again returns the current value.

See the Electrical Characteristics table for additional information regarding telemetry.

The telemetry measurement temperature isn't the module surface temperature. The telemetry temperature is the measured value of the inside the module. So the telemetry temperature includes some error from the surface temperature.

Programming

MYTNC1R86RELA2RA can be programmed through the I²C serial bus interface to configure certain system parameters. Those programmable parameters are output voltage and soft start time.

See the section of "Register Map" and "Detailed Register Description" for program to register.

I²C Interface Bus Overview

The I²C bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. An I²C slave device receives and/or transmits data on the bus under control of the master device.

MYTNC1R86RELA2RA operates as an I²C slave and supports the following data transfer modes, as defined in the I²C-Bus specification: Standard mode (100 Kbps) and fast mode (400 Kbps), and fast mode plus (1 Mbps). The interface adds flexibility to the power supply solution, enabling some functions to be programmed to new values depending on application requirements. Register contents remain intact as long as the VDD bias supply voltage remains above the under-voltage lockout threshold.

The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. MYTNC1R86RELA2RA supports 7-bit addressing; 10-bit addressing and general call address are not supported. The module 7-bit address is defined as '0x30'.

Standard-, Fast-, Fast-Mode Plus Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 10. All I²C-compatible devices should recognize a start condition.

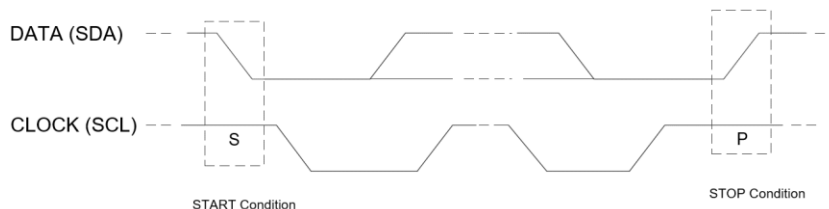


Figure 10. START and STOP Conditions

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 11). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the I²C slave device with a matching address generates an Acknowledge (see Figure 12) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with an I²C slave has been established.

The master generates further SCL cycles to either transmit data to the I²C slave (R/W bit 1) or receive data from the I²C slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by transmitter. So an acknowledge signal can either be generated by the master or by the I²C slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 10). This releases the bus and stops the communication link with the addressed I²C slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address. Attempts to read data from register addresses not listed in this section will result in 0xFF being read out.

I²C Update Sequence

MYTNC1R86RELA2RA requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, MYTNC1R86RELA2RA device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MYTNC1R86RELA2RA, which performs an update on the falling edge of the acknowledge signal that follows the LSB.

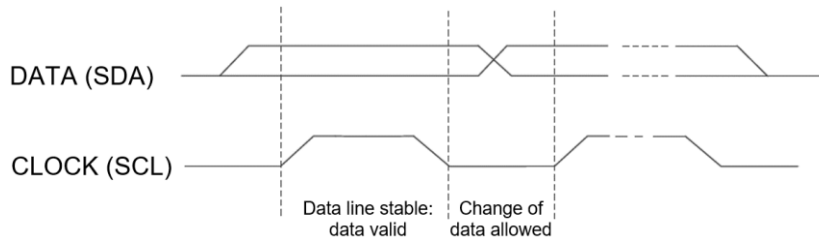


Figure 11. Bit Transfer on the Serial Interface

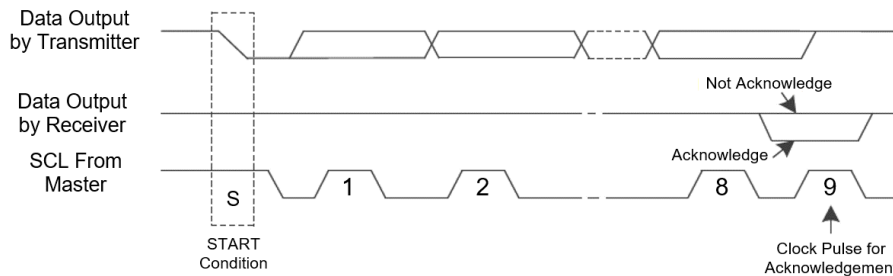


Figure 12. Acknowledge on the I²C Bus

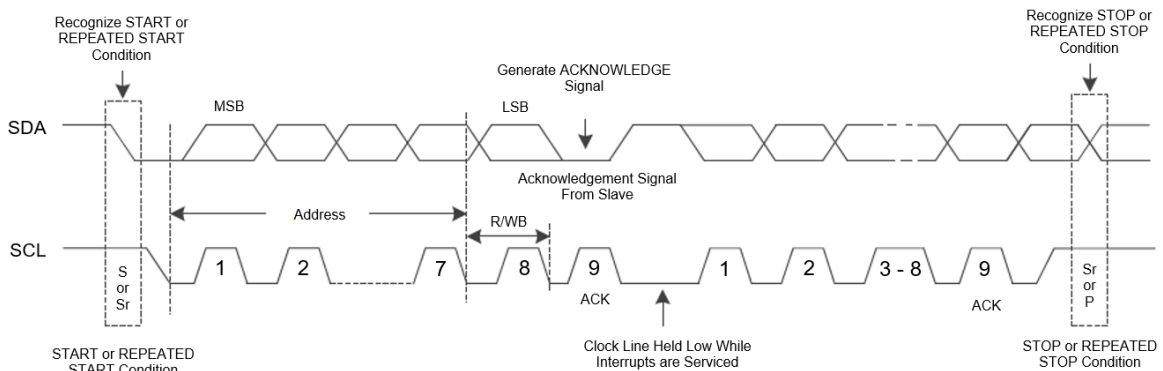


Figure 13. Bus Protocol

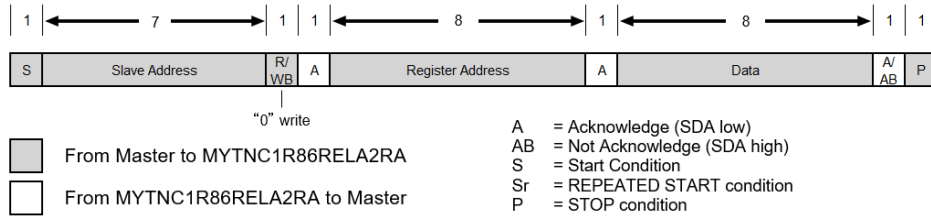


Figure 14. "Write" Data Transfer Format in Standard-, Fast, Fast-Plus Modes

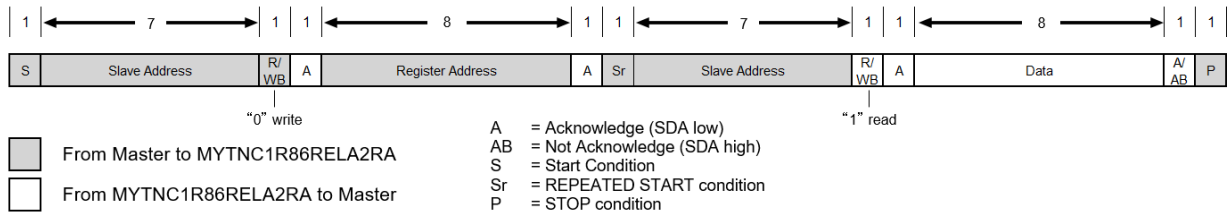


Figure 15. "Read" Data Transfer Format in Standard-, Fast, Fast-Plus Modes

Register Map

 I²C Slave Address: 0110000 (0x30) ⁽¹⁾

Register Configuration Parameters

| NAME | ADD (HEX) | POR Value | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
|--------------|-----------|-----------|-------------------------|----|----|----|-------------------------|--------------|-------------------------|-----------|--|
| VSET1 | 0x00 | 0x46 | VSET | | | | | | | | |
| RESERVED | 0x01 | 0x00 | Reserved | | | | | | | | |
| DCR | 0x02 | 0x00 | DCR | | | | Reserved ⁽²⁾ | | | | |
| CONFIG1 | 0x03 | 0x04 | Reserved ⁽²⁾ | | | | | SS | | | |
| RESERVED | 0x04 | 0x00 | Reserved ⁽²⁾ | | | | | | | | |
| RESERVED | 0x05 | 0x8A | Reserved ⁽²⁾ | | | | | | | | |
| RESERVED | 0x06 | 0x82 | Reserved ⁽²⁾ | | | | | | | | |
| RESERVED | 0x07 | 0x10 | Reserved ⁽²⁾ | | | | | | | | |
| RESERVED | 0x08 | 0x00 | Reserved ⁽²⁾ | | | | | | | | |
| RESERVED | 0x09 | 0x9F | Reserved ⁽²⁾ | | | | | | | | |
| RESERVED | 0x0A | 0x78 | Reserved ⁽²⁾ | | | | | | | | |
| RESERVED | 0x0B | 0x78 | Reserved ⁽²⁾ | | | | | | | | |
| RESERVED | 0x0C | 0x61 | Reserved ⁽²⁾ | | | | | | | | |
| VOUT1_LSB | 0x42 | 0x00 | VOUT1 | | | | Reserved | | | | |
| VOUT1_MSB | 0x43 | 0x00 | VOUT1 | | | | | | | | |
| VIN | 0x46 | 0x00 | VIN | | | | | | | | |
| RESERVED | 0x47 | 0x00 | Reserved | | | | | | | | |
| IOUTF1 | 0x48 | 0x00 | IOUTF1 | | | | | | | | |
| IOUTP1_LSB | 0x4A | 0x00 | IOUTP1 | | | | Reserved | | | | |
| IOUTP1_MSB | 0x4B | 0x00 | IOUTP1 | | | | | | | | |
| TEMP_LSB | 0x4E | 0x00 | TEMP | | | | Reserved | | | | |
| TEMP_MSB | 0x4F | 0x00 | TEMP | | | | | | | | |
| MASTERFAULTS | 0x54 | 0x00 | Reserved | | | | | VOUT_SHORT | VOUT_OCP | OVER TEMP | |
| RESERVED | 0x55 | 0x00 | Reserved | | | | | | | | |
| RESERVED | 0x57 | 0x00 | Reserved ⁽²⁾ | | | | | | | | |
| RESERVED | 0x58 | 0x00 | Reserved ⁽²⁾ | | | | | | | | |
| RESERVED | 0x5A | 0x00 | Reserved | | | | | | | | |
| RESERVED | 0x5B | 0x00 | Reserved ⁽²⁾ | | | | | | | | |
| RESERVED | 0x5C | 0x00 | Reserved ⁽²⁾ | | | | | | | | |
| RESERVED | 0x5D | 0x00 | Reserved ⁽²⁾ | | | | | | | | |
| MTPWRITE | 0x60 | 0x01 | MTP_WRITE_CMD | | | | | MTPWRI TEDNE | Reserved ⁽²⁾ | | |
| MTPUNLOCK | 0x61 | 0x00 | MTPUNLOCK_CMD | | | | | | | | |

Note :

- (1) Excluding read/write bit. 01100000 (0x60) if including read/write bit.
- (2) Do not change these reserved bits. We guarantee operation of the module only when these reserved bit is the initial value.

Table 7. Register map

Detailed Register Description

Register VSET1

| NAME | ADDRESS | POR Value |
|-------|---------|-----------|
| VSET1 | 0x00 | 0x46 |

Bit Assignment

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---|---|---|---|---|---|---|
| VSET1[7:0] | | | | | | | |

Bit Description

| Field name | Bits | Type | POR | Description |
|------------|-------|------|----------|---|
| VSET1[7:0] | [7:0] | R/W | 01000110 | $V_{OUT1} = 2.55/255 \times \text{bin2dec}(VSET1<7:0>)$ Program VOUT1 Output Voltage in 10mV steps: Do not exceed the specified limits of the output voltage range restricted by input voltage or the converter's maximum power rating when applying this register. 00h: 0mV 01h: 10mV 02h: 20mV 77h: 1.19V 78h: 1.2V 79h: 1.21V |

Register DCR

| NAME | ADDRESS | POR Value |
|------|---------|-----------|
| DCR | 0x02 | 0x00 |

Bit Assignment

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|---|---|----------|---|---|---|
| DCR [3:0] | | | | Reserved | | | |

Bit Description

| Field name | Bits | Type | POR | Description |
|------------|-------|------|------|---|
| DCR[3:0] | [7:4] | R/W | 0000 | DCR value for calculation of IOUT. The DCR value is written in test Production. 0000: 14.6 mΩ 0001: 15.4 mΩ 0010: 16.2 mΩ 0011: 17.0 mΩ 0100: 17.8 mΩ 0101: 18.6 mΩ 0110: 19.4 mΩ 0111: 20.2 mΩ 1000: 21.0 mΩ 1001: 21.8 mΩ 1010: 22.6 mΩ 1011: 23.4 mΩ 1100: 24.2 mΩ 1101: 25.0 mΩ 1110: 25.8 mΩ 1111: 26.6 mΩ |

Register CONFIG1

| NAME | ADDRESS | POR Value |
|---------|---------|-----------|
| CONFIG1 | 0x03 | 0x04 |

Bit Assignment

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|---------|---|---|
| Reserved | | | | | SS[2:0] | | |

Bit Description

| Field name | Bits | Type | POR | Description |
|------------|-------|------|-----|--|
| SS[2:0] | [2:0] | R/W | 100 | Program Soft start and VOUT Slew Rate: 000: 1.867mV/ms 100: 0.117mV/ms 001: 0.934mV/ms 101: 0.058mV/ms 010: 0.467mV/ms 110: 0.029mV/ms 011: 0.233mV/ms 111: 0.014mV/ms |

Register VOUT1_LSB

| NAME | ADDRESS | POR Value |
|-----------|---------|-----------|
| VOUT1_LSB | 0x42 | 0x00 |

Bit Assignment

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---|---|---|----------|---|---|---|
| VOUT1[3:0] | | | | Reserved | | | |

Bit Description

| Field name | Bits | Type | POR | Description |
|------------|-------|------|------|---|
| VOUT1[3:0] | [7:4] | R | 0000 | Lower 4 bit of the 12-bit VOUT1 ADC result. VOUT can be calculated as: $2.55V \times \text{bin2dec}(\text{VOUT1}[11:0]) / 4095$ All 12-bit must be read to refresh the next ADC reading. |

Register VOUT1_MSB

| NAME | ADDRESS | POR Value |
|-----------|---------|-----------|
| VOUT1_MSB | 0x43 | 0x00 |

Bit Assignment

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|---|
| VOUT1[11:4] | | | | | | | |

Bit Description

| Field name | Bits | Type | POR | Description |
|-------------|-------|------|-----------|---|
| VOUT1[11:4] | [7:0] | R | 0000 0000 | Upper 8 bit of the 12-bit VOUT1 ADC result. VOUT can be calculated as: $2.55V \times \text{bin2dec}(\text{VOUT1}[11:0]) / 4095$ All 12-bit must be read to refresh the next ADC reading. |

Register VIN

| NAME | ADDRESS | POR Value |
|------|---------|-----------|
| VIN | 0x46 | 0x00 |

Bit Assignment

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|---|---|---|
| VIN[7:0] | | | | | | | |

Bit Description

| Field name | Bits | Type | POR | Description |
|------------|-------|------|-----------|---|
| VIN[7:0] | [7:0] | R | 0000 0000 | 8-bit VIN ADC result. VIN can be calculated as: $20.4V \times \text{bin2dec}(\text{VIN}[7:0]) / 255$ |

Register IOUT1F

| NAME | ADDRESS | POR Value |
|--------|---------|-----------|
| IOUT1F | 0x48 | 0x00 |

Bit Assignment

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|---|
| IOUT1F[7:0] | | | | | | | |

Bit Description

| Field name | Bits | Type | POR | Description |
|-------------|-------|------|-----------|---|
| IOUT1F[7:0] | [7:0] | R | 0000 0000 | IOUT1 Fast Conversion ADC result, update every 32us. IOUT1 ISNS voltage can be calculated as: $V_ISNS1 = 100mV \times \text{bin2dec}(IOUT1F[7:0]) / 255$ IOUT can be calculated as: $IOUT = V_ISNS1 / (DCR[3:0] / 2)$ |

Register IOUT1P_LSB

| NAME | ADDRESS | POR Value |
|------------|---------|-----------|
| IOUT1P_LSB | 0x4A | 0x00 |

Bit Assignment

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|----------|---|---|---|
| IOUT1P[3:0] | | | | Reserved | | | |

Bit Description

| Field name | Bits | Type | POR | Description |
|-------------|-------|------|------|---|
| IOUT1P[3:0] | [7:4] | R | 0000 | Lower 4 bit of the IOUT1 Precision 12-bit ADC result, update every 128us. IOUT1 ISNS voltage can be calculated as: $V_ISNS1 = 100mV \times \text{bin2dec}(IOUT1P[11:0]) / 4095$ IOUT can be calculated as: $IOUT = V_ISNS1 / (DCR[3:0] / 2)$ All 12-bit must be read to refresh the next ADC reading. |

Register IOUT1P_MSB

| NAME | ADDRESS | POR Value |
|------------|---------|-----------|
| IOUT1P_MSB | 0x4B | 0x00 |

Bit Assignment

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|---|---|---|---|---|---|---|
| IOUT1P[11:4] | | | | | | | |

Bit Description

| Field name | Bits | Type | POR | Description |
|--------------|-------|------|-----------|--|
| IOUT1P[11:4] | [7:0] | R | 0000 0000 | Upper 8 bit of the IOUT1 Precision 12-bit ADC result, update every 128us. IOUT1 ISNS voltage can be calculated as: $V_ISNS1 = 100mV \times \text{bin2dec}(IOUT1P[11:0]) / 4095$ IOUT can be calculated as: $IOUT = V_ISNS1 / (DCR[3:0] / 2)$ All 12-bit must be read to refresh the next ADC reading |

Register TEMP_LSB

| NAME | ADDRESS | POR Value |
|----------|---------|-----------|
| TEMP_LSB | 0x4E | 0x00 |

Bit Assignment

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|---|---|----------|---|---|---|
| TEMP[3:0] | | | | Reserved | | | |

Bit Description

| Field name | Bits | Type | POR | Description |
|------------|-------|------|------|--|
| TEMP[3:0] | [7:4] | R | 0000 | Lower 4 bits of the 12-bit IC Temperature ADC result. IC temperature can be calculated as: TEMP (in Kelvin) = $512 \times \text{bin2dec}(\text{TEMP}[11:0]) / 4095$ All 12-bit must be read to refresh the next ADC reading. |

Register TEMP_MSB

| NAME | ADDRESS | POR Value |
|----------|---------|-----------|
| TEMP_MSB | 0x4F | 0x00 |

Bit Assignment

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---|---|---|---|---|---|---|
| TEMP[11:4] | | | | | | | |

Bit Description

| Field name | Bits | Type | POR | Description |
|------------|-------|------|------|--|
| TEMP[11:4] | [7:4] | R | 0000 | Upper 8 bits of the 12-bit IC Temperature ADC result. IC temperature can be calculated as: TEMP (in Kelvin) = $512 \times \text{bin2dec}(\text{TEMP}[11:0]) / 4095$ All 12-bit must be read to refresh the next ADC reading. |

Register MASTERFAULTS

| NAME | ADDRESS | POR Value |
|--------------|---------|-----------|
| MASTERFAULTS | 0x54 | 0x00 |

Bit Assignment

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|------------|----------|----------|
| Reserved | | | | | VOUT_SHORT | VOUT_OCP | OVERTEMP |

Bit Description

| Field name | Bits | Type | POR | Description |
|------------|------|------|-----|--|
| VOUT_SHORT | [2] | R | 0 | VOUT(s) Shorted Fault: 0: No Fault 1: Fault |
| VOUT_OCP | [1] | R | 0 | VOUT(s) Over current Fault: 0: No Fault 1: Fault |
| OVERTEMP | [0] | R | 0 | IC(s) Over temperature Fault: 0: No Fault 1: Fault |

Register MTPWRITE

| NAME | ADDRESS | POR Value |
|----------|---------|-----------|
| MTPWRITE | 0x60 | 0x01 |

Bit Assignment

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------------|---|---|---|---|--------------|----------|---|
| MTPWRITE_CMD[4:0] | | | | | MTPWRITE_DNE | Reserved | |

Bit Description

| Field name | Bits | Type | POR | Description |
|--------------------|-------|------|--------|--|
| MTPWRITE_CMD [4:0] | [7:3] | R/W | 0000 0 | Setting MTPWRITE_CMD to 10010 initiates a programming cycle to burn the contents of customer registers 0x00 to 0x0B into MTP memory, which sets the POR values of the registers upon the next start-up. Since the lower three bits of this register are read-only, it is recommended to just write 0's to them (0x90 for all eight bits). Before taking this step, the user must unlock the MTP user area using register 0x61. |
| MTPWRITE_DNE | [1] | R | 0 | MTP Write Cycle Status : 0: MTP Write Command in Process. When an MTPWRITE_CMD is issued, this bit clears itself, and stays low until the MTP Write cycle completes. 1: MTP Write Cycle Complete |

Register MTPUNLOCK

| NAME | ADDRESS | POR Value |
|-----------|---------|-----------|
| MTPUNLOCK | 0x61 | 0x00 |

Bit Assignment

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|---|---|---|---|---|---|---|
| MTPUNLOCK_CMD[7:0] | | | | | | | |

Bit Description

| Field name | Bits | Type | POR | Description |
|--------------------|-------|------|-----------|---|
| MTPUNLOCK_CMD[7:0] | [7:0] | R/W | 0000 0000 | Before initiating an MTP programming cycle using register 0x60, the user needs to write the value 0x61 into this register to unlock the MTP user space. |

Protections

MYTNC1R86RELA2RA provides extensive and robust protection against input and output faults and over-temperature conditions, as summarized in the following table.

| FAULT MODE | PROTECTION | FAULT RESPONSE | FAULT DETECTION TIME |
|-------------------|-----------------------------|---------------------------------------|-------------------------|
| VIN Under-Voltage | Under voltage Lock out | Power-on reset | Immediate (VIN falling) |
| Over Load | Over current protection | POK de-asserted; Enter hiccup mode | 1ms |
| Output Short | Short circuit protection | POK de-asserted; Enter hiccup mode | Immediate |
| Over Temperature | Over temperature protection | POK de-asserted; Enter hiccup mode | 160µs |

Table 8. Fault Protection Detection Time and Responses

The protection does not guarantee the module operation within the recommended operating conditions. Even if the protection is operating, it may exceed the conditions, and thus may reduce the reliability of the module.

Over Current Protection and Short Circuit Protection

MYTNC1R86RELA2RA provides output over current protection and short circuit protection for load fault. When the converter load current exceeds the over current threshold for the detection time, the converter output is shut down. Following the shutdown, the converter periodically tries to recover by the startup sequence. This mode is called "hiccup" mode and continues until the load current decreases to under the over current threshold. When hiccup mode releases, the converter returns to normal operation.

Short circuit protection is incorporated for times when more rapidly shutdown is needed as output short. When the converter load current exceeds the short circuit threshold, the converter shuts down immediately and operates in hiccup mode until the load current decreases to under the short circuit threshold. When the hiccup mode releases, the converter returns to normal operation.

Over Temperature Protection

MYTNC1R86RELA2RA includes an integrated temperature sensor to protect the system from overheating. Once the converter detects over temperature longer than 160µsec, the output is turned off to reduce the power dissipation of the module. When the temperature drops below the hysteresis limit, the output is turned on again. If the underlying cause of the over-temperature fault is not cleared, the system enters into hiccup mode until the fault condition is removed.

Soldering Guidelines

Murata recommends the specifications below when installing this converter. These specifications vary depending on the solder type. Exceeding these specifications may cause damage to the product. Your production environment may differ, therefore, thoroughly review these guidelines with your process engineers.

| REFLOW SOLDER OPERATIONS FOR SURFACE MOUNT PRODUCTS | |
|---|--------------------------|
| For Sn/Ag/Cu based solders: | |
| Preheat Temperature | Less than 1°C per second |
| Time over Liquidus | 45 to 75 seconds |
| Maximum Peak Temperature | 260°C |
| Cooling Rate | Less than 3°C per second |
| For Sn/Pb based solder: | |
| Preheat Temperature | Less than 1°C per second |
| Time over Liquidus | 60 to 75 seconds |
| Maximum Peak Temperature | 235°C |
| Cooling Rate | Less than 3°C per second |

Table 9. Reflow Guidelines for Sn/Ag/Cu solders and Sn/Pb solders

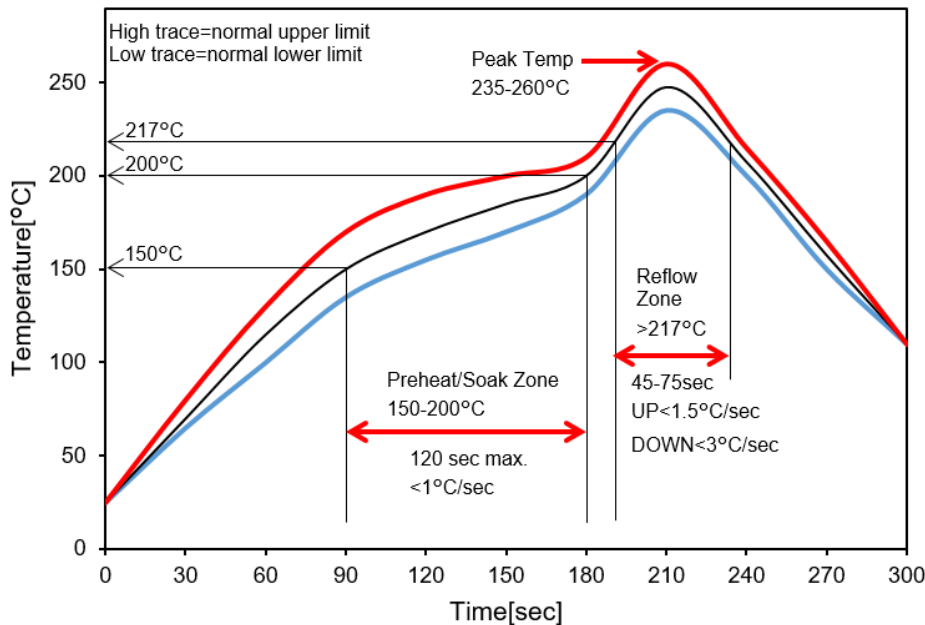


Figure 16. Reflow Profile for Sn/Ag/Cu Solder

Pb-free Solder Processes

For Pb-free solder processes, the product is qualified for MSL 3 according to IPC/JEDEC standard J-STD-020C. During reflow, the module must not exceed 260°C at any time.

Dry Pack Information

Products intended for Pb-free reflow soldering processes are delivered in standard moisture barrier bags according to IPC/JEDEC standard J-STD-033.

(Handling, Packing, Shipping and Use of Moisture, Reflow, and Process Sensitivity Devices).

Using products in high temperature Pb-free soldering processes requires dry pack storage and handling. In case the products have been stored in an uncontrolled environment and no longer can be considered dry, the products must be baked according to J-STD-033.

Application Performance

The Application Performance data is reference and based on the Application Board in Figure 40.

Ta=25°C, No forced air flow, unless otherwise noted.

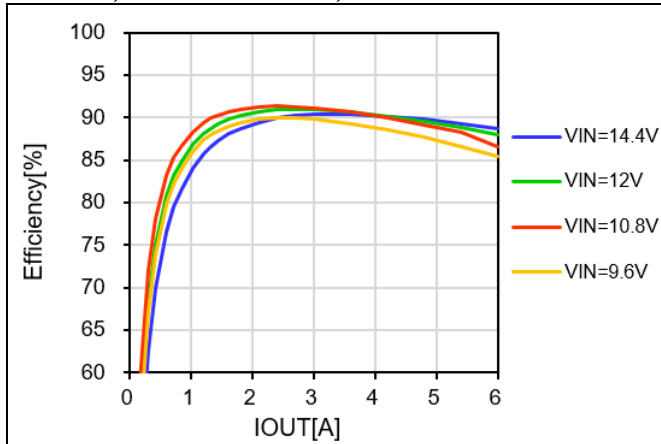


Figure 17. Efficiency vs. Load Current and Line Voltage @+25°C (VOUT=1.8V)

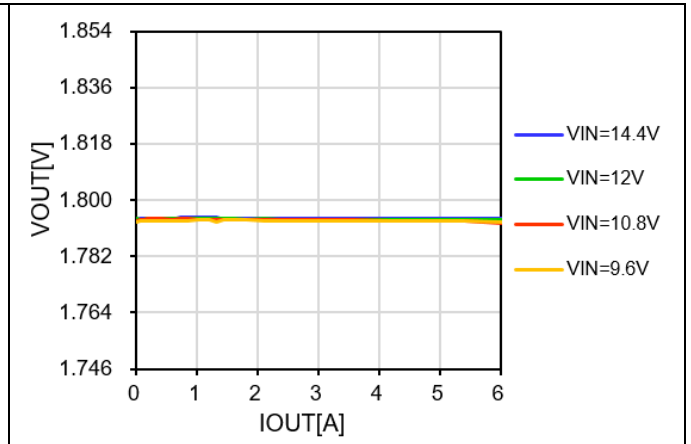


Figure 18. Vo vs. Load Current and Line Voltage @+25°C (VOUT=1.8V)

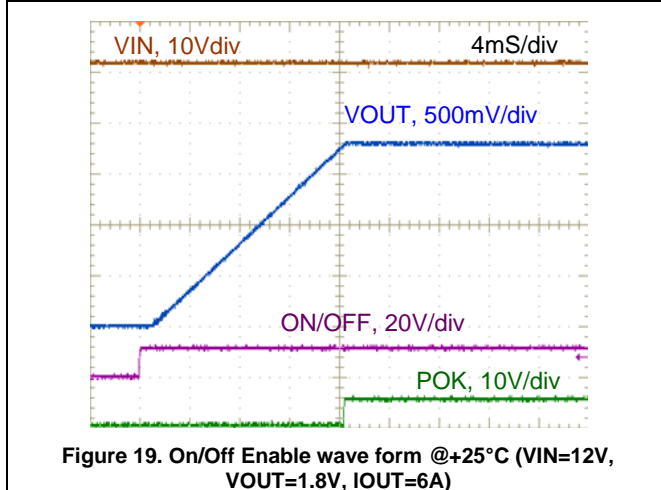


Figure 19. On/Off Enable wave form @+25°C (VIN=12V, VOUT=1.8V, IOUT=6A)

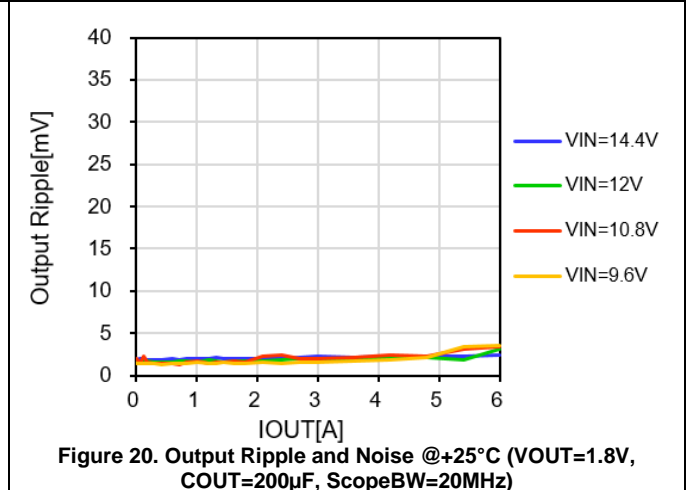


Figure 20. Output Ripple and Noise @+25°C (VOUT=1.8V, COUT=200µF, ScopeBW=20MHz)

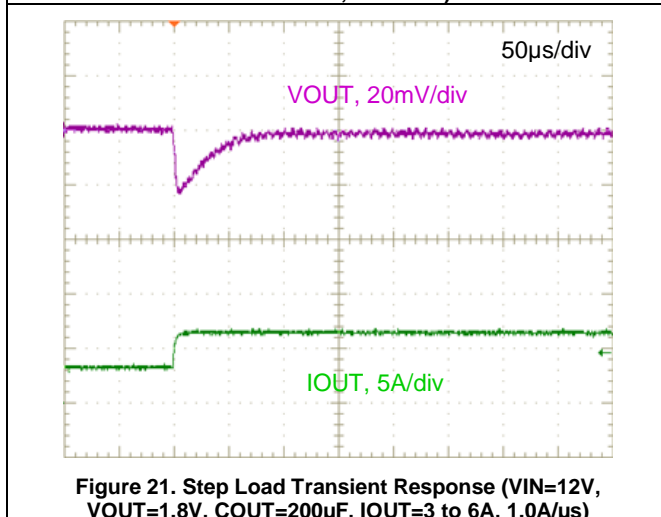


Figure 21. Step Load Transient Response (VIN=12V, VOUT=1.8V, COUT=200µF, IOUT=3 to 6A, 1.0A/µs)

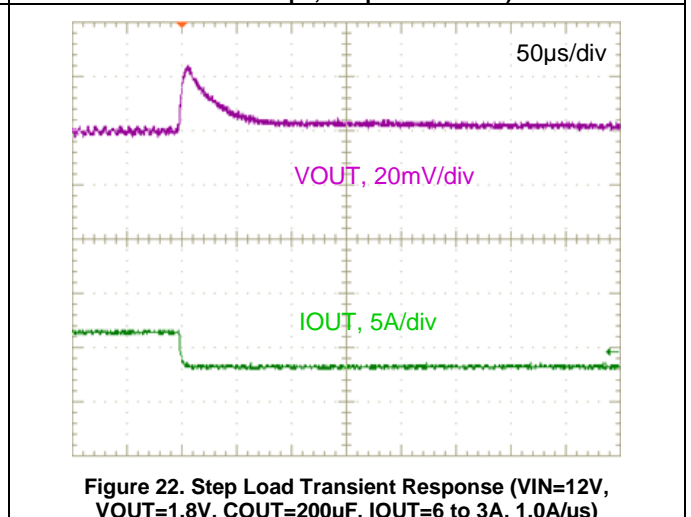


Figure 22. Step Load Transient Response (VIN=12V, VOUT=1.8V, COUT=200µF, IOUT=6 to 3A, 1.0A/µs)

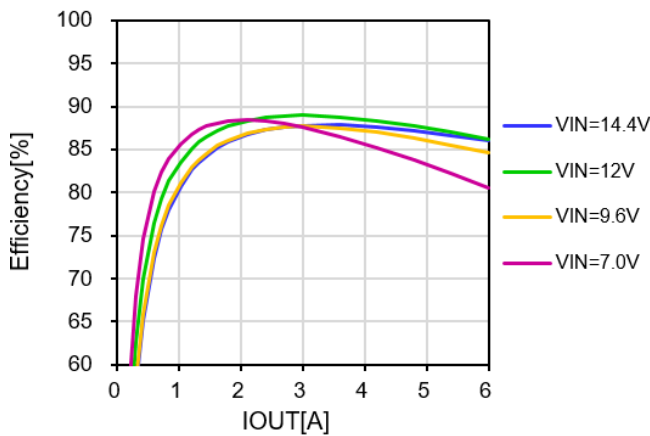


Figure 23. Efficiency vs. Load Current and Line Voltage @+25°C (VOUT=1.2V)

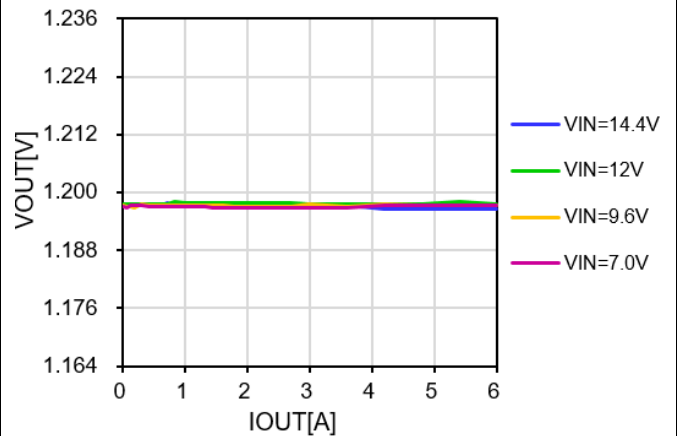


Figure 24. VOUT vs. Load Current and Line Voltage @+25°C (VOUT=1.2V)

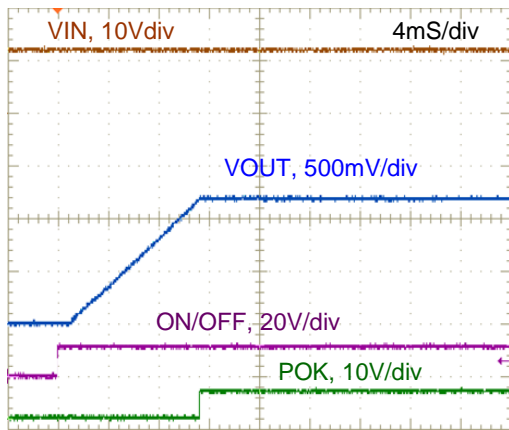


Figure 25. On/Off Enable wave form @ +25°C (VIN=12V, VOUT=1.2V, IOUT=6A)

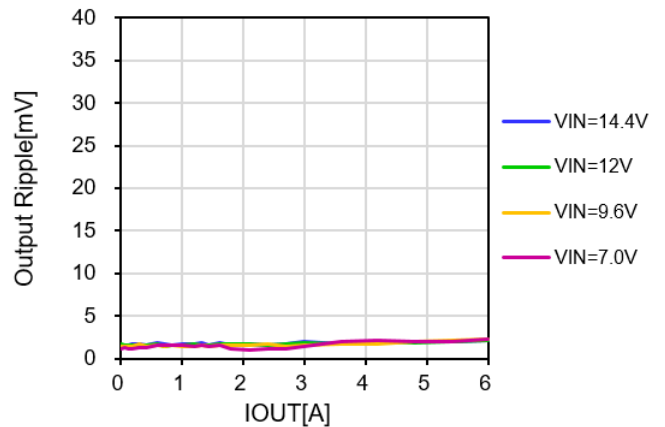


Figure 26. Output Ripple and Noise @ +25°C (VOUT=1.2V, COU=200μF, ScopeBW=20MHz)

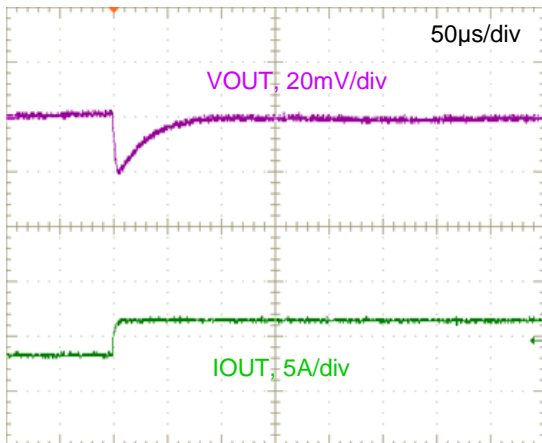


Figure 27. Step Load Transient Response (VIN=12V, VOUT=1.2V, COU=200μF, IOUT=3 to 6A, 1.0A/μs)

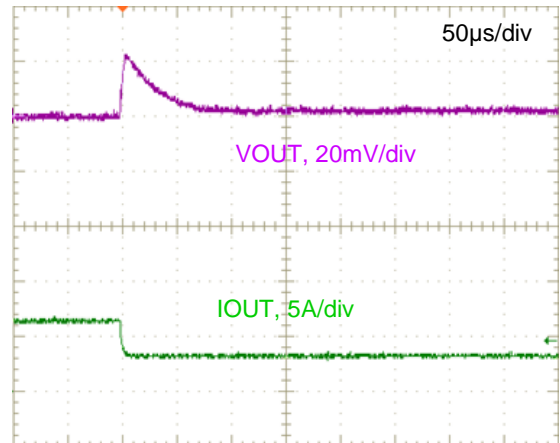


Figure 28. Step Load Transient Response (VIN=12V, VOUT=1.2V, COU=200μF, IOUT=6 to 3A, 1.0A/μs)

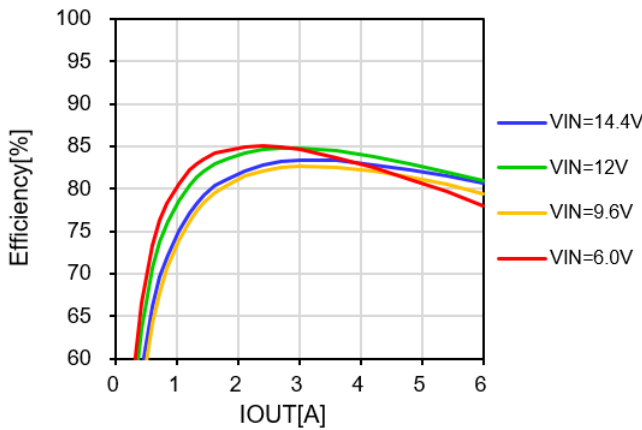


Figure 29. Efficiency vs. Load Current and Line Voltage @+25°C (VOUT=0.7V)

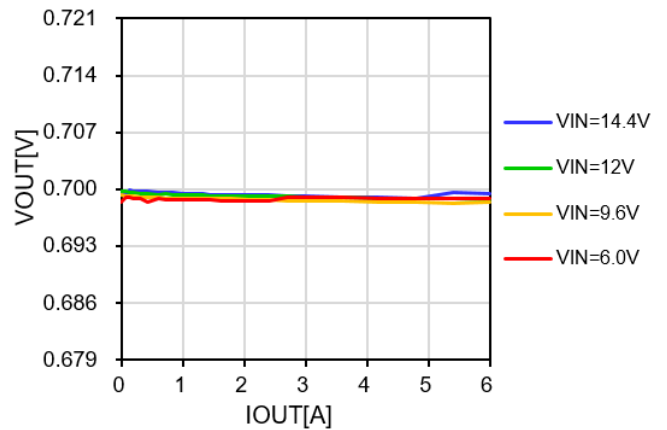


Figure 30. Vo vs. Load Current and Line Voltage @+25°C (VOUT= 0.7V)

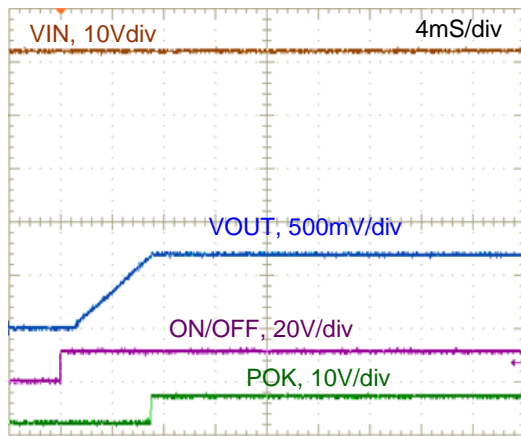


Figure 31. On/Off Enable wave form @+25°C (VIN=12V, VOUT=0.7V, IOUT=6A)

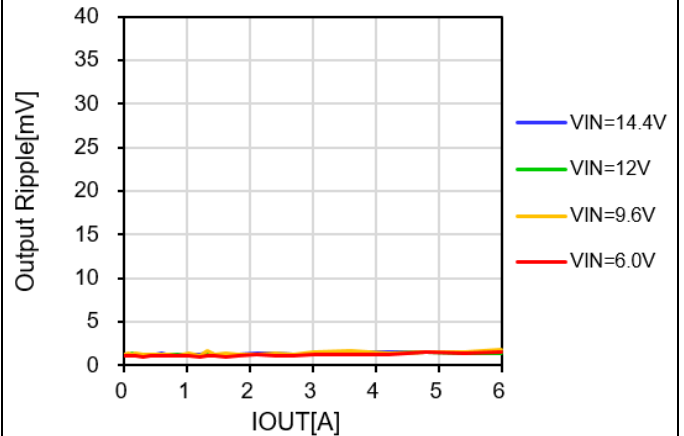


Figure 32. Output Ripple and Noise @+25°C (VOUT=0.7V, COUT=200μF, ScopeBW=20MHz)

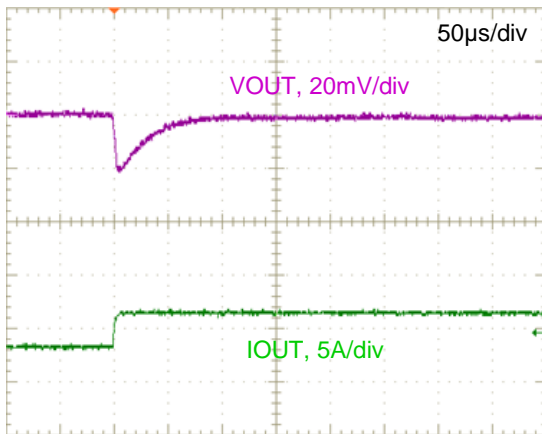


Figure 33. Step Load Transient Response (VIN=12V, VOUT=0.7V, COUT=200μF, IOUT=3 to 6A, 1.0A/μs)

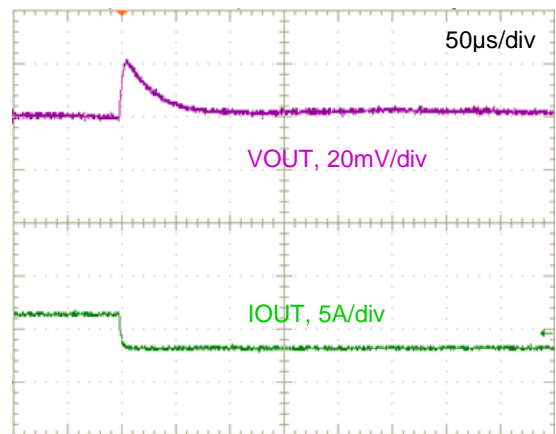


Figure 34. Step Load Transient Response (VIN=12V, VOUT=0.7V, COUT=200μF, IOUT=6 to 3A, 1.0A/μs)

Transient Performance

| VOUT [V] | VIN [V] | COUT [μF] | VOLTAGE DEVIATION [mV] |
|----------|---------|-----------|-------------------------|
| | | | 3A-6A LOAD STEP (1A/μs) |
| 1.8 | 12 | 200 | 23.2 |
| 1.2 | | | 22.4 |
| 0.7 | | | 21.2 |

Table 10. Transient Performance and Conditions

Test Circuit

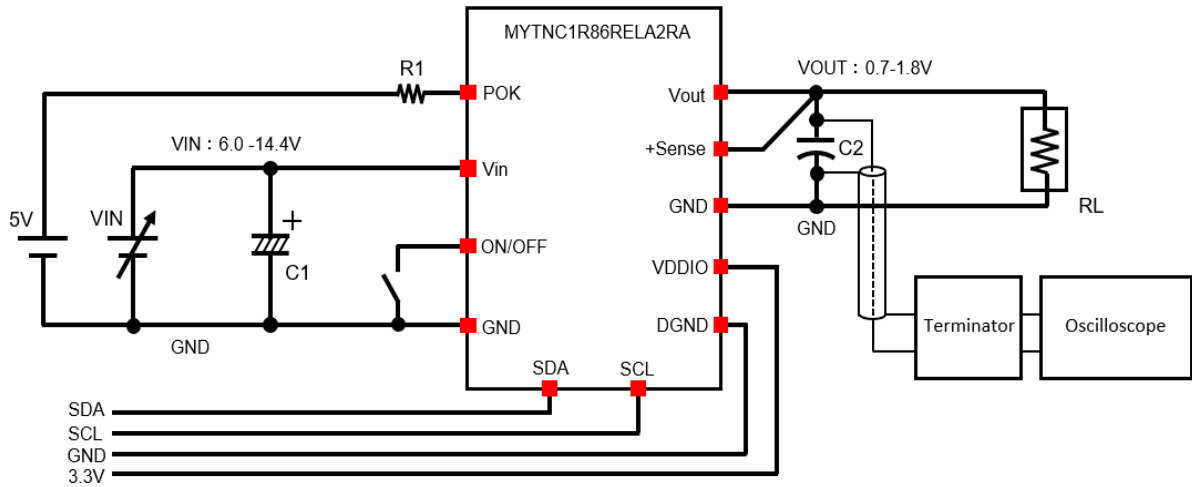


Figure 35. Test Circuit

| REFERENCE | VALUE | DESCRIPTION | PART AND EQUIPMENT |
|--------------|-------------|-------------------------------|-------------------------------|
| C1 | 1000μ | Electrolysis Capacitor | - |
| C2 | 100μ x 2pcs | CAP/CER/100uF/4V/X7U/1206/20% | GRM31CE70G107MEA8 (Murata) |
| R1 | 100k | 1/10W/5% | - |
| VIN | - | DC Power Supply | - |
| RL | - | Electronic Load Device | ELL-355(KeisokuGiken) |
| Oscilloscope | - | Digital Oscilloscope | DPO5034 or TDS5034(Tektronix) |
| Terminator | - | Terminator | TRC-50F2(KeisokuGiken) |

Table 11. Test Circuit Parts and Equipments List

Component Selection

Users of MYTNC1R86RELA2RA should adhere closely to the parts selected for the reference design bill of materials (BOM). Component selection is a complex process, and several parameters of importance to the design are not typically specified for passive components. Users wishing to deviate from these components are urged to contact Murata for guidance.

Input Fuse

Certain applications and/or safety agencies may require fuses at the inputs of power conversion components. Normally, the fuse should be inserted on the primary side input supply line. For greatest safety, we recommend a fast blow fuse installed in the ungrounded input supply line of this module too. The installer must observe all relevant safety standards and regulations.

For safety agency approvals, install the converter in compliance with the end-user safety standard.

Input Capacitor

In general input environment (there are sufficient consideration about parasitic impedance and stability.), MYTNC1R86RELA2RA does not need an external input capacitor. If you want to reduce the ripple on input more, you can add the external input capacitor. The input capacitor should be placed as close to the module as possible to reduce any parasitic inductance effects. The voltage rating of the capacitor needs to be as high as the absolute maximum voltage rating for the system. The capacitor has voltage coefficient of capacitance, so you should determine the rated value of capacitor that is taken into account the effective capacitance value at the applied VIN.

Output Capacitor

We recommend a low-ESR ceramic (Murata GRM31 series) capacitor for output. The ceramic type capacitor may be tried using either single or multiple capacitors in parallel.

The converter will achieve its rated output ripple and noise with additional external capacitor. The user may install more external output capacitance to reduce the ripple even further or for improved dynamic response.

These capacitors should be placed as closely as possible to the converter, and the output ripple measured under your load conditions. Use only as much capacitance as required to achieve your ripple and noise objectives. Excessive capacitance can make step load recovery sluggish or possibly introduce instability or start-up failure. Do not exceed the maximum rated output capacitance listed in the specifications. Please be careful the maximum capacitance depends on the soft start setting.

Packaging Information

This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the MYTNC1R86RELA2RA in the 10.5 x 9.0 x 2.1mm LGA package is MSL3.

Package Drawing

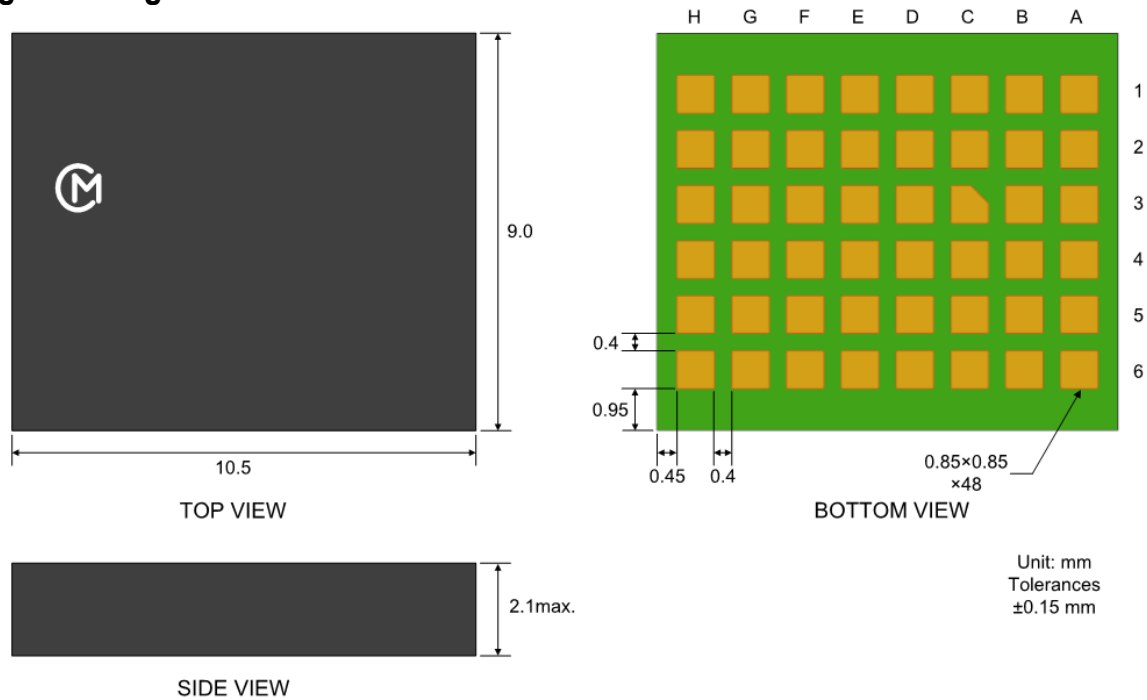


Figure 36. Package Outline Drawing

Recommended Board Land Pattern (Top View)

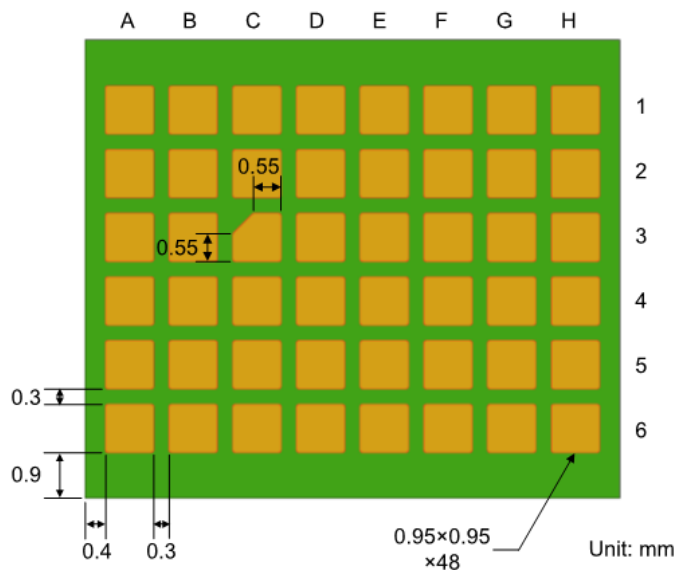
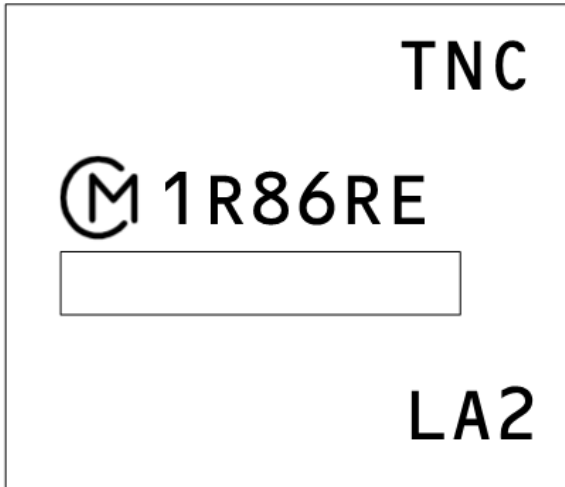


Figure 37. Recommended Board Land Pattern (Top View)

Top Marking Specification



| CODES | DESCRIPTION |
|--|--|
| Ⓜ | Pin 1 Marking |
| TNC1R86RELA2 | Product code (Please see product code table beside) |
| | Internal manufacturing code |

| PART NUMBER | PRODUCT CODE |
|------------------|--------------|
| MYTNC1R86RELA2RA | TNC1R86RELA2 |

Figure 38. Top Marking Specification

Application Circuit

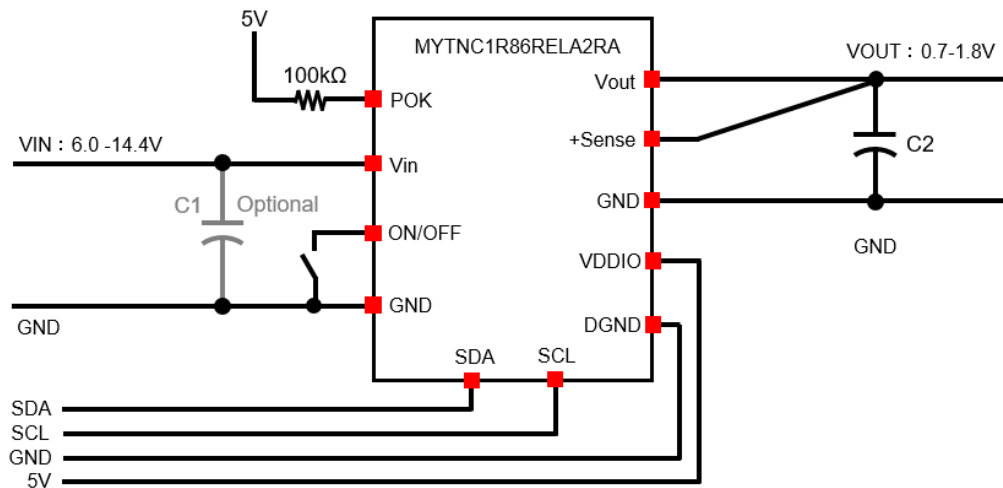


Figure 39. Application Schematic

Application Circuit Part List (Recommended)

| REFERENCE | VALUE | DESCRIPTION | PART NUMBER |
|-----------|-------------|--|----------------------------|
| C1 | 1000u | Electrolysis Capacitor (Optional) ⁽¹⁾ | - |
| C2 | 100u x 2pcs | CAP/CER/100μF/4V/X7U/1206/20% | GRM31CE70G107MEA8 (Murata) |

Table 12. Application Circuit Part List

(1) If there is a non-negligible parasitic impedance between the power supply and the converter, such as during evaluation, the optional input capacitor "C1" may be required to reduce the impedance. The recommended optional capacitor is an example. Please consider the optimum value for the case. This capacitor is usually an aluminum electrolytic type. It isn't necessary to place the capacitor near the input terminal of the converter.

Application Board Example

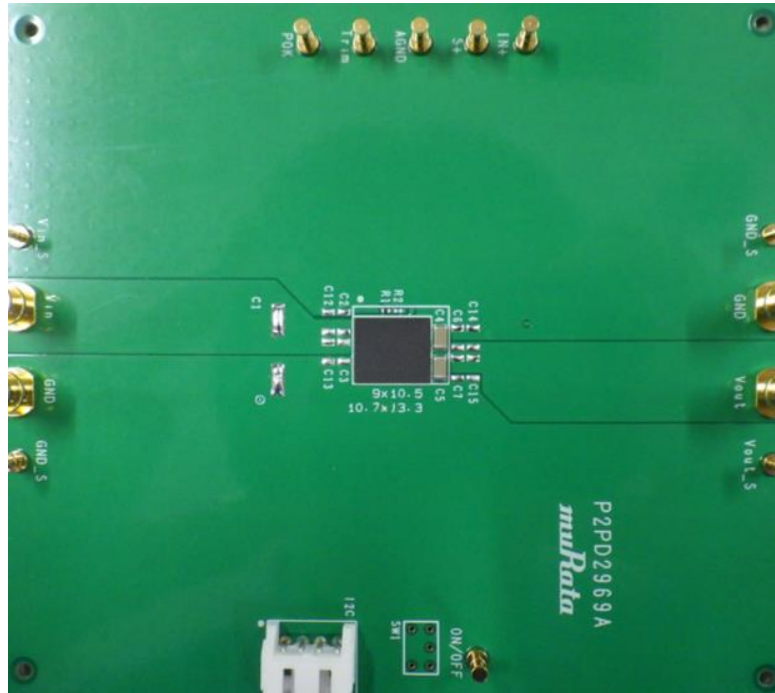


Figure 40. Application Board Example (Based on JEDEC standard)
 114.5 x 101.5 x 1.6mm (4 Layer FR-4)
 Outside copper(1,4) layer=2oz, Inner copper(2,3) layer=1oz

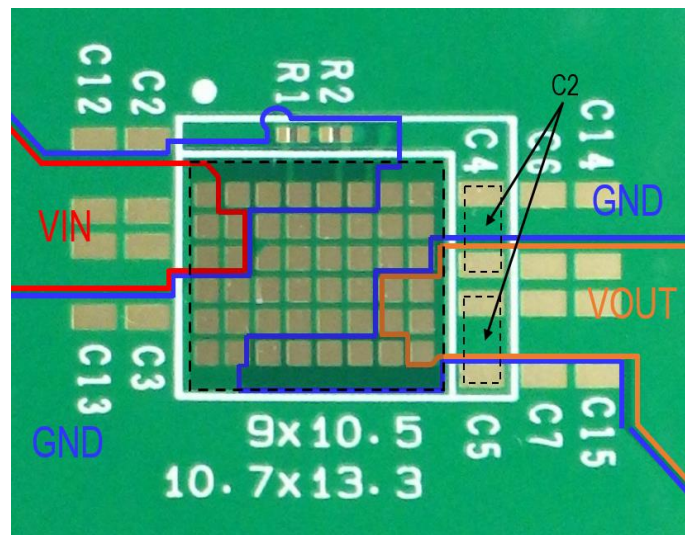


Figure 41. Land Pattern Example

Tape and Reel Specification
Tape Dimension

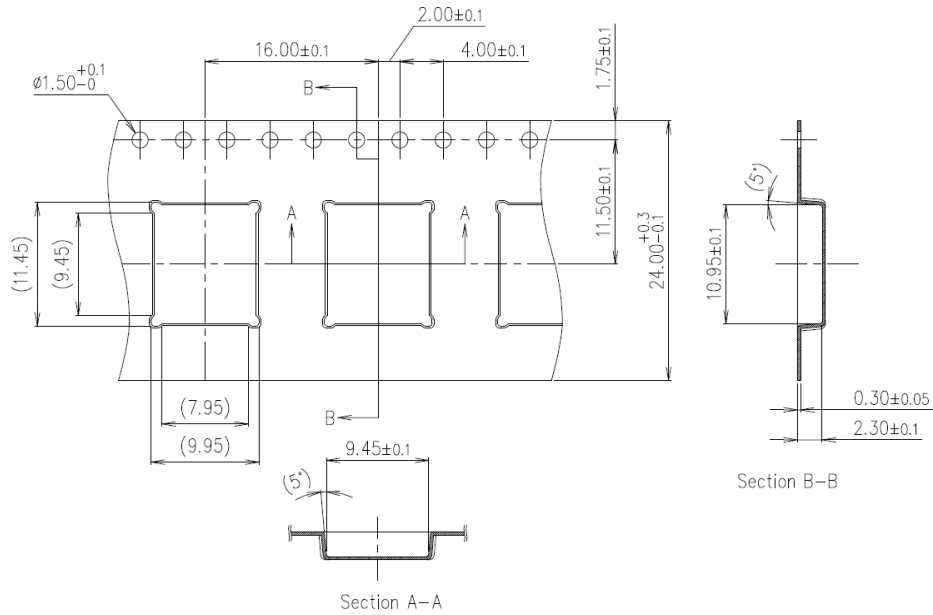


Figure 42. Tape Dimension

Reel Dimension

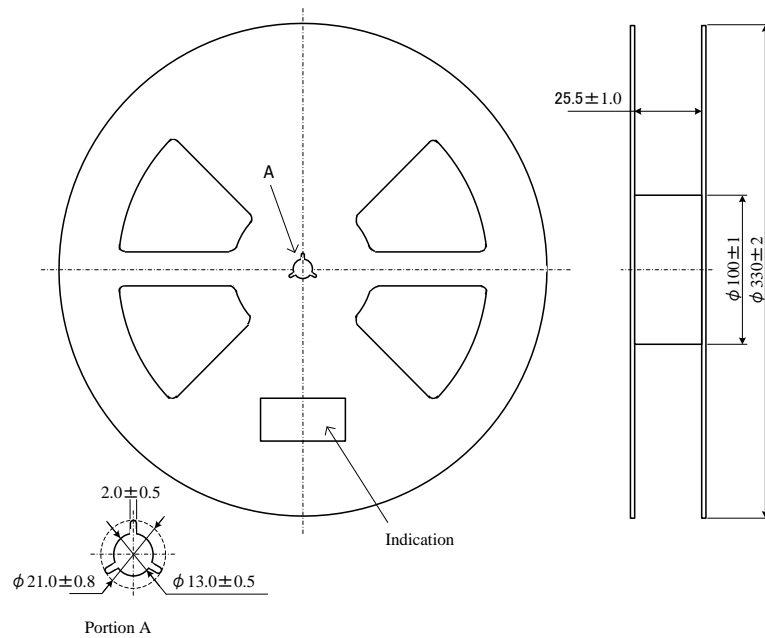


Figure 43. Reel Dimension

Module orientation in Tape

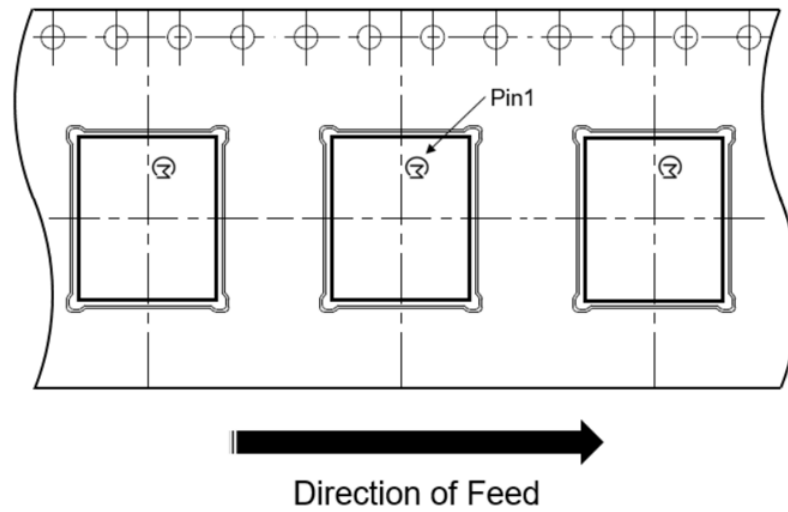


Figure 44. Module Orientation in Tape

Taping specification

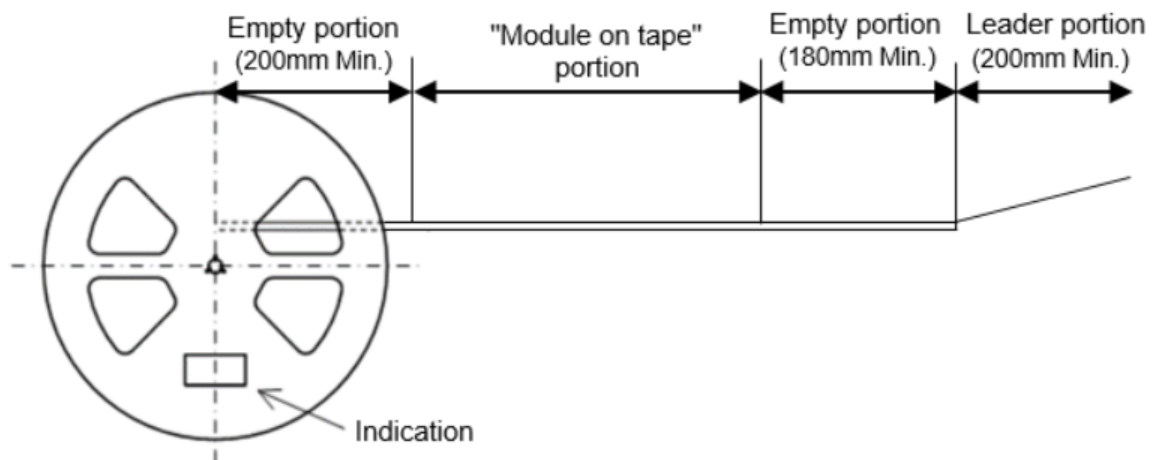


Figure 45. Taping Specification

1. The adhesive strength of the protective tape is within 0.1-1.3N.
2. Each reel contains 400 or 100pcs.
3. Each reel set in moisture-proof packaging because of MSL 3.
4. No vacant pocket in "Module on tape" section.
5. The reel is labeled with Murata part number and quantity.
6. The color of reel is not specified.

Order Codes

| ORDER CODES | DESCRIPTION | PACKAGING | SHIPPING METHOD |
|-------------------|------------------------------------|------------------------|-----------------|
| MYTNC1R86RELA2RA | MYTNC1R86RELA2RA Buck Converter | 10.5 x 9.0 x 2.1mm LGA | 400 units/T&R |
| MYTNC1R86RELA2RAD | MYTNC1R86RELA2RA Buck Converter | 10.5 x 9.0 x 2.1mm LGA | 100 units/T&R |

Table 13. Order Codes

Notices

CAUTION

Limitation of Applications

Please contact us before using our products for the applications listed below which require especially high reliability for the prevention of defects which might directly cause damage to the third party's life, body or property.

- Aircraft equipment
- Aerospace equipment
- Undersea equipment
- Power plant control equipment
- Medical equipment
- Transportation equipment (vehicles, trains, ships, etc.)
- Traffic signal equipment
- Disaster prevention / crime prevention equipment
- Data-processing equipment
- Application of similar complexity and/or reliability requirements to the applications listed in the above

Note

1. Please make sure that your product has been evaluated in view of your specifications with our product being mounted to your product.
2. You are requested not to use our product deviating from the reference specifications.
3. If you have any concerns about materials other than those listed in the RoHS directive, please contact us.
4. Be sure to provide an appropriate fail-safe function on your product to prevent a second damage that may be caused by the abnormal function or the failure of our product.
5. Please don't wash this product under any conditions.

Product Specification

Product Specification in this datasheet are as of August 2020. Specifications and features may change in any manner without notice. Please check with our sales representatives or product engineers.

Sales contact

For additional information, contact Sales at <https://www.murata.com/contactform>.

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[MAX25203BATJA/VY+](#) [MAX77874CEWM+](#) [XC9236D08CER-G](#) [ISL95338IRTZ](#) [MP3416GJ-P](#) [BD9S201NUX-CE2](#) [MP5461GC-Z](#)
[MPQ4415AGQB-Z](#) [MPQ4590GS-Z](#) [MCP1603-330IMC](#) [MCP1642B-18IMC](#) [MCP1642D-ADJIMC](#)