

30V P-Channel Enhancement Mode MOSFET

Description

The NP20P03D6 G uses advanced trench technology to provide excellent $R_{DS(ON)}$. This device is suitable for use as a load switch or in PWM applications.

General Features

- ◆ $V_{DS} = -30V$ $I_D = -20A$
 $R_{DS(ON)}(Typ.) = 16m\Omega$ @ $V_{GS} = -10V$
 $R_{DS(ON)}(Typ.) = 21m\Omega$ @ $V_{GS} = -4.5V$
- ◆ High power and current handing capability
- ◆ Lead free product is acquired
- ◆ Surface mount package
- ◆ 150 °C operating temperature
- ◆ 100% UIS tested

Application

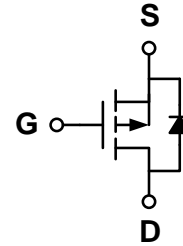
- ◆ PWM applications
- ◆ Load switch
- ◆ Uninterruptible power supply

Package

- ◆ PDFN5*6-8L-A

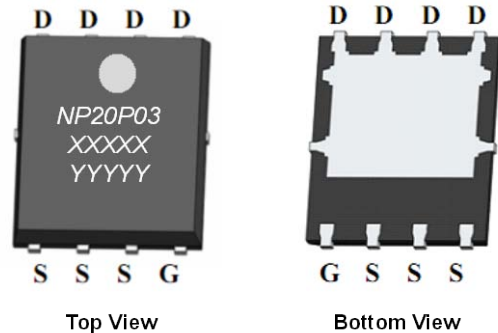
100% UIS TESTED!
100% ΔVds TESTED!

Schematic diagram



Marking and pin assignment

PDFN5*6-8L-A



XXXXX—Wafer Information
 YYYYY—Quality Code



Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
NP20P03D6-G	-55°C to +150°C	PDFN5*6-8L-A	5000

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

parameter	symbol	limit	unit
Drain-source voltage	V_{DS}	-30	V
Gate-source voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	TC=25°C	20
		TC=70°C	16
Pulsed Drain Current	I_{DP}	80	A
Avalanche energy (Tj=25°C, VDD=30V, VG=10V, L=0.5mH, Rg=25Ω)	E_{AS}	170	mJ
Power Dissipation	P_D	TC=25°C	31
		TC=70°C	15
Operating junction Temperature range	Tj	-55—150	°C

Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V$	-	-	1	μA
		$T_J=85^\circ C$	-	-	30	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 100	nA
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.2	-1.6	-2.5	V
Drain-source on-state resistance ¹	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-20A$	-	16	21	m Ω
		$V_{GS}=-4.5V, I_D=-15A$	-	21	26	
On Status Drain Current	$I_{D(ON)}$	$V_{DS}=-15V, V_{GS}=-10V$	25	-	-	A
Diode Characteristics						
Diode Forward Voltage ¹	V_{SD}	$I_{SD}=-20A, V_{GS}=0V$	-	-0.8	-1.3	V
Diode Continuous Forward Current	I_S		-	-25	-	A
Reverse Recovery Time	t_{rr}	$I_F=-20A,$ $di/dt=-100A/\mu s$	-	24	-	ns
Reverse Recovery Charge	Q_{rr}		-	16	-	nC
Dynamic Characteristics²						
Gate Resistance	R_G	$V_{GS}=0V, V_{DS}=0V, f=1MHz$	-	0.65	-	Ω
Input capacitance	C_{ISS}	$V_{GS}=0V, V_{DS}=-15V$ $f=1.0MHz$	-	1360	-	μF
Output capacitance	C_{OSS}		-	250	-	
Reverse transfer capacitance	C_{RSS}		-	210	-	
Turn-on delay time	$t_{D(ON)}$	$V_{GS}=-10V, V_{DD}=-30V,$ $R_L=3\Omega, I_D=20A, R_G=2.5\Omega$	-	9	-	ns
Turn-on Rise time	t_r		-	10	-	
Turn-off delay time	$t_{D(OFF)}$		-	50	-	
Turn-off Fall time	t_f		-	20	-	
Total gate charge	Q_g	$V_{GS}=-10V, I_D=-20A$ $V_{DS}=-15V$	-	31	-	nC
Gate-source charge	Q_{gs}		-	3	-	
Gate-drain charge	Q_{gd}		-	9	-	

Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	29	34	$^\circ C/W$
Maximum Junction-to-Ambient ^A		Steady-State	56	
Maximum Junction-to-Lead ^B	$R_{\theta JC}$	3.2	4	

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ C$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10s$ thermal resistance rating.

B: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

Typical Performance Characteristics

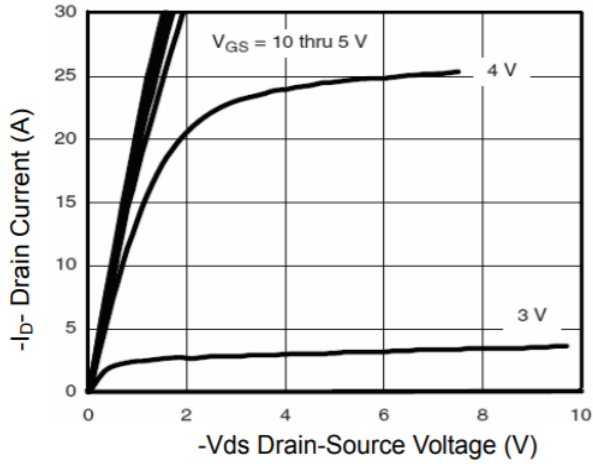


Figure 1 Output Characteristics

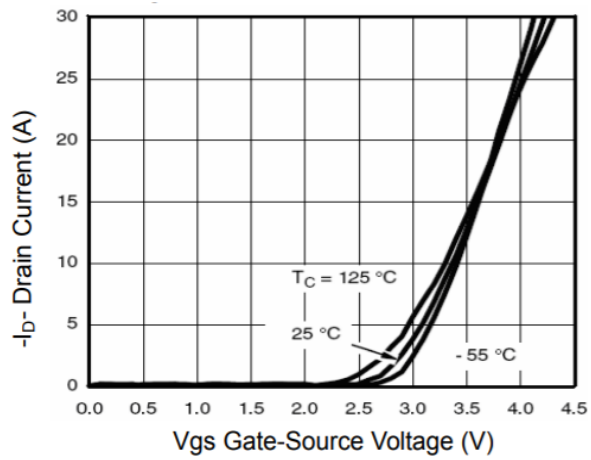


Figure 2 Transfer Characteristics

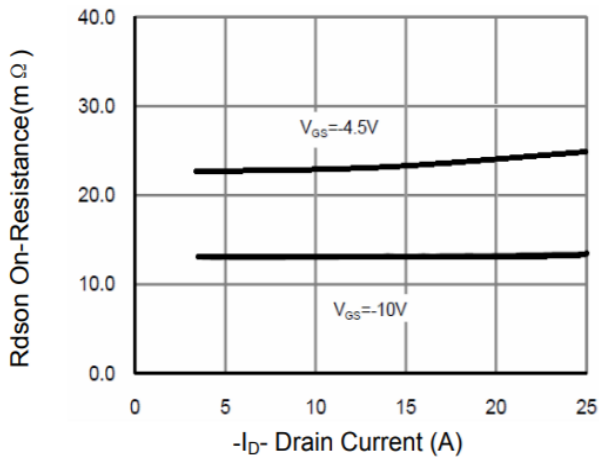


Figure 3 Rdson- Drain Current

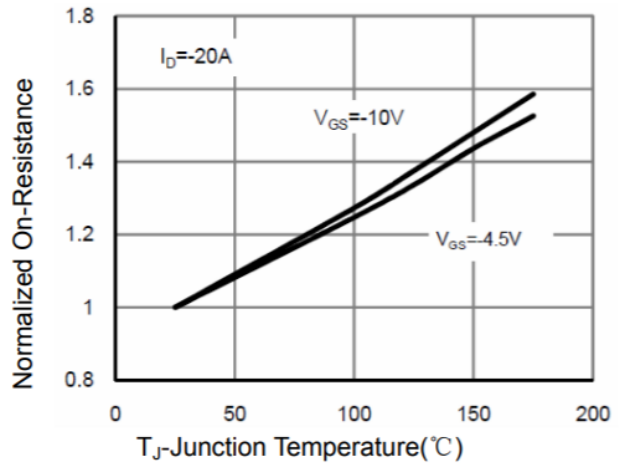


Figure 4 Rdson-Junction Temperature

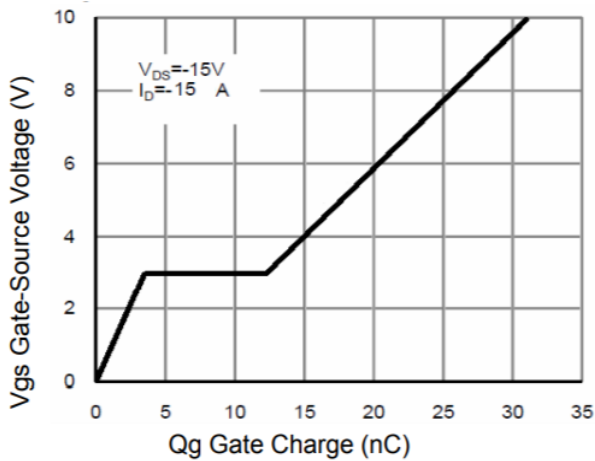


Figure 5 Gate Charge

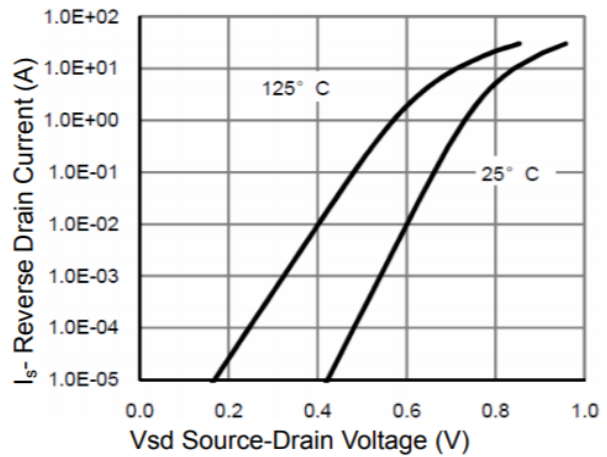


Figure 6 Source- Drain Diode Forward

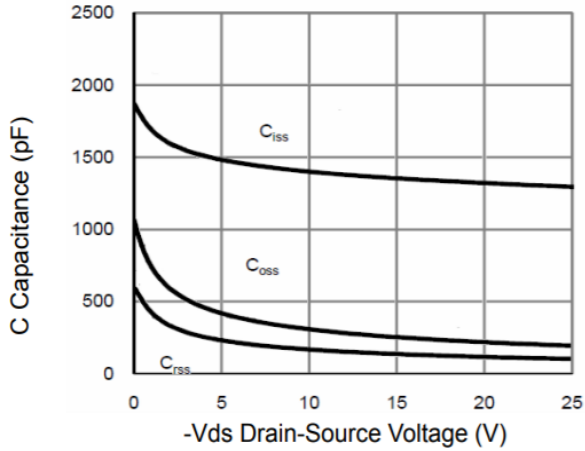


Figure 7 Capacitance vs Vds

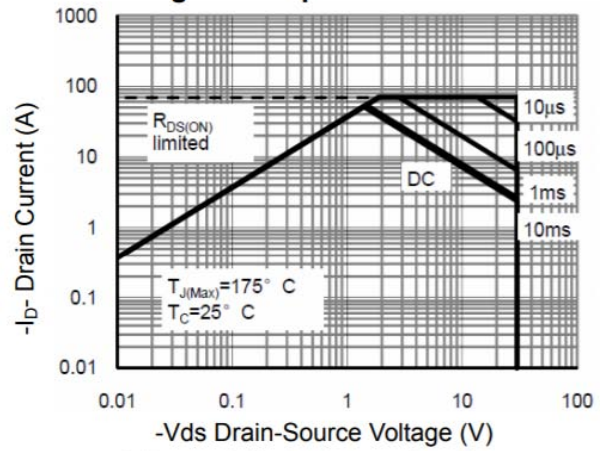


Figure 8 Safe Operation Area

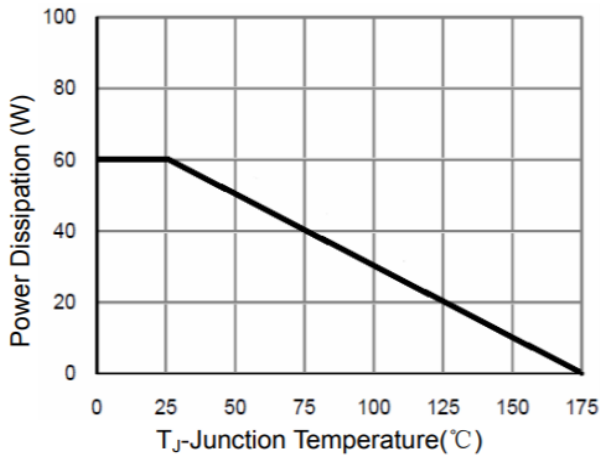


Figure 9 Power De-rating

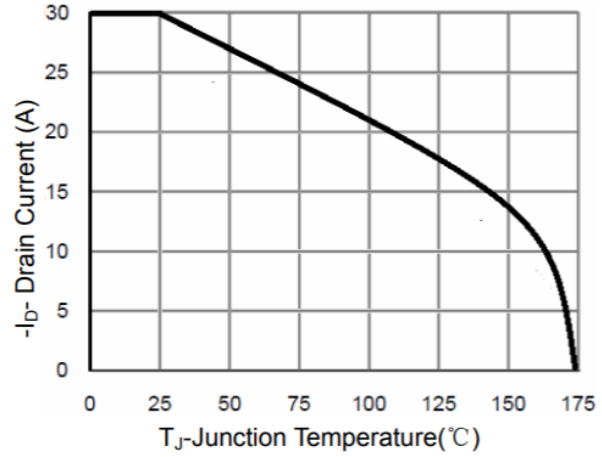


Figure 10 ID Current Derating

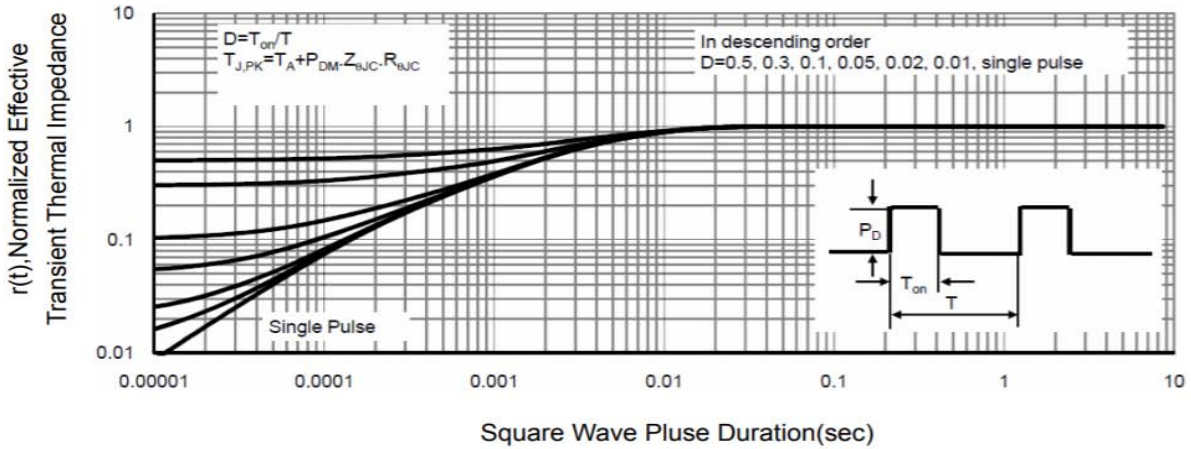


Figure 11 Normalized Maximum Transient Thermal Impedance

Figure A: Gate Charge Test Circuit & Waveforms

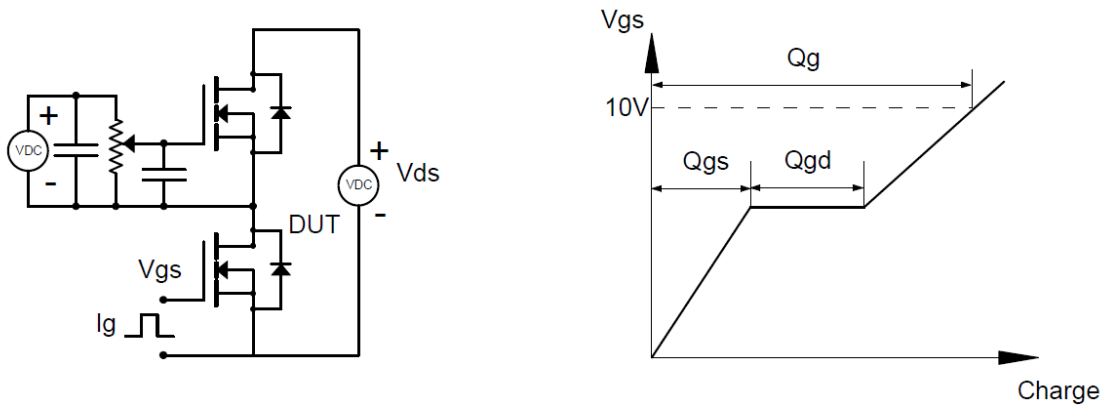


Figure B: Resistive Switching Test Circuit & Waveforms

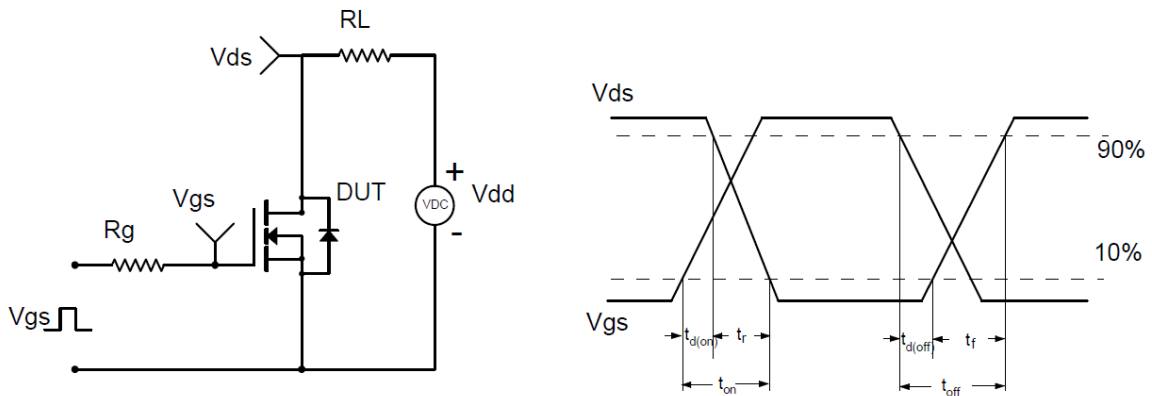


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

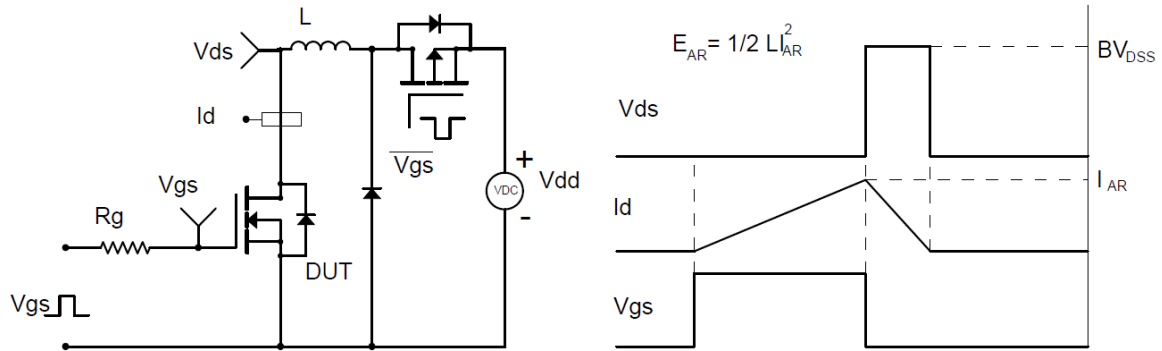
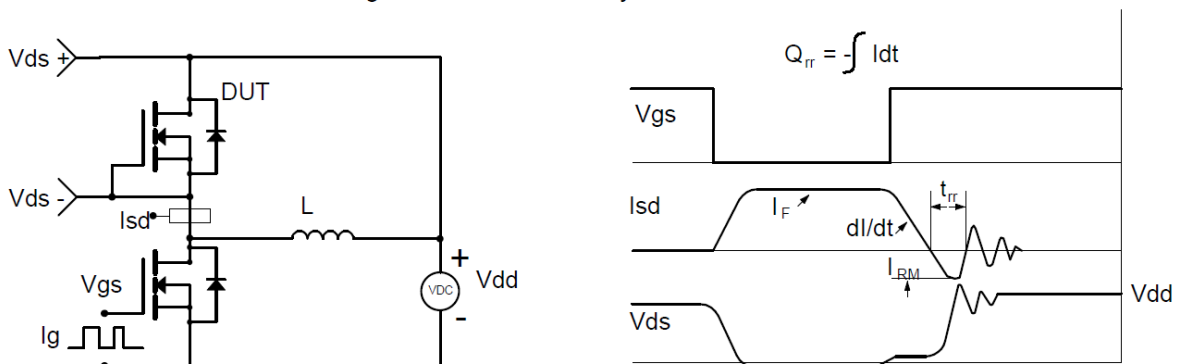
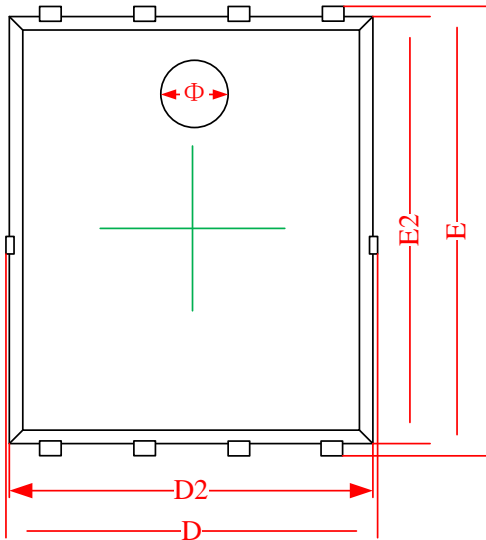
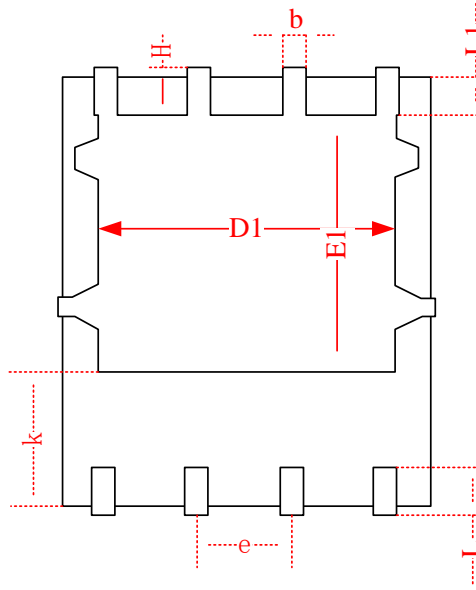
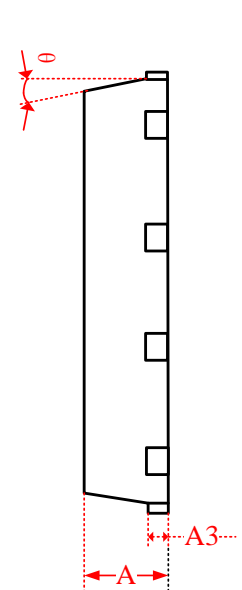


Figure D: Diode Recovery Test Circuit & Waveforms



Package Information

- PDFN5*6-8L-A

Top View

Bottom View

Side View


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.870	0.900	0.930	0.034	0.035	0.036
A3	0.152REF.			0.006REF.		
D	4.944	5.020	5.096	0.195	0.198	0.201
E	5.974	6.050	6.126	0.235	0.238	0.241
D1	3.910	4.010	4.110	0.154	0.158	0.162
E1	3.375	3.475	3.575	0.133	0.137	0.141
D2	4.870	4.900	4.930	0.192	0.193	0.194
E2	5.720	5.750	5.780	0.226	0.227	0.228
k	1.190	1.290	1.390	0.047	0.051	0.055
b	0.350	0.380	0.410	0.014	0.015	0.016
e	1.270TYP.			0.050TYP.		
L	0.559	0.635	0.711	0.022	0.025	0.028
L1	0.424	0.500	0.576	0.017	0.020	0.023
H	0.574	0.650	0.726	0.023	0.026	0.029
θ	10°	11°	12°	10°	11°	12°
Φ	1.150	1.200	1.250	0.045	0.047	0.049

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